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RULLI; A Photon Counting Imager

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RULLI is an acronym for Remote Ultra-Low Light Imager. The system responds to individual photons using a modification to conventional image intensifier technology and very fast TIM (time interval meter) electronics. Each photon received at the detector is resolved in three dimensions (X,Y, and time). The accumulation of photons over time allows the system to image with very low light levels such as starlight illumination. Using a low power pulsed laser and very fine time discrimination, three dimensional imaging can be accomplished with vertical resolution of a few cm.

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A Photon Counting Imager

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Abstract:

The Remote Low Light Imaging (RULLI) system responds to individual photons using a modification to conventional image intensifier technology and fast timing electronics. Each photon received at the detector is resolved in three dimensions (X, Y, and time). The accumulation of photons over time allows the system to image with very low light levels, such as starlight illumination. Using a low power pulsed laser and very fine time discrimination, three dimensional imaging has been accomplished with a vertical resolution of five cm.

Introduction

In standard high speed imaging, a focal plane array (FPA) will accumulate photo-electrons either directly from the scene illuminated by a strobed light source, or from a gated image intensifier. Thus the FPA acts as a photonic memory with the integrated scene information stored until the information is accessed. After accumulating the photons which originated from the scene and moment of interest, the pixels in the focal plane array are read out in a parallel-serial process. The serial transfer of a line of data through the output amplifier is often the rate-limiting step. Recent advances in focal plane arrays such as parallel or multi-port readouts and high bandwidth output amplifiers have increased the frame rate capabilities of high-speed cameras to many thousands of frames per second.

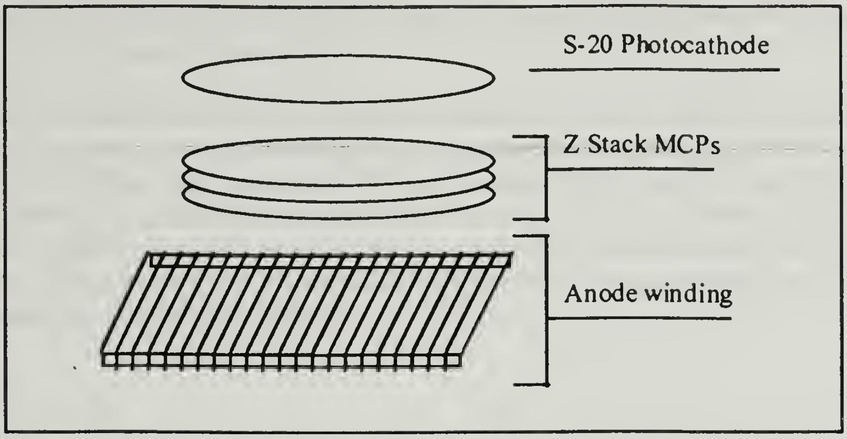
In contrast, this detector system processes each photon event as it occurs. The detector is made up of a standard micro-channel-plate (MCP) image-intensifier front end with high gain for photon counting and with a wire-wound crossed delay-line (CDL) anode. Thus it is referred to as an MCP/CDL detector. The detector signals are input into fast front-end electronics, called Pulse Absolute Timing (PAT) channels. The PAT channel converts the analog signal from the detector into the raw time information needed to determine the position and time of arrival of the photon with respect to the photo-cathode. Final data display is provided through custom processing software.

By sensing each photon for position and time of arrival, several important new approaches to imaging are possible. First is the ability to image with near noiseless performance. For low light conditions, this enables long integration times with contrast improvement, since only scene-generated photons are collected. For visible photons this is achieved without having to cool the detector. Second is the ability to deblur an image based solely on the scene contrast. Since the MCP/CDL is not integrating photons in the sense of a FPA, post processing of high contrast elements within the scene enable a reordering of the image over time. Third is the ability to image in three dimensions, when using a synchronously pulsed light source. This gives a very flexible imaging system that can provide much more information than standard focal plane systems. A report was published that rigorously treats various applications of this system [1].

The detector

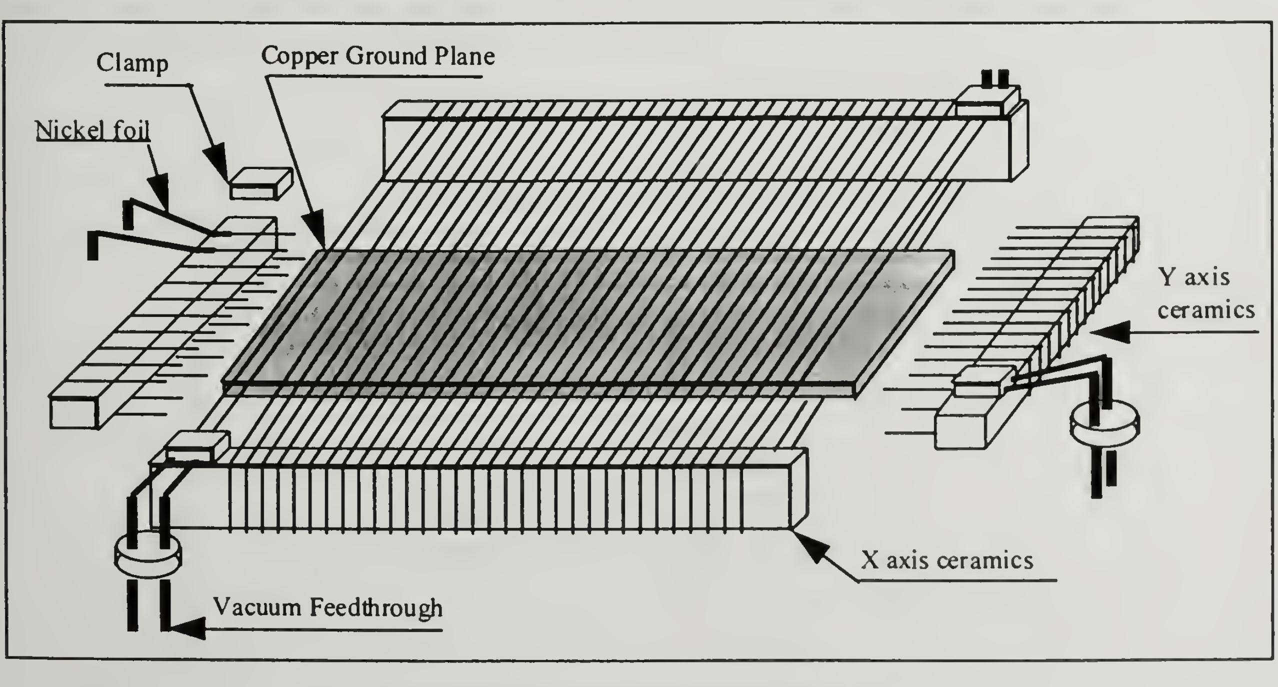
The detector is operated in a photon counting mode. The detector uses a low noise S-20 photocathode for photon detection, and a triple (Z) stack of micro-channel-plates (MCPs) for electronic gain (up to 10^7).

The front end components, the photocathode and MCPs, are from a resistive anode tube design that is a commercial product.



Drawing of basic elements of micro-channel-plate crossed-delay-line detector.

The remainder of the tube is the CDL wire anode [2,3]. It consists of two windings, each about 100 feet long, wound around a 3.5 in. square copper ground plane with insulating ceramic edges. One set of ceramic edges is larger in height from the ground plane than the other. Thus there is an inner wire winding in one direction (Y axis), and an slightly larger orthogonal winding for the other direction (X axis). In the drawing below, the Yaxis wires are cut away for clarity. Each winding is composed of a bifilar coil of Cu-Zr wires, that is two wires are spooled simultaneously with a fixed space between them. They are pulled with substantial tension so that as the wires pass over the ceramic insulator, they form a taught flat grid in parallel to the copper ground plane. Effort has been made to ensure the wires maintain their tension through the tube processing, which includes a 300 deg C bake-out cycle. The bifilar construction of each winding yields a balanced transmission line for the high frequency signals to propagate along, with a slight (18V) bias from one line to the next. The end of the wire is carefully clamped with a thin (0.002 in) nickel foil strip wrapped around it. Each nickel strip is then attached to a vacuum feedthrough pin in order to make electrical connection outside the tube.



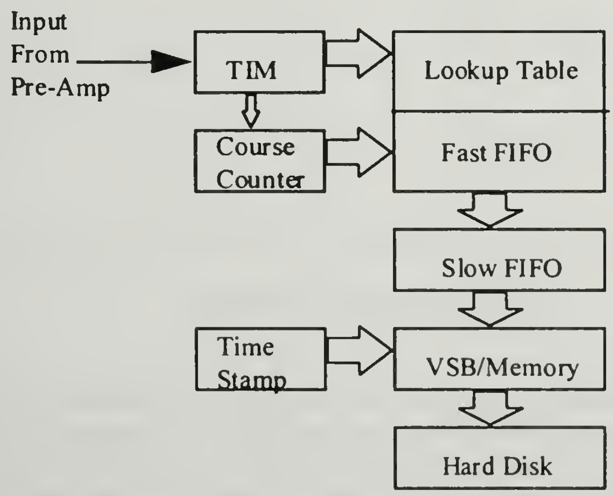
Drawing of wire-wound crossed delay line anode.

Thus, there is a three level structure through which the cloud of electrons move, giving rise to simultaneous signals on the outer winding, the inner winding, and lastly being absorbed into the copper ground plane. There are the same three levels seen from the back side, which are shielded from seeing electrons by the innermost layer, the solid copper ground plane.

The Z stack MCPs are biased so that the last plate is in saturation, giving a nearly constant electron gain for each photon that is detected. The amplified electrons are moderately accelerated (700V) from the last MCP to the wire-wound delay-line anode where they spread and strike an area at least a few wire diameters wide. From the interaction, a signal is impressed on each wire due to electrons that are captured, secondary electrons that are released or absorbed, and currents induced by the electrons passing through the small bifilar field (18V). This current signal propagates to each end of the winding where it is extracted through vacuum feedthroughs to external preamplifiers.

The electronics

The pulse absolute timing, or PAT, electronics are comprised of a wide bandwidth four channel preamplifier at the detector, and four VME modules. One double width VME module is used for each PAT channel and it has an associated single width memory module sitting next to it in the VME chassis. There are four PAT channels in the system. The electronics of each PAT channel are designed around a custom 1X3 in. hybrid electronics module called a time interval meter (TIM). The TIM includes a number of internal circuits; a constant fraction discriminator (CFD) front end, a dual interpolator stage, and a ten bit time to digital converter (TDC). The TIM of each channel is connected to one of the ends from the two windings of the detector anode, hence the need for four channels. About 80 ns after a trigger, that is a photon signal from the detector, the TIM generates a fine count number. The fine count is the difference between the time of a trigger and the clock phase of a very stable 100 MHz system clock, expressed with 20 ps of accuracy. The fine count is passed through a lookup table, which provides correction for linearity and other artifacts. External to the TIM, but triggered from it, is a course counter, which keeps track of time in 10 ns increments over the course of a collection period. The two count values, fine and course, are passed on to a fast FIFO for intermediate ordering. The fast FIFO is followed by a slow FIFO, which parallels the data, and synchronizes the data with a VSB interface. At the interface, a periodic time stamp is inserted which keeps the data in records of know time duration. The data from each channel, and time stamps, are stored in a fast RAM memory card (128 or 256 Mb) which sits on the VSB bus. When the acquisition is complete, the data is transferred to a hard disk array.

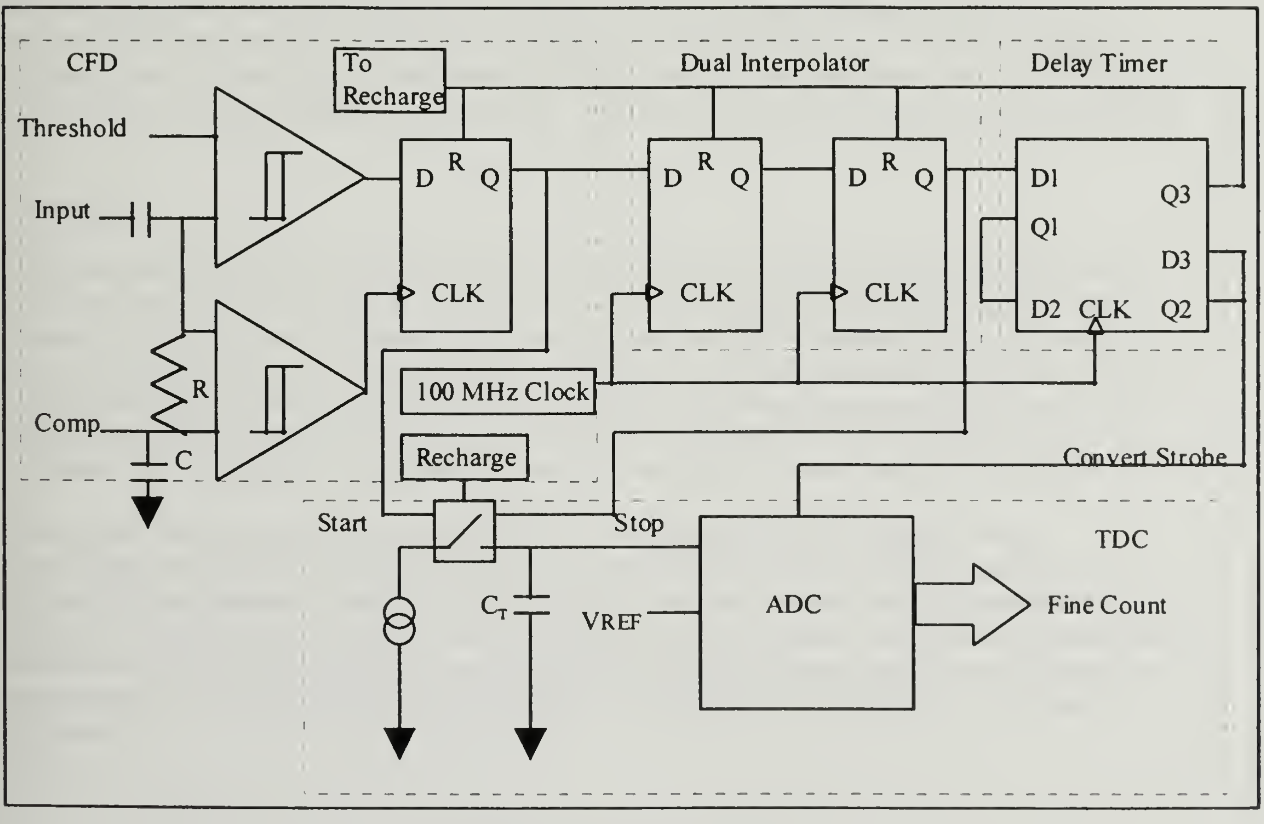


Block diagram of the Electronics System.

TIM electronics

Time is measured by recording the cycle number of the reference clock and the clock phase at which an event arrived. First the CFD latch and the dual interpolator latches form a pulse whose duration is proportional to the phase plus 1 clock width. This pulse duration is used to switch a constant current source to a capacitor and store an analog voltage that is proportional to the arrival phase. Also the pulse edge is used to select an unambiguous cycle of the clock. Those two values combine to compute the time.

The CFD used in the TIM is a modification of one originally designed by Bojan Turko and R. Clayton Smith. It was shown that this circuit was capable of detecting signals with amplitude variation of 40 dB, while maintaining a time walk of less than 100 ps [4]. The circuit is built using two high speed ECL comparators. The first comparator sets the threshold of the input signal, triggering on the leading edge of the detector pulse. The second comparator sees a slightly integrated version of the input signal, and compares it to a reference level called compensation, which is usually set close to ground. The first comparator passes a logic level to the data input of an ECL D flip flop, while the second comparator triggers the clock input of the same D flip flop. With this dual trigger approach, and the slight integration of the input signal, the CFD is able to maintain a stable firing time even if the pulse amplitude varies over a range of 100:1. The complementary outputs of the D flip flop are fed to the inputs of the dual interpolator stage.



Schematic of TIM hybrid circuit.

The ADC is a 10 bit 40 MHz Flash ADC chip, and requires 20 ns of setup and hold time. After halting the discharge of the timing capacitor, C_T, the CFD trigger signal from the second stage of the dual interpolator is clocked through two periods of the 100 MHz system clock through two more stages of D flip flops. After the 20 ns delay, the ADC is triggered to convert the voltage remaining on the capacitor to a digital output. A final stage of D flip flop is used to delay the CFD trigger signal for 10 ns. The output of this final delay is used to send a reset signal to all the gates, and to a recharge circuit which brings the voltage on the capacitor back to the initialized level.

Data Processing:

Post processing, or photon event reconstruction, is the step where the position of the photon relative to the photocathode is calculated, based on the raw timing data sets previously stored on disk. The photon event reconstruction software compares the relative time it takes a pulse to arrive at each end of the delay line with the sum equal to the total delay of the winding. Using this test for appropriate pairing, the data set is reduced by a small amount as some data pairs are rejected. The data is then matched, in order associate appropriate pairs from each axis, so that a two dimensional position is determined for the initial photon event. By summing these spatial events over time, the analysis yields a two dimensional data set equivalent to a "frame". For FPA based imaging, a frame is usually taken as both fixed in spatial and in temporal dimensions. The temporal dimension here can be adjusted for as long a time as is needed for developing sufficient photon statistics in constructing the image.

For three dimensional imaging, a pulsed light source is used that is time synchronous with the PAT system. The source employed in several recent experiments is a Hamamatsu PLP-01 solid state diode laser. This laser has a pulse width of 85 ps at 655 nm wavelength, and was operated synchronously by dividing down the 100 MHz system clock to 1.56 MHz. By ordering the data into pulse synchronous time bins, an additional level of association is calculated that results in a distance determination with resolution of 5 cm or better. Three dimensional structures from a 3X3X3 ft. box to a polystyrene target with the LANL logo in 2 in. letters have been imaged with this system. These experiments are described in detail elsewhere [5].

Conclusion:

The approach of imaging by photon counting is not new. But most systems suffer from deadtime issues which limit their useful counting rates to no more than a few thousand to a hundred thousand counts per second. This system currently operates at 10 times that rate, and has the potential of another factor of three or more increase in photon rate. The high speed electronics, which have made this performance possible, are built using hybrid electronics techniques. Even higher performance is expected out of newer ASIC IC designs that are being proposed. In fact, an very high precision, though lower speed ASIC IC has been developed which can achieve better than 10 ps accuracy with very low power and space requirements.

The system described was first proposed in 1993. A prototype was rapidly constructed which demonstrated the utility of the approach, especially as applied to UV imaging. An intermediate prototype was developed and operated from 1994 to 1996. By mid-1997, the PAT version of the system was developed. Also in 1997, a new tube vendor was producing robust detectors, which could be used in field experiments as well as the laboratory. Several field experiments have been conducted over the past year proving that the system has several unique capabilities which complement existing low light imaging techniques.

Acknowledgements

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