Error Correction Circuits for Bio-Implantable Electronics

Chris Winstead and Yi Luo
Dept. of Electrical and Computer Engineering
Utah State University
Logan, UT 84322
chris.winstead@usu.edu

***Abstract*—Methods are reviewed for achieving high data rates in bio-implantable devices. Particular attention is given to cortical stimulator arrays for restoring vision. Error-correction codes (ECC) are shown to be essential to obtain reliable operation in next-generation high-rate implants. A survey of reported ECC implementations is presented, and power-vs-performance tradeoffs are revealed after re-scaling to remove differences in technology and clock speed. Recommendations are offered for realizing high-rate ECC circuits within the tight power constraints of implantable device applications.**

I. Introduction

Error correction codes (ECC) are widely used to optimize performance in wireless communication devices. Some advanced ECC techniques are able to approach theoretical limits on performance, which is defined by the minimum signal energy needed to maintain reliable operation. Unfortunately the advanced ECC implementations consume more than 100mW of power. Because of this high power consumption, ECC components are a limiting factor in power consumption of high-performance wireless devices. Advanced ECC options are also inaccessible to micro-power communication devices, which are increasingly important for biomedical applications, personal area networks and distributed sensor networks. In this paper, we survey the literature on ECC implementations and identify methods for incorporating ECC into power-constrained applications.

Cut point.

The field of bio-implantable electronics comprises a rapidly expanding family of applications and has attracted considerable research interest. As the capabilities of bio-implantable devices expand, their data communication requirements become more demanding. This is especially true for applications in neural rehabilitation and brain-machine interfaces, which provide wireless transmission of complex neural signals [1]. The challenges are compounded if the communication bandwidth is shared among many stimulating and recording sites. Vision restoration systems, like the one illustrated in Fig. 1, are applications that require a large array of stimulating sites and a correspondingly high bandwidth for wireless transmission [2], [3].

Neural stimulator arrays are subject to a different set of constraints from traditional communication systems. Traditional systems are commonly designed to minimize the energy expended by a transmitter. In a bio-implanted device, by contrast, it is more important to minimize power consumed by the implanted device. Any power consumed by the implanted receiver is dissipated as excess heat, which can cause tissue damage within the body. There is consequently a need to devise high-speed receiver circuits with power consumption on the order of 10mW or less. Over the past decade, several cortical data links were demonstrated with typical rates in the range of 1–10Mbps [2]–[10]. While data rates in this range are deemed sufficient to restore minimal visual function, a larger throughput is required in order to provide quality vision [11].

In this paper we review recent results on high-rate communication for cortical implants. Very high-rate communication is made possible by using impulse radio ultra-wideband (IR-UWB) transmission, proposed by Charles as a low-power method suitable for cortical implants [12], [13]. Impulse radio signals suffer from significant attenuation within the body. Furthermore, power limitations force the use of low-complexity receiver circuits which introduce additional noise and jitter, potentially rendering the system unusable. The author recently reported a candidate IR-UWB system in which these effects are fully compensated by the use of error correction codes (ECC) [14].

In the remainder of this paper, recent results are summarized on applying ECC for high-rate implantable IR-UWB receivers. Available ECC options are compared and assessed in terms of their performance and power consumption, and conclusions are offered for realizing power-compatible ECC devices for implantable applications.

II. Error-correction in cortical data links

A variety of wireless circuits for cortical applications were demonstrated during the past decade. In most cases these circuits utilized narrow-band modulations, mainly Amplitude-Shift Keying (ASK) [6] or Phase-Shift Keying (PSK) [3], [8], [15]. More recently an impulse-based solution known as Pulse-Harmonic Modulation was introduced by Inanlou and Ghovanloo [7], which delivered a throughput of 10.2Mbps, the highest reported to date. All of these systems utilize resonant behavior in the coupled coils that comprise the transcutaneous link. By utilizing self-resonance in the link, it is possible to deliver high-amplitude signals to the implanted device. The coils' self-resonance frequency also constrains the choice of

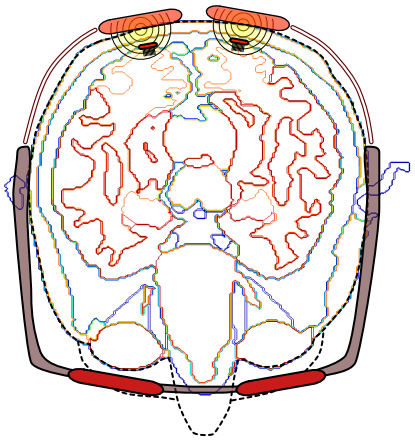

Fig. 1. Cortical implant system for stimulating the visual cortex. Image data is collected from cameras mounted on glasses. The data is translated into a neural stimulus pattern, which is transmitted to cortical implants via a wireless inductive transcutaneous link.

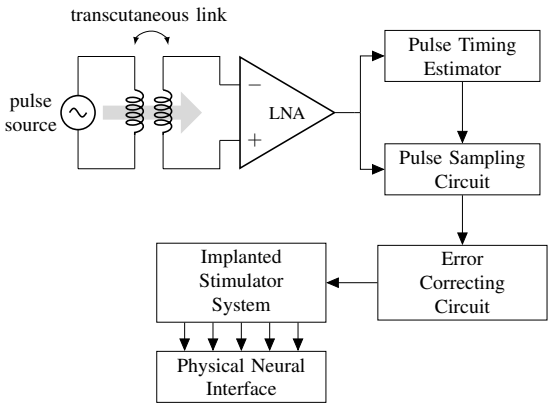

Fig. 2. Receiver architecture [14] based on a UWB receiver described by Hu, Chiang et al. [16]. Pulse timing is obtained using a low-complexity injection-locking VCO circuit.

carrier frequency, which consequently limits the achievable throughput in these systems.

To achieve an ultra-wideband data link, the author proposed adapting an IR-UWB system described by Hu [16], which consumes 90pJ/bit at a maximum throughput of 500Mbps. The modified receiver architecture is shown in Fig. 2. In order to adapt this system to the cortical implant application, it is necessary to suppress the coils' self resonance so that the link has a relatively flat frequency response. The flat response minimizes pulse distortion and inter-symbol interference, but also introduces significant attenuation.

An ECC layer is added to the architecture in Fig. 2. Simulation results indicate that the receiver's pulse-timing jitter, together with the undesirable channel characteristics, induce an *error floor* which prevents the system from functioning reliably. When the ECC component is introduced, as shown in Fig. 3, the error floor is eliminated and the system's reliability can be made quite low. These results indicate that it should be possible to increase the data rate by an order of magnitude

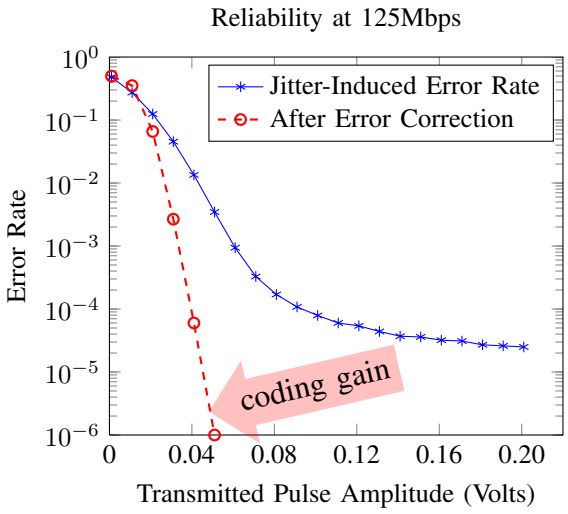

Fig. 3. Bit Error Rate (BER) results for the implantable UWB receiver [14]. The injection locking method introduces substantial timing jitter, which makes the receiver unusable unless ECC is applied. In this example, a low-complexity hard-decision (HD) ECC decoder was used.

compared to current solutions, if a suitably low-power ECC solution is available.

III. Comparison of ECC Solutions

Efficient circuits and algorithms for ECC have been pursued since the 1950's, and a wide variety of codes and implementations have been devised. Until the 1990's most research focused on low-complexity hard-decision (HD) and bit-flipping decoder designs. During the past two decades, significant effort was invested in implementing high-performance ECC decoders based on Turbo codes [17] and Low-Density Parity-Check (LDPC) codes [18], [19], which are known to approach the theoretical Shannon Limit on communication performance. Some of the earliest implementations required as much as 1W of power, which prompted some researchers to propose analog implementations [20], [21], which are comprised of continuous-time micro-current processing arrays. Analog decoders are also appealing for use in power constrained applications because the total power consumption is precisely specifiable and easily controlled.

A. Technology scaling trends in ECC implementations

Analog implementations initially proved much more power efficient than digital options, but that gain has diminished recently due to steady improvements in digital efficiency. To a great extent, the improvements in digital efficiency are attributable to technology scaling. Fig. 4 shows the power efficiency of reported digital ECC chips, arranged by technology node. Fig. 4 also shows a dashed line indicating the improvements that would be expected due to scaling theory [22].

B. Technology-adjusted performance of ECC implementations

The reported implementations are demonstrated in a variety of different technologies, making it difficult to assess

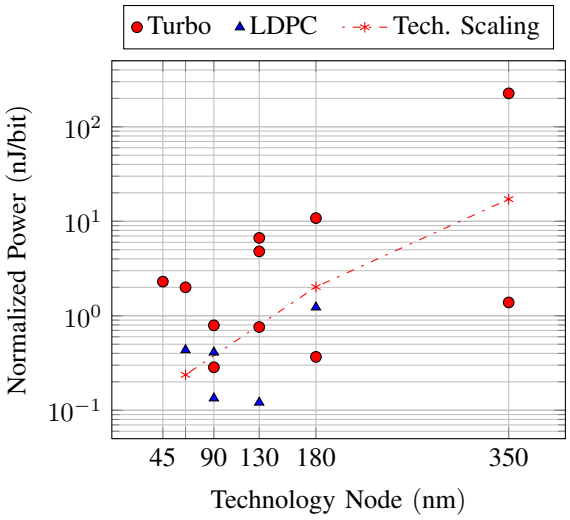

Fig. 4. Technology scaling trends in digital ECC implementations, including Turbo decoders [23]–[31]and LDPC decoders [32]–[40]. Also shown is the trend line predicted by Dennard scaling theory [22].

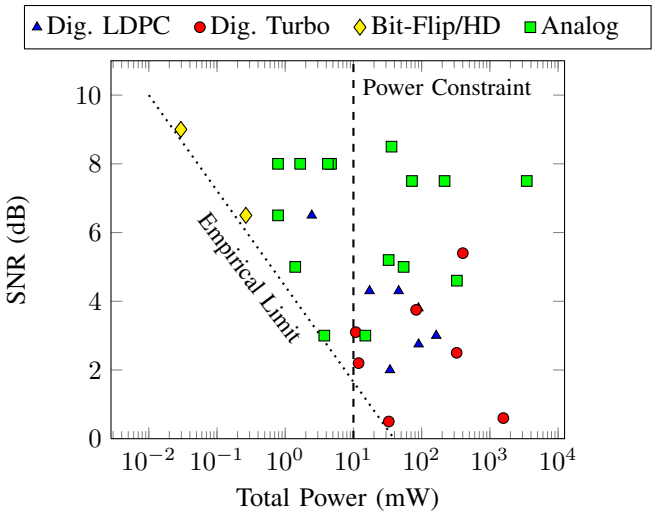

Fig. 5. Comparison of scaled power and performance among reported decoder implementations, including digital Turbo decoders [23]–[31], digital LDPC decoders [32]–[40], and a variety of analog decoders [42]–[49]. Also shown are two hard-decision decoders that were synthesized for this work. All power numbers are scaled to a common 65nm technology, and are normalized to a fixed throughput of 200Mbps. The SNR is defined as the signal-to-noise ratio required for a decoder to achieve a bit error-rate of 10^{-5} on a standard binary-input additive white Gaussian noise channel.

differences attributable to algorithm and architecture choices. These comparisons must ideally be made between circuits implemented in a common technology, operating at a common throughput. In order to properly compare the efficiencies of competing ECC designs, the figures may be adjusted to predict their expected performance when migrated to a designated reference technology.

Approximate adjustments can be made by appealing to generalized process scaling rules, which account for typical differences in supply voltage and terminal capacitance [22]. For digital designs, the adjusted efficiency is obtained by multiplying the power ratio γ_D, defined as

$$\gamma_D = \frac{C_2 V_{\text{DD}2}^2}{C_1 V_{\text{DD}1}^2} = \xi^2,$$

where ξ is the technology scale ratio, the subscript '1' indicates the original reported technology, and subscript '2' indicates the target reference technology.

For scaling analog designs, the scaling ratio is somewhat different because analog ECC implementations are usually based on continuous-time processing with current-mode circuits. The efficiency is therefore linear with V_{DD}, and the power ratio is

$$\gamma_A = \frac{C_2 V_{\text{DD}2}}{C_1 V_{\text{DD}1}} = \xi^{3/2}.$$

These predictions indicate that technology scaling should be more favorable for digital implementations than analog. It has furthermore been argued that traditional analog designs cannot be migrated into nanometer-scale technologies due to matching limitations [41].

Fig. 5 presents a variety of reported decoder designs, revealing the tradeoff between the required signal-to-noise ratio (SNR) and the expected total power consumption. For implantable device applications, 10mW is assumed as an absolute maximum power constraint, as indicated in Fig. 5. For this analysis, two hard-decision bit-flipping decoders were designed based on traditional hard-decision algorithms [18], and were synthesized using the FreePDK45 design flow. For the reported designs, an approximate throughput adjustment is obtained via clock-frequency scaling. This method neglects the high leakage power of some digital designs. Leakage power is not always reported, but has been measured as high as 50mW. The results indicate that some digital Turbo decoders come close to the power constraint, but only the analog and bit-flipping designs fall significantly below the power limit.

IV. Conclusions

ECC algorithms were shown to be an enabling solution for very high-speed implantable data links. Analog and bit-flipping decoder circuits were shown to provide the safest options for meeting low-power constraints. High-performance digital options have become more efficient over time, but the improvements are largely correlated with process scaling. In the future, process scaling may offer diminishing returns for these high-activity algorithms. Analog designs are similarly limited by mismatch effects. In order to migrate analog designs to newer technology generations (65nm and below), it will be necessary to devise mismatch-tolerant versions of analog decoding circuits. We may conclude that hard-decision and bit-flipping methods offer the best compatibility for near-term applications in bio-implantable electronics.

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