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# Design and Control for High Efficiency in High Step-Down Dual Active Bridge Converters Operating at High Switching Frequency

D. Costinett

D. Maksimovic

Zane Regan
*Utah State University*

# Design and Control for High Efficiency in High Step-Down Dual Active Bridge Converters Operating at High Switching Frequency

Daniel Costinett, *Student Member, IEEE,* Dragan Maksimović, *Senior Member, IEE,* and Regan Zane, *Senior Member, IEEE*

***Abstract*—A control scheme is developed to maximize efficiency over a wide range of loads for a Dual Active Bridge (DAB) converter. A simple control circuit using only phase-shift modulation is proposed which considers both the converter conversion ratio and switching dead times in order to maintain high efficiency in the presence of varying loads. To demonstrate feasibility of the proposed control method, experimental results are presented for a 150-to-12 V, 120 W, 1 MHz prototype converter which has 97.4% peak efficiency and maintains greater than 90% efficiency over a load range between 20 W and 120 W.**

## I. Introduction

THE Dual Active Bridge (DAB) converter of Fig. 1 has been given considerable interest in recent years for its favorable characteristics, including zero voltage switching (ZVS) of all devices, near-minimum voltage and current stresses, and integrated transformer turns ratio [1]–[5]. The DAB architecture has therefore been selected to operate as an unregulated, 150-to-12 V, 120 W, 1 MHz converter. In this paper, the term "unregulated" refers to the output voltage not being controlled to follow a fixed reference but instead being adjusted in closed loop for the purpose of improving efficiency. This type of converter can find many applications, e.g. as a bus converter for DC power distribution [6]–[9], where the presence of subsequent point-of-load converters removes the need for tight output voltage regulation. Additionally, the 1 MHz switching frequency, high efficiency, and relatively low output power allow for a small overall converter size.

Previous studies have shown methods for offline efficiency optimization of the DAB converter that are able to set wide ZVS range while maintaining low RMS currents through all devices [10], [11]. Additionally, online efficiency improvements have been proposed which alter switch control schemes in order to extend the ZVS range and improve light load efficiency [12]–[16]. In these methods, multiple switch modulation schemes are used across varying load conditions, resulting in improved efficiency at the expense of increased control complexity. This work takes advantage of the unregulated nature of the application by using the ability to dynamically adjust the output voltage of the converter to extend ZVS range of the high voltage primary devices and achieve high efficiency while maintaining a simple phase shift modulation control strategy across the entire range of load conditions.

The DAB converter has been analyzed extensively with output power above 1 kW and switching frequency below 100 kHz [1]–[3], [10]–[17]. Under these conditions, resonant intervals responsible for achieving ZVS occupy a sufficiently small percentage of the switching period to allow their exclusion from converter analysis. However, at higher frequencies and lower output power levels, the resonant interval resulting in primary-side ZVS corresponds to a significant portion of the switching period, and must be included in the analysis of converter operation. This work seeks to examine the nature of this ZVS interval across a full range of load conditions and use the resulting analysis to develop a simple, high-efficiency control strategy for the unregulated DAB converter.

The different operating modes of the converter across varying output power and voltage are analyzed in Section II; a loss model across these operating modes is developed in Section III. Section IV employs the loss model to determine the optimal "trajectory" across which the output voltage should be varied in the presence of load variations. Section V details the proposed control architecture to dynamically set both the output voltage and timing parameters. Section VI presents experimental results confirming the feasibility of implementing this control. Section VII concludes the paper.

## II. Analysis of DAB Operating Modes

Analysis, taking into account the resonant ZVS transitions, has been completed in [18] under the condition that output

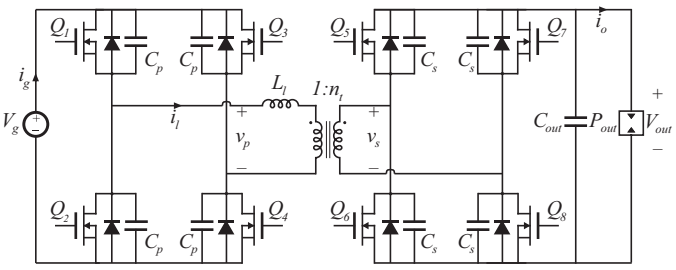


Fig. 1. Dual active bridge architecture. Linear time-equivalent capacitances $C_p$ and $C_s$ to nonlinear device output capacitances on the primary and secondary side are shown explicitly.

Daniel Costinett and Dragan Maksimović are with the Department of Electrical, Computer, and Energy Engineering, University of Colorado, Boulder, CO, 80309 USA. Regan Zane is with the Department of Electrical and Computer Engineering at Utah State University, Logan, UT 84322 USA.
e-mail: Daniel.Costinett@Colorado.edu

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power is large enough to achieve ZVS of all devices and $V_{out} = n_t V_g$; i.e. the conversion ratio is equal to the transformer turns ratio. A new solution is developed for the more general case of $V_{out} = n_{ctrl} V_g$, where $n_{ctrl}$ is the converter conversion ratio, and is not necessarily equal to the transformer turns ratio $n_t$. For simplicity, a variable $M_N$ is defined as the conversion ratio normalized by transformer turns ratio,

$$M_N = \frac{V_{out}}{n_t V_g} \ . \tag{1}$$

Important waveforms of converter operation under operating steady-state conditions sufficient to provide ZVS of all devices are shown in Fig. 2. Input and output capacitances of the converter are assumed to be large enough such that $V_g$ and $V_{out}$ are well approximated as constant over a single switching period. To reduce control complexity, it is desired to operate with phase shift modulation at all operating points: $Q_1$ and $Q_4$ are switched simultaneously at near-50% duty cycle with a small dead time, and $Q_2$ and $Q_3$ are switched 180° out of phase. Similar drive waveforms are used for secondary side devices, with a controlled phase shift relative to the primary.

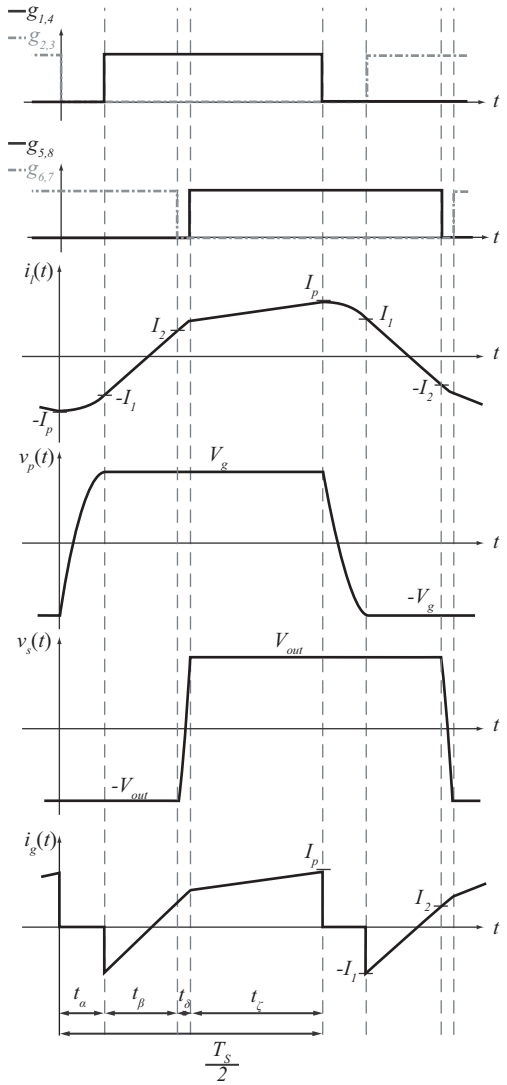


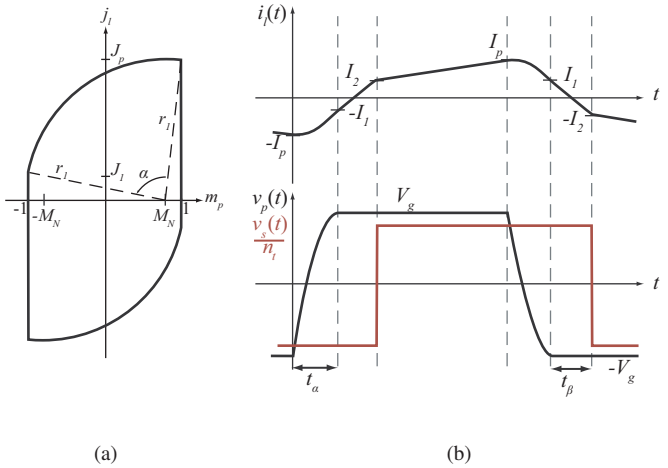

Fig. 2. Operational waveforms of DAB for the case where $V_{out} < n_t V_g$.

### A. Mode 1: Operation with $\beta > 0$ and primary ZVS

As shown in Fig. 2, the converter exhibits four intervals per half-period, referred to by their corresponding timing labels. In the $\alpha$-interval, a resonant energy transfer between $L_l$ and the output capacitance $C_p$ of the primary-side transistors causes zero-voltage switching on all primary devices. During the $\beta$-interval, the maximum available voltage, $V_g + V_{out}/n_t$, is applied to $L_l$ to quickly ramp the inductor current. The $\delta$-interval consists of a resonant transition between $C_s$ and $L_l$, which obtains ZVS of all secondary devices if $I_2$ is sufficiently large. Finally, the $\zeta$-interval is the main power delivery interval of the converter, in which the inductor current is slowly ramping according the voltage across $L_l$, which is non-zero if $M_N \neq 1$.

To simplify analysis of the converter the effect of the $\delta$-interval is ignored when solving the converter, which allows the Mode 1 solution to remain valid for both soft-and hard-switching operation of the secondary devices. Due to the high step-down ratio, it is expected that the high currents of the secondary side are capable of charging and discharging $C_s$ quickly; further, though the analytical ZVS condition is $I_2 > 0$, stray inductances on the high-current secondary are significant, causing ringing at $v_s$ and significantly affecting the switching losses of these transitions, as noted in [11], [12]. Though the interval is negligible in the solution of converter operating mode, the losses associated with the $\delta$-interval are not, and will be considered in Section III.

The primary resonant interval is analyzed by looking at the normalized $v_p - i_l$ state plane of Fig. 3. As in [18], normalization is employed with respect to $V_{base} = V_g$ and $I_{base} = V_g/R_0$, where ${R_0}^2 = L_l/C_p$ is the characteristic impedance of the primary-side resonant transition. The resulting normalized tank inductor current, $j_l = i_l/I_{base}$ and primary side voltage, $m_p = v_p/V_{base}$ are plotted over one full switching period in the state-plane diagram of Fig. 3, where the resonant angle $\alpha$ is the normalized primary dead time, $\alpha = t_\alpha \omega_0$, with $\omega_0 = 1/\sqrt{L_l C_p}$. This solution applies only




(a) (b)

Fig. 3. Operating waveforms of the DAB converter in Mode 1 as both normalized state plane (a) and corresponding time-domain waveforms (b).

under operating conditions illustrated by the waveforms shown in Fig. 2. That is, when $\beta$ and $J_1$ are positive, resulting in

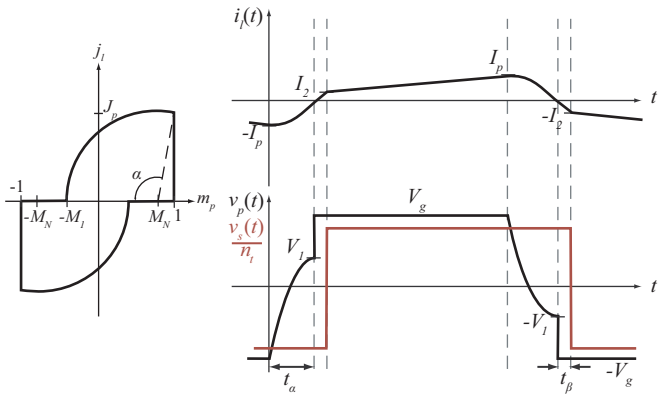
ZVS of all primary-side devices. The solution breaks down when the operating mode of the circuit changes, either due to insufficient current $J_p$ to obtain ZVS of primary devices, or due to $\beta$ decreasing below zero. These modes are analyzed in Sections B-D, with solution details for all four modes summarized in Appendix I.

### *B. Mode 2: Operation with $\beta > 0$ and hard-switched primary*

As output power decreases or output voltage increases, the current $I_p$ available to obtain ZVS of primary devices decreases accordingly. From the state plane diagram of Fig. 3, it can be seen that this boundary occurs when $J_p$ becomes so small that $r_1 < 1 + M_N$, resulting in a ZVS condition of operating mode 1

$$J_p > \sqrt{4M_N} \ . \tag{2}$$

which simplifies to the familiar $J_p > 2$ for $n_{ctrl} = n_t$, i.e. when ZVS is obtained with zero voltage across $L_l$. Below this boundary, the inductor current is reduced to zero before full ZVS can be achieved. If the primary devices are then switched directly at $i_l = 0$ to obtain minimal switching loss, the state plane of operation becomes modified as shown in Fig. 4. A new variable $M_1$ is defined, where $(1 - M_1)$ is the normalized voltage remaining on $V_p$ just before devices $Q_1$ and $Q_4$ are turned on. Thus, for $M_1 = 1$, soft-switching is obtained, and the converter operates at the boundary of this operating mode and Mode 1. Since $J_1 = 0$, $J_2 \geq 0$ in this mode, soft-switching is obtained on all secondary devices.




(a) (b)

Fig. 4. State plane and time-domain waveforms of the DAB converter in Mode 2, with hard switched primary devices. Because $M_1 < 1$, stored energy in $L_l$ is insufficient to achieve primary ZVS.

### *C. Mode 3: Operation with $\beta < 0$ and soft-switched primary*

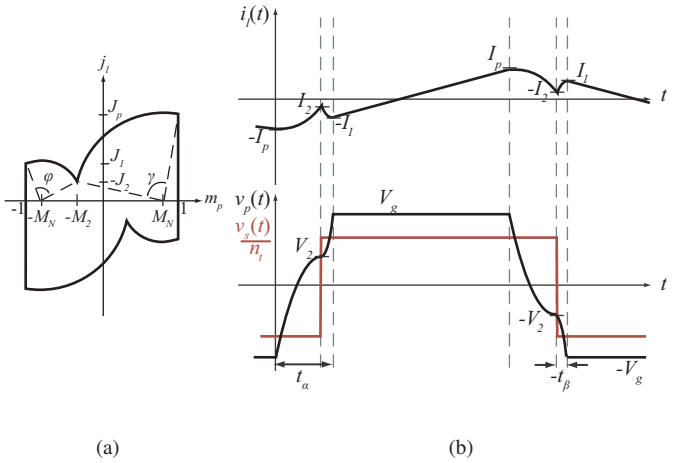
In Mode 3, the secondary devices are hard-switched during the dead time of the primary devices, resulting in two distinct resonant intervals whose combined effect is to achieve ZVS on the primary side devices. Because $t_\beta$ is defined as the time interval between the end of the primary dead time and beginning of secondary dead time, the converter can operate with $t_\beta < 0$ and still remain in positive power flow operation so long as $t_\alpha + t_\beta + t_\delta > 0$ remains true.

The state plane diagram for this mode of operation is shown in Fig. 5. To match boundary conditions with other operating modes, two new angles are defined as

$$\gamma = \alpha + \beta \ , \tag{3a}$$

$$\phi = -\beta \ . \tag{3b}$$

Additionally, the value $(1 - M_2)$ is the normalized absolute value of the voltage $v_p$ when the secondary side is switched. Switching the secondary during the primary resonant interval inverts $v_s$, altering the DC voltage biasing the resonant circuit formed by $L_l$ and $C_p$, as shown by the altered center of resonance in Fig. 5. Therefore, the secondary full bridge is commutated with previously conducting devices still having positive drain-to-source currents, causing hard-switching of secondary devices; this results in an output current which is now negative for a significant portion of the switching period. The resulting circulating current allows sufficient energy to be available for soft-switching primary devices below normal ZVS boundaries.



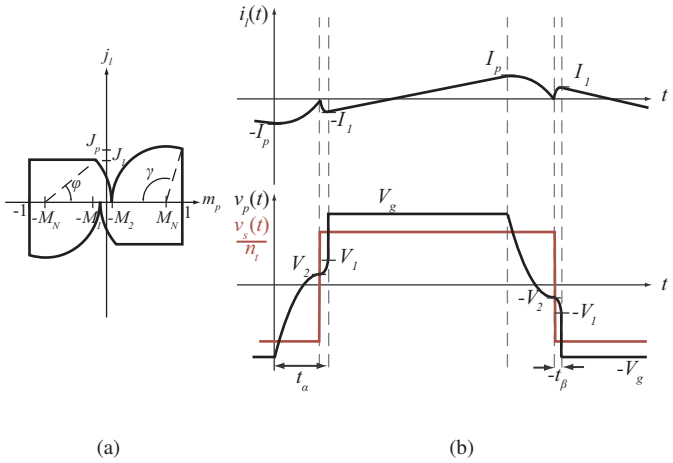

(a) (b)

Fig. 5. State plane and time-domain waveforms of the DAB converter in Mode 3 under $\beta < 0$ conditions. Because $J_2 < 0$, the converter loses secondary ZVS.

### *D. Mode 4: Operation with $\beta < 0$ and All Devices Hard Switched*

The final operating mode necessary to define converter operation consists of the area bounded by the $J_2 = 0$ boundary of Mode 2 and the $J_2 = 0$ boundary of Mode 3. The converter is solved by setting $J_2 = 0$ for the entire region and again introducing the variable $M_1$, at which point all primary transistors are switched with associated energy loss. By its nature, this region consists of some hard switching on all devices. The state plane diagram for this mode of operation is shown in Fig. 6.

Further operating modes beyond the four detailed here are possible, but are not addressed in this paper due to their necessary exhibition of either decreased efficiency or increased modulator complexity.




(a) (b)

Fig. 6. State plane and time-domain waveforms of the DAB converter under $\beta < 0$ conditions, with all devices hard switched.

## III. Converter Loss Modeling

The ramping of the current during the $\zeta$-interval provides opportunity for optimization of converter efficiency. By setting the output voltage less than the reflected input, $V_{out} < n_t V_g$, the converter is operated with larger $I_p$ for a given output power, allowing more energy to be stored in $L_l$ at the onset of the $\alpha$-interval. By increasing this energy, the ZVS range of the converter is extended, but higher RMS currents result. Because the intended application does not require strict output voltage regulation, $V_{out}$ can be adjusted to obtain maximum efficiency across all load conditions – decreased to provide additional energy for ZVS and increased to reduce RMS currents. In order to ascertain a method for adjusting $V_{out}$, as well as for selecting optimal dead times, a loss model is constructed for the DAB converter for the given application. To simplify analysis, losses are divided into conduction, switching, and core losses.

### A. Conduction Losses

In general, all devices in the DAB converter conduct RMS current equal to the input, output, tank, or reflected tank currents. Neglecting the need to reflect impedances through the transformer, this leaves only $i_{g\_rms}$, $i_{l\_rms}$, and $i_{o\_rms}$ to solve. However, in the case where the $\delta$-interval is neglected and transformer magnetizing current is negligibly small, the reflected output current is equal in magnitude to the tank current $i_l$ at all times, yielding

$$i_{o\_rms} = \frac{i_{l\_rms}}{n_t} \tag{4}$$

and leaving only $i_{g\_rms}$ and $i_{l\_rms}$ to solve. These values are solved independently for each operating mode by finding the RMS contribution of the piecewise linear and sinusoidal segments given from the analysis in the Section II, and summing them according to the method of [19]. On-resistances of all devices are included and copper losses of all magnetic windings are considered using finite element analysis to calculate AC resistances at the switching frequency and its harmonics [20].

### B. Switching Losses

Switching losses in the large step-down DAB converter consist of power loss due to the output capacitances of all devices, as well as significant losses due to stray inductances on the high-current secondary side. On the primary side, switching loss due to the output capacitance of the high voltage devices occur only in Modes 2 and 4, and consists at each switching transition of two devices turning on with a voltage $V_g\left(1-M_1\right)/2$ across them, and two devices being forcedly charged in a non-resonant manner from $V_g\left(1+M_1\right)/2$ to $V_g$. Using the analysis of [21], the nonlinear nature of $C_p$ is included by using a voltage-dependent capacitance $C_{oss,p}(v)$, whose defining function is taken from the datasheet of the primary-side device. Power loss attributed to hard-switching of $C_p$ is solved as:

$$P_{sw_p} = 4 f_s V_g \int_{V_g(1+M_1)/2}^{V_g} C_{oss,p}(v) dv \ , \tag{5}$$

Although the $\delta$-interval has little impact on the solution for converter waveforms, the switching loss associated with the high-current secondary is significant, and must be taken into account. To do so, state plane analysis is carried out for the resonance between $L_l$ and $C_s$ at the nominal operating point solved for in the previous section; this resonance now has new normalization parameters $V_{base} = V_{out}$ and $I_{base} = V_{base}/R_{0,s}$, ${R_{0,s}}^2 = {n_t}^2 L_l/C_s$. Additionally, the state plane is traversed counter-clockwise as opposed to the primary resonance. The $\delta$-interval is assumed to have a programmed-constant dead time equal to $t_{\delta 0}$, where resonance occurs between $C_s$ and $L_l$ if the tank current is positive during any portion of the interval. If the current remains negative during the entire interval, device antiparallel diodes will conduct for the duration of the interval, resulting in full hard switching of secondary device capacitances. Otherwise, $M_{1s}$ is calculated as the dual of $M_1$ on the primary side, and the switching losses due to $C_s$ are given by:

$$P_{sw_s} = 4 f_s V_{out} \int_{V_{out}(1+M_{1s})/2}^{V_{out}} C_{oss,s}(v) dv \ , \tag{6}$$

where the nonlinear MOSFET output capacitance is again considered.

Finally, due to the high currents present on the secondary, switching losses due to stray secondary inductances may be significant. Generally, these inductances arise due to MOSFET packaging and component layout. If the FETs are turned off with positive drain-to-source current, the energy stored in these stray inductances is left to ring out until dissipated, resulting in a power loss determined by the value of the stray inductance $L_x$ in series with each device and the current at the switching instance $I_2$

$$P_{sw_s l} = L_x \left(\frac{I_2}{n_t}\right)^2 2 f_s. \tag{7}$$

Not considered in this analysis are losses in the gate drive circuitry due to the charging and discharging of device gate charge nor losses in the control circuitry. These losses are constant across all operating points and are thus not subject to constant switching frequency optimization.

### C. Core Losses

Core losses are calculated according to the NSE/iGSE [22], [23] for both the tank inductance and transformer. Transformer voltage stresses are directly given by $v_s$. Voltage stress on $L_l$ is given by the difference between $v_p$ and $v_s$ reflected to the primary. However, both the primary-referenced leakage inductance of the transformer $L_{lk}$ and stray inductances $L_x$ of the secondary side cause potentially significant division of the voltage applied to the discrete component implementing the tank inductance. Thus, voltage stress on the inductor core is

$$v_l = \left(v_p - \frac{v_s}{n_t}\right) \frac{L_l}{L_l + L_{lk} + 2\frac{L_x}{n_t}} \tag{8}$$

and the waveform from (8) is used in the NSE calculation. The effect is less significant in the calculation of transformer stresses, so long as the magnetizing inductance is large in comparison to all other inductances.

## IV. Analysis of Optimal Efficiency Trajectory

In order to further examine converter efficiency across a range of operating modes and conditions, a prototype converter is used to obtain numerical results. Details of this converter are given in Table I, with derived analytical values in Table II and experimental results presented in Section VI. Of considerable interest is determining the boundaries of each operating mode from the converter solution. These regions are defined by the range of values $M_N$ and $P_{out}$ over which the converter solution remains internally consistent i.e. where the solved voltages, currents, and times are of value that do not violate the form of the state planes in the respective operating modes. These boundaries are solved iteratively, with the results shown in Fig. 7a, and example waveforms $i_l$ and $v_p$ corresponding to points A-E given in Fig. 7b. The converter is designed for a nominal output voltage of 12 V, which occurs when $V_{out} = n_t V_g$, or $M_N = 1$. In this case, without output voltage variation, the converter will cross from Mode 1 to Mode 2 at an output power of 110 W, with hard switching of the high voltage primary occurring at lower powers. However, if the output voltage can be dynamically decreased as the power falls below 110 W, ZVS can be maintained on all devices as low as 70 W by tracking the boundary between Mode 1 and Mode 2, and on primary devices to zero power if $M_N \geq 0.88$ is permitted, corresponding to an output voltage as low as 10.4 V. The extension of ZVS range comes at the cost of increased RMS current. By decreasing the output voltage, a higher average output current is needed to maintain output power; in addition, any move away from $M_N = 1$ causes increased ramping of inductor current during the $\zeta$-interval, resulting in a higher peak-to-average current ratio, though lower absolute RMS currents remain possible by increasing $M_N$ above unity. Thus, following directly the boundary between Mode 1 and Mode 2 for the power range 70 W $\leq P_{out} \leq$ 110 W maintains primary ZVS with the lowest RMS currents possible.

For $P_{out} > 110$ W, larger values of $M_N$ result in lower RMS currents, which help quell the dominance of conduction losses at high current. However, also of significance are the losses due to stray inductance $L_x$, and the inductor core losses, both of which increase at high power due to large phase shift and peak currents. Losses due to $L_x$, particularly, decrease at lower $M_N$, where the inductor current waveshape during the $\zeta$-interval allows smaller currents in $L_x$ when the secondary is switched.

Below $P_{out} = 50$ W, switching and core losses are dominant due to the low current levels. Mode 4 can be safely assumed to be a poor choice for low power operation, as significant switching losses are contributed from both primary and secondary bridges. Further, hard switching of the secondary is preferable to hard switching of the primary, as the high voltage input leads to greater losses from hard switching the primary than the secondary as long as

$$C_p > C_s \left(M_n n_t\right)^2 \tag{9}$$

which is true for most device combinations when $n_t$ is sufficiently small, as is the case in this application. Further, transformer voltage stresses are only marginally affected by converter operating point, and the lack of a large phase shift limits voltage stresses on the inductor. Thus, within Mode 3, efficiency is determined largely by constant losses, and output voltage has only a minor effect on determining losses.

To verify the efficiency analysis, losses in each operating mode are calculated to produce the efficiency contour plot of Fig. 8. The optimal efficiency trajectory across all output powers follows largely the expected trajectory. A second, proposed trajectory is also illustrated, which will be shown in the following section to have significant advantage in terms of controllability. For now, the proposed trajectory can be seen to be very near to optimal efficiency across the majority of the load range, with some deviation at low and high power. The breakdown of the losses on both trajectories is compared to experimental measurements with the prototype converter in Fig. 9.

TABLE I
Prototype Circuit Components

| | |
|---|---|
| Primary MOSFETs | FDMC2610 |
| Secondary MOSFETs | 2x IRFS6713 |
| Tank Inductance | LP02-500-1S |
| Transformer Core | 0L42020UG |
| Transformer Turns Ratio | 25:2 |

TABLE II
Prototype Circuit Parameters

| $C_p$ | $C_s$ | $L_l$† | $L_{lk}$ | $L_x$ | $n_t$ | $V_g$ | $P_{out}$ |
|---|---|---|---|---|---|---|---|
| 70 pF | 2 nF | 8 $\mu$H | 2 $\mu$H | 1.5 nH | 0.079 | 150 V | 20-120 W |

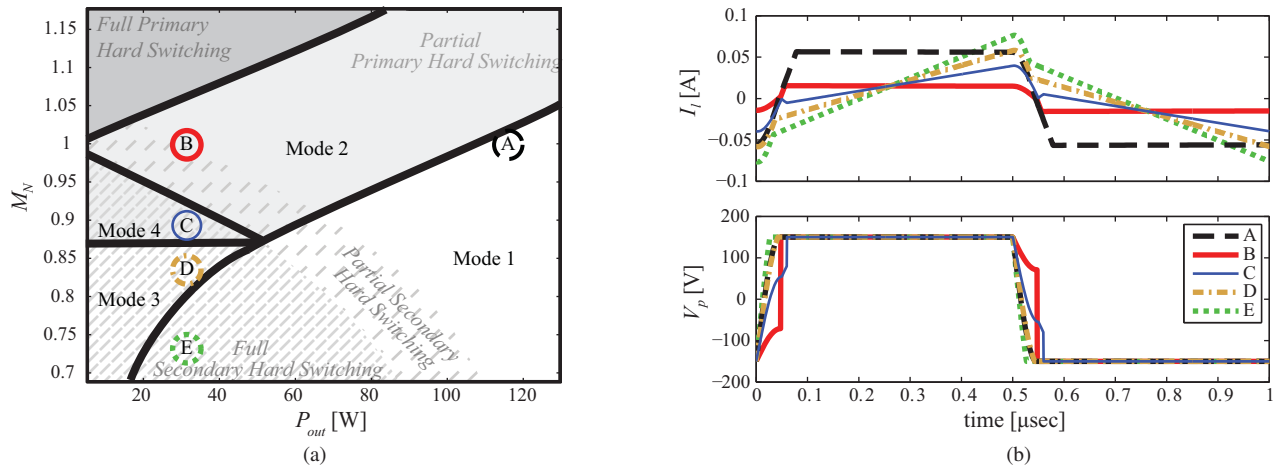
† reflected from 50 nH inductor on secondary-side, not including stray/leakage inductances

## V. Automatic Regulation of Converter Dead Times and Output Voltage

Fig. 10 shows the steady-state dead time $\alpha$, and total phase shift

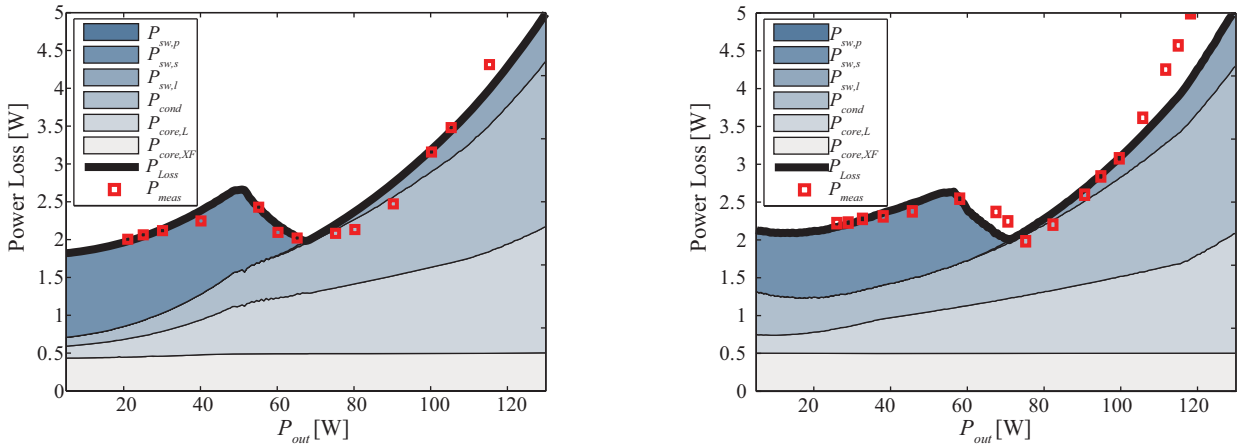
$$\Phi_{ab} = \alpha + \beta + \delta \ , \tag{10}$$

along with the normalized conversion ratio required to keep the converter on either the optimal or proposed trajectories




(a) (b)

Fig. 7. Operating mode locations for prototype converter are shown in (a). Shaded regions indicate primary hard switching, while the dashed region indicates hard switching of secondary devices. The points labeled A-E correspond to the time-domain waveforms of (b).




(a) (b)

Fig. 9. Analytical loss breakdown for both optimal (a) and proposed (b) trajectories. Note that $P_{sw,p}$ is not included, as neither trajectory contains points in which any hard switching of the primary devices is incurred.

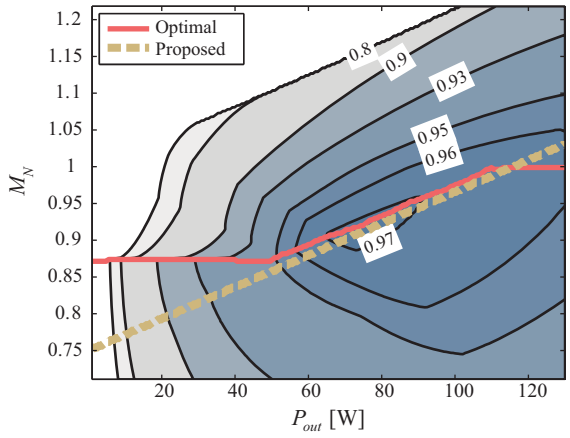



Fig. 8. Efficiency contours of DAB converter in Modes 1-4. The solid line indicates the highest efficiency trajectory.

of Fig. 8. In order to regulate the converter onto a given trajectory, an effective controller must adjust both $\alpha$ and $\Phi_{ab}$ to the specified values at each output power to obtain the correct conversion ratio. For the optimal controller, the values in Fig. 10a are both nonlinear and widely varying; in order to accurately track this trajectory, a controller is likely to require measurement of the output power and a lookup table to find the appropriate control parameters for each power. Conversely, the control parameters of Fig. 10b, for the proposed trajectory, are quite simple. On this trajectory, primary dead time $\alpha$ may be approximated as constant with only minimal additional detriment to converter efficiency in terms of diode conduction or minor partial hard switching or primary. Further, it can be seen that both the total phase shift $\Phi_{ab}$ and conversion ratio $M_N$ are very nearly linear functions of $P_{out}$; and are thus linear with one-another. Therefore, it is possible to construct a controller for this trajectory which does not require measuring the output power, but instead enforces a linear relationship between $\Phi_{ab}$ and $M_N$, of the form

$$M_N = K\Phi_{ab} + C \ . \tag{11}$$

For this purpose, the controller of Fig. 11 is employed. The

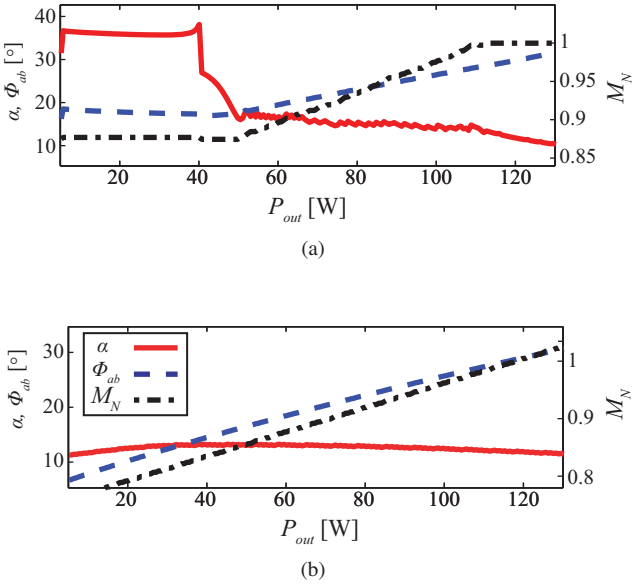



Fig. 10. Plot of control angles $\alpha$ and phase shift $(\alpha+\beta)$, in radians, plotted across a range of output powers for both the ideal efficiency trajectory (a) and proposed control trajectory (b) from Fig. 8.

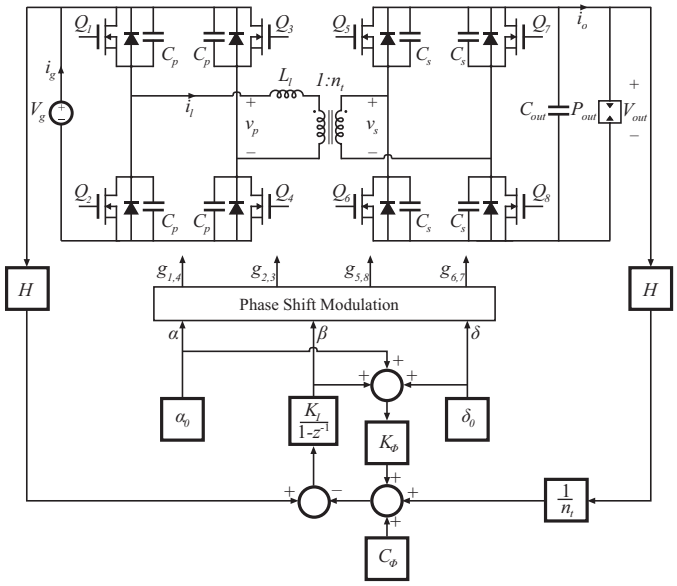



Fig. 11. Proposed control architecture for DAB converter. Linear feedback of $\Phi_{ab}$ is used to set conversion ratio $M_N$.

dead times $t_\alpha$ and $t_\delta$ are set to constants of value slightly less than one-quarter of the resonant period of $L_l$ and the respective primary and secondary capacitances. The phase shift is then set through $t_\beta$ by a feedback loop consisting of sensed values (through ADC gain $H$) for $V_g$ and $V_{out}$, whose difference is the input to an integral compensator. Around this integrator, a second loop adjusts the conversion ratio by adding or subtracting both a constant offset $C_\phi$ and an offset proportional to the total phase shift, $K_\phi\Phi_{ab}$. This additive approach allows the controller to be implemented digitally without the need for floating point division, so long as the $1/n_t$ gain on $V_{out}$ relative to $V_g$ can be implemented with resistive voltage dividers in the sensing circuitry. The controller implements a feedback which, through the use of an integral compensator, forces steady-state behavior

$$M_N = \left(\frac{K_\Phi}{HV_g}\right)\Phi_{ab} + \left(\frac{C_\Phi}{HV_g}+1\right) \quad , \qquad (12)$$

which appropriately matches the desired form from (11). Proper operation of the proposed controller, as well as verification of the loss model is given in Section VI.

## VI. Experimental Results

The converter depicted in Table I is constructed. Because gate drive losses are considered independent of the proposed optimization, eight DCH0105 isolated supplies are implemented on a separate PCB to provide power to gate drivers with very low common mode coupling. The converter power stage occupies roughly 3 in$^2$ on a dual-sided PCB, without the isolated supplies or control circuitry. The control loop of Fig. 11 is implemented using a Xilinx Virtex 4 FPGA to demonstrate controller operation. A delay line is implemented to achieve 3.2 GHz modulator resolution, and 12-bit, 15 MSPS ADCs are used to track input and output voltages. Values for $K_\phi$ and $C_\phi$ are tuned experimentally, and $K_I$ is set to stabilize the loop. The PWM and control circuitry occupy fewer than 5,000 gates on the Virtex 4, verifying that the simple control strategy could be implemented on a low-cost IC.

Conversion ratio and efficiency are measured experimentally using two calibrated Agilent 34411A multimeters to measure input current and output voltage, as well as two Fluke 45 multimeters for output current and input voltage, while converter waveforms are measured using a Tektronix DPO2014 oscilloscope with TCP0030 current probe. A comparison between the obtained experimental efficiencies and the predicted efficiencies for both the proposed closed-loop control method, and for manually optimized timing parameters and output voltage for maximum efficiency, is given in Fig. 12. Example waveforms and comparison between experimental and analytical state plane diagrams are given in Fig. 12 and 13, respectively, for a single operating point at 80 W output power and 97.4% efficiency. Note that, like the analysis, the efficiency results presented here do not include the gate drive losses, which are taken from a separate supply, and are estimated analytically to be 2.75 W for the given device combination.

## VII. Conclusion

This paper considers the analysis and control of an unregulated, high step-down, high frequency dual active bridge converter. Due to the combination of the high step-down conversion ratio, high switching frequency, and modest power level, the duration of the primary-side ZVS interval becomes significant when determining converter operation and is therefore analyzed across four different operating modes of the converter which encompass the full range of operating conditions and output powers. A loss model for the converter is developed, and a simple phase-shift modulation control strategy is proposed to operate the converter at near-optimal efficiency across all output power levels. Controller function

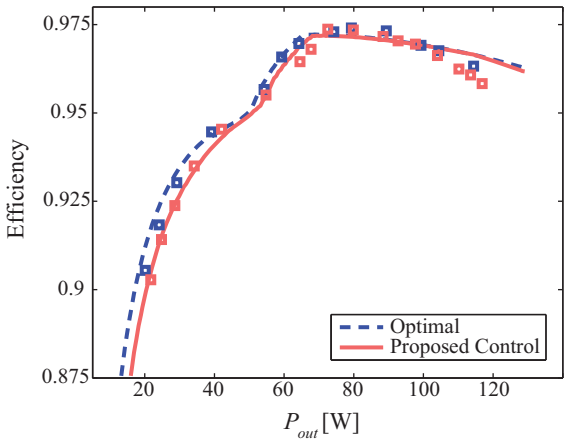



Fig. 12. Comparison of analytical solutions (lines) and experimental data (boxes) for optimal and proposed trajectories.

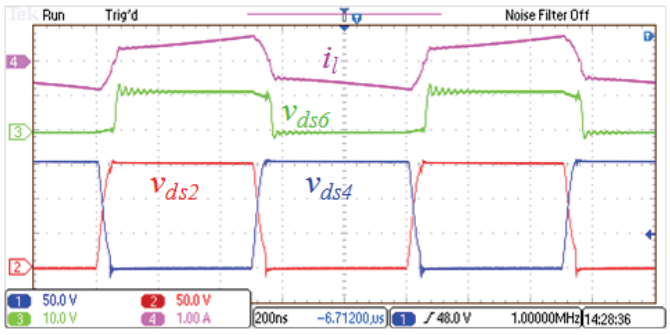



Fig. 13. Sample waveforms for DAB converter with proposed closed loop control for $P_{out} = 80$ W. The converter efficiency is 97.4%.

and loss model accuracy are verified experimentally with a 1 MHz, 150-to-12 V, 120 W converter which obtains 97.4% peak efficiency and is able to maintain greater than 90% efficiency above 20 W by continuously varying the output voltage in the range 10.4 V $< V_{out} <$ 12.5 V. This small varition in output voltage is expected to have minimal impact on the performance of latter conversion stages, but is a topic for future research.

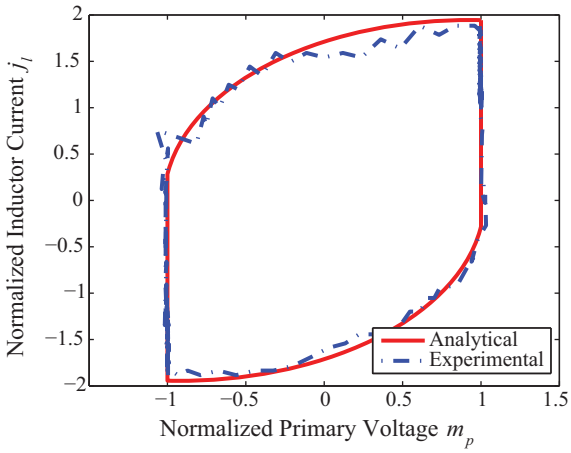



Fig. 14. Analytical and experimental results for primary state plane of prototype DAB operating at 80 W output power.

## Appendix A
## State Plane Converter Solution

### A. Solution in Mode 1

Fig. 3 is solved using geometric arguments to find the average output current. First, the radii $r_1$ are related to give

$$J_1 = \sqrt{{J_p}^2 - 4M_N} \ . \tag{13}$$

The conduction angle of the primary resonance is given by

$$\alpha = \cos^{-1}\left(1 - \frac{(J_p - J_1)^2 + 4}{2{J_p}^2 + 2\left(1 - M_n\right)^2}\right) \ . \tag{14}$$

Using this same normalization, the conduction angles for the $\beta$ and $\zeta$ intervals can be found from the time domain plots as

$$\beta = \frac{J_1 + J_2}{1 + M_N} \ , \tag{15a}$$

$$\zeta = \frac{J_p - J_2}{1 - M_N} \ . \tag{15b}$$

Further, the switching period is $T_s = 2(t_\alpha + t_\beta + t_\zeta)$ from Fig. 2 which, when normalized, becomes

$$\frac{\pi}{F} = \alpha + \beta + \delta \ , \tag{16}$$

with $F = f_s/f_0$. Finally, the averaged output current is solved from Fig. 2 by integrating the charge transferred to the output in each interval to obtain

$$J = \frac{\langle i_o \rangle}{I_{base}} = \frac{F}{n_t \pi}\left(2 + \frac{J_p + J_2}{2}\zeta + \frac{J_1 - J_2}{2}\beta \ .\right) \tag{17}$$

### B. Solution in Mode 2

In the Mode of Fig. 4, $J_1 = 0$ always and $M_1$ is found by examining the triangle formed between $r_1$ and the $m_p$ axis as

$$M_1 = \sqrt{{J_p}^2 + \left(1 - M_N\right)^2} - M_N \ . \tag{18}$$

Equations (15a), (15b), and (16) are unchanged, and the equations for $\alpha$ and $J$ become

$$\alpha = \cos^{-1}\left(1 - \frac{{J_p}^2 + (1 + M_1)^2}{2\left(M_1 - M_n\right)^2}\right) \ , \tag{19}$$

$$J = \frac{\langle i_o \rangle}{I_{base}} = \frac{F}{n_t \pi}\left(1 + M_1 + \frac{J_p + J_2}{2}\zeta - \frac{J_2}{2}\beta\right) \ . \tag{20}$$

### C. Solution in Mode 3

The converter solution as shown in Fig. 5 takes the form of a set of coupled equations derived from the conduction angles and from the two radii

$$\gamma = \cos^{-1}\left(1 - \frac{(J_p + J_2)^2 + (1 + M_2)^2}{2\left(1 - M_n\right)^2 + 2{J_p}^2}\right) \ , \tag{21a}$$

$$\phi = \cos^{-1}\left(1 - \frac{(J_1 + J_2)^2 + (1 - M_2)^2}{2\left(M_n - M_2\right)^2 + 2{J_2}^2}\right) \ , \tag{21b}$$

$${J_2}^2 = \left(1 - M_N\right)^2 + {J_p}^2 - \left(M_2 + M_N\right)^2 \ , \tag{21c}$$

$$J_1{}^2 = -\left(1 - M_N\right)^2 + J_2{}^2 + \left(M_N - M_2\right)^2 \ . \qquad (21d)$$

The equation for the $\zeta$ interval is slightly modified due to $I_2$ occurring before $I_1$ to get

$$\zeta = \frac{J_p + J_1}{1 - M_N} \ . \qquad (22)$$

Because $\beta < 0$, (16) becomes

$$\frac{\pi}{F} = \gamma + \phi + \zeta = \alpha + \zeta \ . \qquad (23)$$

Finally, the averaging of the output current yields

$$J = \frac{\langle i_o \rangle}{I_{base}} = \frac{F}{n_t \pi}\left(2M_2 + \frac{J_p - J_1}{2}\zeta\right) \ . \qquad (24)$$

### *D. Solution in Mode 4*

The converter solution in the mode of Fig. 6 follows closely that of Mode 3 with $J_2 = 0$ and notable exceptions

$$\phi = \cos^{-1}\left(1 - \frac{J_1{}^2 + \left(M_1 - M_2\right)^2}{2\left(M_n - M_2\right)^2}\right) \ , \qquad (25)$$

$$J = \frac{\langle i_o \rangle}{I_{base}} = \frac{F}{n_t \pi}\left(2M_2 + 1 - M_1 + \frac{J_p - J_1}{2}\zeta\right) \ . \qquad (26)$$

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**Daniel Costinett** (S'10) received the B.S. and M.S. degrees in electrical engineering from the University of Colorado, Boulder, in 2011. Currently, he is working toward the Ph.D. degree in power electronics from the Department of Electrical, Computer, and Energy Engineering, Colorado Power Electronics Center, University of Colorado, Boulder, while assisting with course development at the Department of Electrical and Computer Engineering at Utah State University in Logan, UT. His current research interests include high frequency and soft switching converter design, RF energy harvesting, mixed signal IC design for power electronics applications, and power electronics design for electric vehicles.

**Regan Zane** (SM'07) received the Ph.D. degree in electrical engineering from the University of Colorado, Boulder, in 1999. He is currently a USTAR Professor in the Department of Electrical and Computer Engineering at Utah State University in Logan, UT. Prior to joining USU, Dr. Zane was a faculty member at the University of Colorado-Boulder, Colorado Power Electronics Center, CoPEC, 2001 to 2012, and research engineer at GE Global Research Center, Niskayuna, NY, 1999 - 2001. He has recent and ongoing projects in bi-directional converters for dc and ac micro-grids, high step-down power converters for dc distribution systems such as high efficiency data centers, improved battery management systems (BMS) for electric vehicles, LED drivers for lighting systems and low power energy harvesting for wireless sensors. Dr. Zane received the NSF Career Award in 2004 for his work in energy efficient lighting systems, the 2005 IEEE Microwave Best Paper Prize for his work on recycling microwave energy, the 2007 and 2009 IEEE Power Electronics Society Transactions Prize Letter Awards for his work on modeling of digital control of power converters and the 2008 IEEE Power Electronics Society Richard M. Bass Outstanding Young Power Electronics Engineer Award. He received the 2006 Inventor of the Year, 2006 Provost Faculty Achievement, 2008 John and Mercedes Peebles Innovation in Teaching, and the 2011 Holland Teaching Awards from the University of Colorado. He currently serves as Associate Editor for the IEEE Transactions on Power Electronics, Letters, and as the Publicity Chair for the IEEE Power Electronics Society.

**Dragan Maksimovic** (M'89-SM'04) received the B.S. and M.S. degrees in electrical engineering from the University of Belgrade, Yugoslavia, in 1984 and 1986, respectively, and the Ph.D. degree from the California Institute of Technology, Pasadena, in 1989. From 1989 to 1992, he was with the University of Belgrade, Serbia (Yugoslavia). Since 1992, he has been with the Department of Electrical, Computer and Energy Engineering, University of Colorado, Boulder, where he is currently a Professor and Director of the Colorado Power Electronics Center (CoPEC). His current research interests include mixed-signal integrated circuit design for control of power electronics, digital control techniques, as well as energy efficiency and renewable energy applications of power electronics. Prof. Maksimovic has co-authored over 200 publications and the textbook Fundamentals of Power Electronics. He received the 1997 NSF CAREER Award, the IEEE Power Electronics Society Transactions Prize Paper Award in 1997, the IEEE Power Electronics Society Prize Letter Awards in 2009 and 2010, the Holland Excellence in Teaching Awards in 2004 and 2011, the University of Colorado Inventor of the Year Award in 2006, and the IEEE PELS Modeling and Control Technical Achievement Award for 2012.