

Ensuring Clean Power for RF and Digital Applications

Tom Boehler and Steven Sandler
AEi Systems
Los Angeles, CA, 90045; 310-216-1144
TomBoehler@aeng.com
Steve@aeng.com

ABSTRACT

Power supply designs are often overlooked as part of a high-frequency electronic system. A wide range of approaches are used and many of these power designs simply don't work as well as they should. These power supply designs perform poorly for a number of technical reasons, and it may be helpful examine these issues. Key performance requirements, such as stability, regulation, ripple, and headroom are often overlooked and not properly met. To ensure these performance criteria are addressed, design engineers require more complete data sheets, appropriate computer-aided simulation models, and suitable test equipment.

In many designs, the same power supply, usually consisting of a converter and various linear regulators and POLs, is used to feed various RF and digital loads. Increasing device speeds can cause transient edges of load currents are becoming more difficult to ignore reaching switching speeds of hundreds of picoseconds. Regulators have also increased in speed, reaching bandwidths up to 10 MHz which this makes a standard 2-MHz network analyzer under-equipped to measure voltage regulators. As a result, power electronics engineers may find themselves struggling with RF engineering issues. This paper is aimed at identifying these issues through a mix of new and existing power supply measurement techniques.

BACKGROUND AND OBJECTIVES

Power supply design is an often overlooked area in modern high speed digital and RF systems. The performance of a voltage regulator (both switching and linear) is often not analyzed or optimized for its specific application. IC manufacturers' datasheets typically provide example circuit topologies and part values that are more often than not simply "copy and pasted" into a system without regard for the context of the sample topology.

In many designs, one power supply (consisting of a converter and many regulators) is used to feed a wide range of loads, which are often digital or RF in nature (see Figure 1). Devices in these circuits have become so fast that the transient edges of the load currents are much more of a problem than they used to be. In addition to the high load current slew rates, regulators have also become faster, meaning the standard 2-MHz network analyzer is no longer adequate for performing measurements. Today's regulators often have bandwidths in the 5- to 10-MHz region. As a result of these issues, the power electronics engineer is faced with much difficulty when attempting to solve RF engineering issues.

A typical distributed power system is heavily reliant on linear regulators and filtering to clean up DC-DC converter ripple and noise. These methods of reducing noise, however, can cause problems such as poor phase margin, which can lead to a significant degradation in RF and digital performance.

Often either RF or systems engineers are constructing distributed architecture power systems. A common tactic is to simply use off-the-shelf converters or designs taken from previous programs. Even the most experienced RF or systems engineers can be under-equipped and not familiar with the specific pitfalls that

come with the complex details of distributed power systems.

It is generally believed that Low Dropout Regulators (LDOs) and linear regulators can simply be dropped into the power supply and distribution system, but there is a lack of understanding in regards to the relationship between these devices and the unique loading that is applied to them. For example, in space applications, large value capacitors (typically tantalum capacitors) are used to reject single event upsets (SEUs), while RF and digital ICs require large quantities of smaller value ceramic capacitors for decoupling.

The design process of the power system begins with classifying all output voltage needs, current needs, and other functionality such as under/over-voltage protection and housekeeping circuitry. In space applications the most common method for achieving the multiple output voltages is to use a multi-winding flyback or forward transformer with one winding dedicated to regulation, with post-regulation being achieved on all other windings via LDOs or linear regulators.

The optimum approach is to perform a trade study to observe the advantages and disadvantages with various converter topologies. Forward converters are good for high-power designs and generally have lower output ripple, but suffer at lower power levels. Flyback converters on the other hand are optimal for low-power applications, but suffer from higher output ripple voltages and currents and can have severe cross-regulation and stability issues.¹

The following sections of this paper address the testing methods that should be used to find issues in power supply designs. The consequences of a poorly designed power supply system are also discussed.

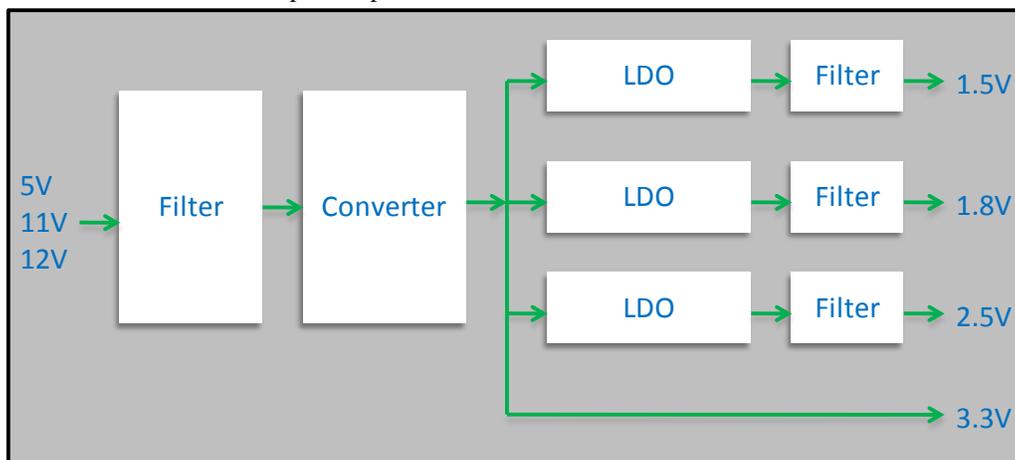


Figure 1: Distributed Power System Architecture

EQUIPMENT

It is important to understand power measurement, and to use the correct equipment to analyze the parameters of a power supply, to ensure clean power for the application. In Figure 2 below, the power supply under test is shown in the center with the important measurement characteristics listed around it.

The measurements shown in blue are the most common measurements made on a power system and can be measured with a simple oscilloscope or multimeter. The orange areas represent the metrics that are often overlooked, yet these are the ones that truly define a power supply's performance, especially for high speed applications. These measurements require higher fidelity test equipment to measure, with almost all metrics requiring a Frequency Network Analyzer or Vector Network analyzer to measure properly.

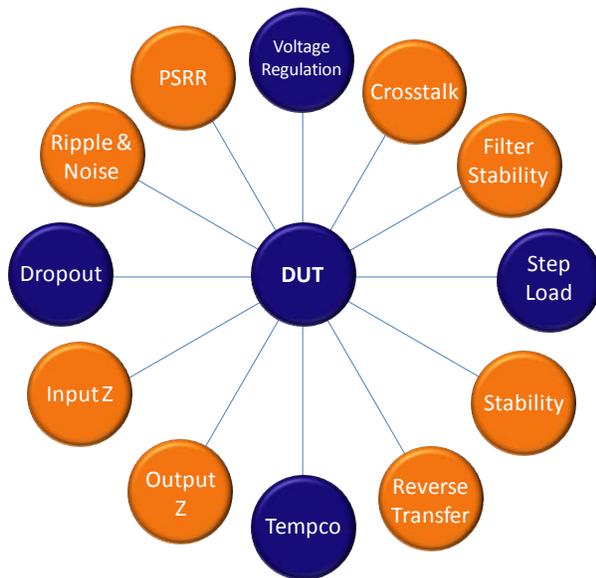


Figure 2: Power Supply Measurements

The network analyzer, sometimes referred to as a Frequency Response Analyzer (FRA) or Vector Network Analyzer (VNA), is a common piece of equipment in most electronics labs. Analyzers are used for a variety of tasks including stability analysis, component characterization and of course frequency response measurements. They can vary in features, but regardless of the analyzer being used, the analyzer oscillator signal must be injected into the circuit being tested in order for a measurement to be made.

Signal Injectors, also known as test adapters or interface adapters, are used to inject or transmit signals into and from various circuits so that the circuit's characteristics can be tested. Tests include Bode plot

control loop analysis, circuit and component impedance measurements and conducted susceptibility measurements, to name just a few.

The quality of the test signal injector, or test adapter, and the injection method can have a direct impact on the test results. For example, it is often the case that we see "hobby store" transformers used to inject signals into the loops of power supplies. In this case, the results are likely to be distorted due to the poor frequency response and impedance matching of the transformer.

It is critical to understand the bandwidth limitations and the impedance of the test interface adapter, as well as the impact of the injection signal magnitude on the measurement, in order to achieve accurate and repeatable test results.

Different tests require different injectors. In some cases, more than one injector will be required to complete one type of test. The details can be found in the next sections for the following tests:

- Bode Plots
- Output Impedance
- Step Load
- Power Supply Rejection Ratio (PSRR)

These tests are chosen, as they are considered to be important in power supply design--the quality of these characteristics can heavily impact high-speed system performance.

BODE PLOTS (STABILITY)

Bode plots are by far the most common method of measuring stability and provide a bandwidth, phase margin, and gain margin of a DC-DC converter or voltage regulator. These are shown in Figure 3.

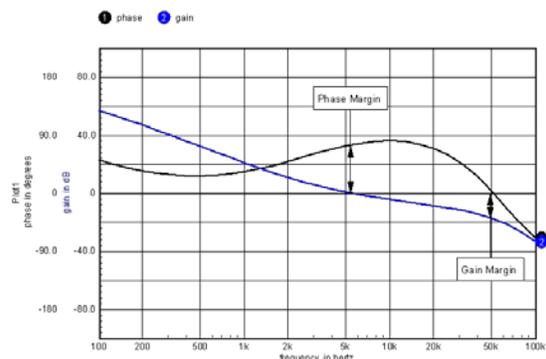


Figure 3: Typical Bode Plot

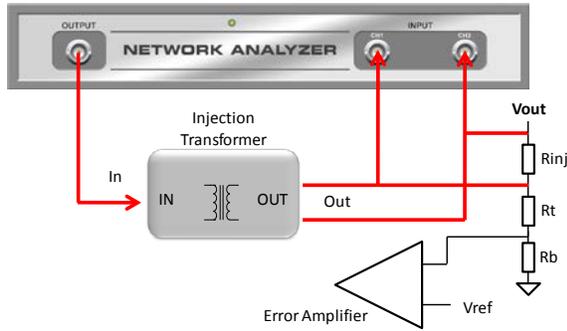


Figure 4: Connection Diagram for Making a Bode Plot Measurement

Figure 3 shows that the bandwidth can be measured by observing the frequency where the gain crosses the zero axis. The distance from this point to the point on the phase curve measures the phase margin of the system, and at the point in frequency where the phase crosses zero, the distance from the zero axis to the gain curve is the gain margin of the system.

This is standard for defining the stability criteria of a power supply and plays a large role in how the other characteristics of the power supply behave. This will be shown in later sections.

Figure 4 shows the appropriate way to inject a signal and measure the Bode response of the system. A small AC signal is injected from the network analyzer (isolated by a 1:1 injection transformer) across a small value resistor, typically 5 to 20 Ohms. This opens the control to the AC response while maintaining DC feedback. The size of the injection signal must be kept small as larger signal sizes can overdrive the signal and generate erroneous Bode plot results.²

Not all injection transformers are capable of the small signal wide bandwidth measurement required for a good Bode plot. While many users believe that audio and video transformers can be used, it is untrue. Many users believe the transformer is not a part of the measurement, again this is untrue. A high frequency transformer must be used in high speed applications as the bandwidths of regulators used to power RF and digital systems get higher and higher.

OUTPUT IMPEDANCE

Sometimes a Bode plot cannot be measured directly, yet somehow we must be able to measure the stability of the power system. Examples of this include three terminal regulators or hybrids where the control loop is not exposed, or integrated production hardware where it is not possible to break into the control loop to inject the test signal. In these cases the stability may still be determined by testing or simulating the circuit's output

impedance. The connection diagram for measuring output impedance is shown in Figure 5.

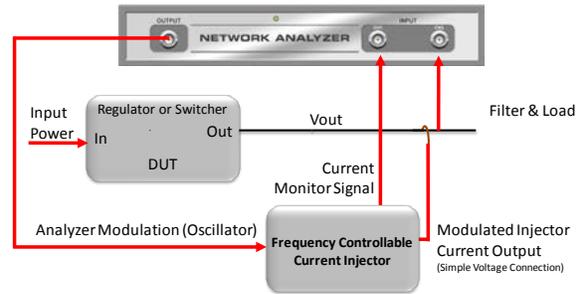


Figure 5: Connection Diagram for Making an Output Impedance Measurement

Both bandwidth and phase margin can be determined from output impedance by observing peaking in the group delay of the impedance.³

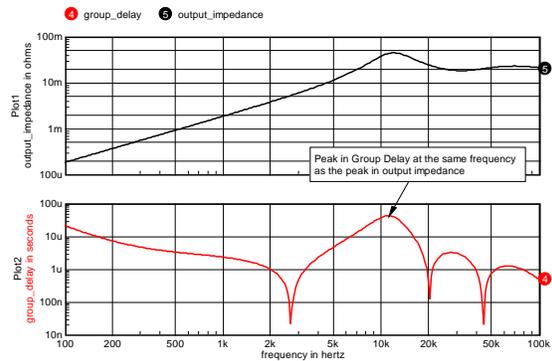


Figure 6: Typical Output Impedance Plot

Group delay is the time distortion between two signals (the two signals in this case being the perturbed load current and resulting voltage response) and is obtained by differentiating the phase difference between the current and the voltage. Group delay is defined in Equation 1 as:

$$T_g = \frac{d\phi}{d\omega} \quad (1)$$

Each peak in the group delay represents a unique Quality Factor or "Q" and these peaks can present themselves as voltage oscillations with dynamic load currents at the frequency of the peak. The higher the Q of each peak, the more susceptible the circuit is to oscillations at that peak's frequency. Q is defined in Equation 2 as:

$$Q = T_g \cdot \text{Freq} \cdot \pi \quad (2)$$

Tg is the group delay value at a given peak on the curve and Freq is the frequency of the peak. From this Q value, we can compute the exact phase margin value as shown in Equation 3.⁴

$$PM := \text{atan} \left(\frac{\sqrt{1 + 4Q^4}}{2Q^4} \right) \cdot \frac{180}{\pi} \quad (3)$$

A sample measurement of this phase margin extraction from an output impedance measurement is shown below in Figure 7. Some network analyzers, such as the Omicron-Lab Bode 100 Vector Network Analyzer have these equations built in to make the phase margin extraction a simple cursor measurement.

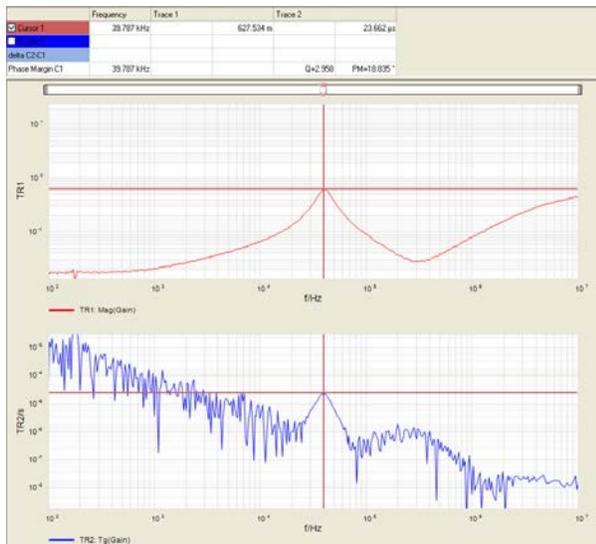


Figure 7: Non-Invasive Phase Margin Measurement Using Output Impedance

This measurement can be made in-system while the unit is performing under normal operation. This gives an accurate depiction of the real-life stability performance of a power supply or voltage regulator without the need to alter the system to make a stability measurement.

STEP LOAD

Newer point-of-load converters, RF amplifiers and FPGAs have the capability of drawing extremely high currents from the power supply in a very short period of time. Some FPGAs can draw up to 10A in under 1nS when changing operating modes from stand-by to full operation in a single clock cycle. Any parasitic or real inductance on the part or the board can cause voltage spikes that could potentially harm the device. The stability of the regulator will also dictate the amount of ringing observed

Small-signal step load responses are used to verify the stability of a regulator, as opposed to large-signal step load responses, since the former can be directly compared to a Bode plot of the open loop response or output impedance measurements, while large signal responses can easily impact the circuit response due to circuit nonlinearities.

A step load measurement can also be performed in-system while the unit is performing under normal operation. The measurement is similar to an output impedance measurement; however a time domain graph can be obtained, which is generally more easily understood when under review. The method for load stepping a power supply is shown in Figure 8.

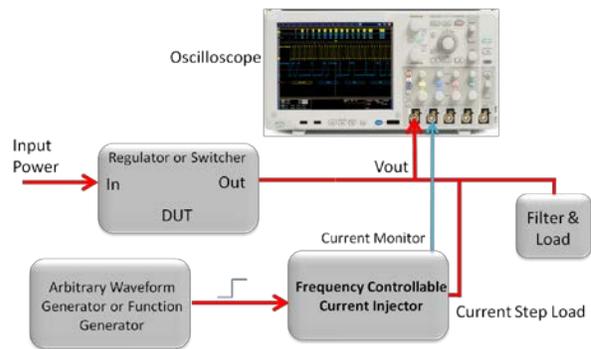


Figure 8: Connection Diagram for Making a Step Load Measurement

Using a small-signal load step on the order of 20mA can provide enough perturbation to provide a verification of the stability of the supply.

The edge speed of the current pulse is important, as it should replicate the actual high-speed load as closely as possible. The current injector used to make this measurement is a Picotest J2111A and produces current rise and fall times of 20nS. A sample measurement of a linear regulator load step is shown in Figure 9.



Figure 9: Small-Signal Load Step and Voltage Response

PSRR

PSRR or Power Supply Rejection Ratio is the measure of the conducted susceptibility of a regulator. In short, this is a measure of how much of an AC signal is attenuated from the input to the output.

This is a particularly important aspect in high speed design as this is the measure of how well the post-regulators in the distributed architecture system will filter ripple, noise, and transients from the switching converter or bus voltage. The proper way to measure PSRR is shown in Figure 10.

To properly inject an AC signal onto the DC input line of the voltage regulator, a Picotest J2120A Solid-State Line Injector is used. Many application notes have stated using an injection transformer is an appropriate way to inject AC into the system, however, performance injection transformers use very high permeability specially annealed core material for high inductance. The typical high-quality injection transformer cannot operate with more than 5mA-10mA of DC current. Higher currents will provide incorrect results, but also can permanently bias the core, rendering the transformer useless

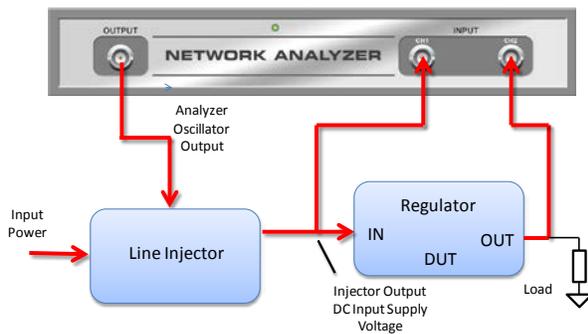


Figure 10: PSRR vs. Phase Margin

PSRR is typically very high at low frequencies and falls off rapidly as frequency is increased. PSRR is heavily dependent on the stability of the system and can degrade very quickly as regulator phase margin goes down as shown in Figure 11.

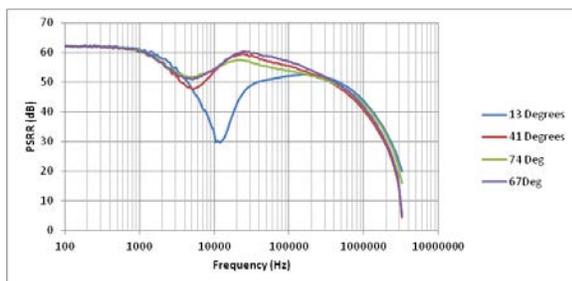


Figure 11: PSRR vs. Phase Margin

The sharp “dip” in PSRR due to lower phase margins is the most critical factor in high speed systems. The frequency at which the dip occurs is near the bandwidth of the regulator which typically coincides with switching frequencies, or harmonics of switching frequencies of the switching converter feeding the voltage post-regulators. This can introduce noise into the RF and digital components as the filter that is supposed to come from the regulators may not be there due to poor performance.

CONCLUSION – WHY DO WE CARE?

Stability has been measured using various methods, and a PSRR has been linked to the stability performance observed in testing. So what does this actually mean to a high-speed system? Is it relevant to an RF or digital engineer and should they care?

The answer is of course yes. It is even easily quantifiable by looking at how a power system with good stability and one with poor stability impact the performance of a digital clock.

If we power a 20MHz high-speed digital clock with a linear regulator and vary the stability, we can observe the clock jitter which is directly related to how clean and accurate timing signals behave.

Looking at the regulator powering the clock with 70 degrees of phase margin, we can see the clock jitter measures about 4.9pS as shown in Figure 12.

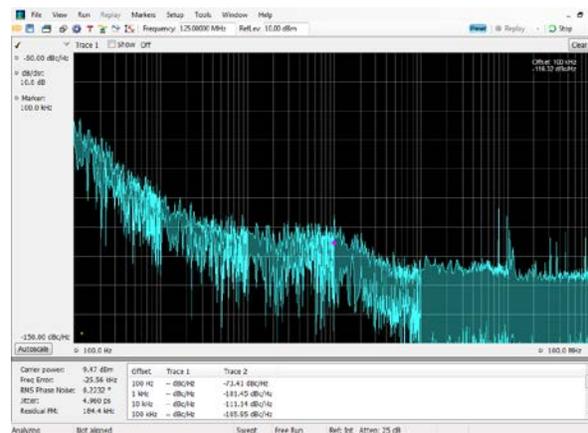


Figure 12: Clock Jitter When Powered by a Regulator with 70 Degrees of Phase Margin

If we power this same clock with the same linear regulator not optimized for stability, we can see the harsh degradation in clock performance. The same linear regulator is used but only has 15 degrees of phase margin. The clock jitter now measures approximately 281pS of jitter as shown in Figure 13.

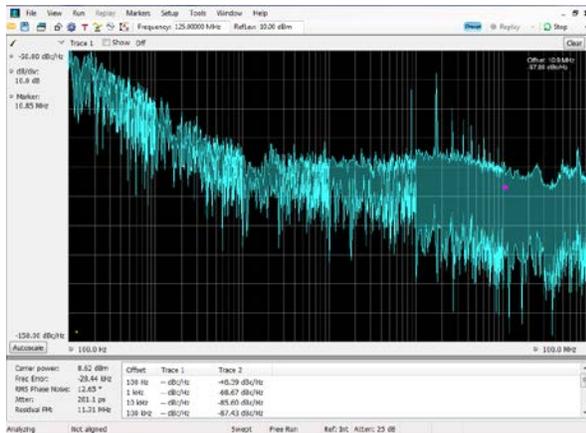


Figure 13: Clock Jitter When Powered by a Regulator with 15 Degrees of Phase Margin

Nearly two orders of magnitude is an incredible difference in clock performance, due simply to the regulator stability not being optimized.

This degradation in performance will affect the noise in RF systems as well as digital system performance characteristics such as Signal to Noise Ratio (SNR) and Bit Error Rate (BER).

If a power system is not carefully designed, analyzed, and fully tested, the payload of the entire system may not function at its full potential. Making your power systems cleaner in terms of performance and stability can be seen as a free performance boost to digital and RF engineers.

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