Radiation Hardened by Design 8 bit RISC with Dual I2C Bus Support and SPI for External NVM Support

Sasan Ardalan, Donald Elkins, Will Burke
Micro-RDC
8102 Menaul Blvd NE, Albuquerque, NM, 87110; 505-294-1962
sasan.ardalan@micro-rdc.com

Richard S. Marquez
Air Force Research Laboratory, Space Vehicles Directorate

ABSTRACT

The Mini-PnP 3x3 mm ASIC has been designed with Radiation Hardened by Design (RHBD) techniques using the IBM9LP CMOS process. The chip includes a high performance 8 bit PIC based RISC with 4Kx14 EDAC protected on chip Instruction RAM and two banks of registers supporting 192 bytes each. The registers are implemented using temporal latch technology and are SEU immune. The architecture supports two master inter-integrated circuit (I2C) buses where one can be configured as an I2C slave. The chip implements a SPI Master core. The cores are integrated with the RISC processor using a Wishbone Bus Crossbar switch. Mini-PnP ASIC supports bootup from an external SPI based Non Volatile Memory (NVM). The reading of the "eXtensible Transducer Electronic Datasheet" (xTEDS) from the external SPI NVM is also supported for Plug and Play applications. The ASIC Mini-PnP Silicon has been successfully tested with the design clock of 50 MHz. In this paper, the power consumption of the core power versus clock scaling is presented. The goal of the multi-chip module (MCM) implementation of Mini-PnP is to reduce the system size to around 15x15mm with integrated ASIC Mini-PnP, I2C driver circuits, SPI NVM (128Kbytes), and multiplexing to support external programming of the SPI NVM. A Chip on Board (COB) solution will be presented.

INTRODUCTION

The Space Plug-and-Play Avionics (SPA) approach is part of the Air Force Research Laboratory's (AFRL) efforts to streamline satellite design, development, assembly and testing [1-4]. The implementation of SPA is defined in a series of draft standards maintained by AFRL. SPA is designed as a system of systems using the Plug-and-Play (PnP) principle to interconnect devices across a common network can be implemented over a variety of physical layers. In the case of SPA-1 the Physical Interface is the I2C bus. The Structured ASIC Mini-PnP is a SPA-1 compatible device and supports the xTEDS that has been adopted to facilitate a "driver-less" form of plug-and-play. Micro-RDC has also taped out and successfully tested the Silicon for a spacewire based (SPA-S) and USB based (SPA-U) Structured ASIC (SASIC) appliqué sensor interface module (ASIM) that was described in [5]. The SASIC design using the IBM 90nm 9LP CMOS process is based on RHBD techniques. This includes the use of temporal latch technology for single event upsets (SEU) mitigation [6-7]. All registers and flops in Mini-PnP SASIC use the temporal latch technology making the chip immune to SEU in the harshest environments in space. In fact, a SASIC chip is being planned to scrub FPGA's in which case the chip itself is immune to SEU [6]. The Mini-PnP SASIC is a System on a Chip (SOC) based on a high performance 8 bit RISC and can be used in a wide variety of space borne applications.

MINI-PNP BLOCK DIAGRAM AND ARCHITECTURE

SASIC Mini-PnP is a 3x3, 90nm CMOS Structured ASIC SPA-1 ASIM designed for high performance processing using an 8 bit RISC with 14 bit instruction code size (modeled based on the PIC 16F74 PIC). The RISC Core is based on a Micro-RDC enhanced version of the Open Cores 16F84A PIC RTL. Mini-PnP SASIC supports two I2C busses for interfacing to sensors and peripherals. The I2C bus also performs the networking function between multiple SASIC Mini-PnP's. The chip supports reloading the on chip EDAC protected 4Kx14 Program RAM from an external SPI NVM. The reloading supports on-demand scrubbing of the on chip 4Kx14 Program RAM using a single reload signal (triggered on the rising edge).

For efficient programming, Mini-PnP SASIC supports interrupts on both I2C busses and from an on-chip Watchdog Timer.

The chip uses RHBD techniques and is taped out using the IBM 90nm 9LP CMOS process. The radiation hardness of the chip is as follows:

- Total Ionizing Dose: Within specifications after exposure to greater than 1Mrad (Si).
- Single Event Latch Up: Latchup immune to 100 MeV-cm2/mg
- SRAM Error Rate: Supports Scrubbing Program SRAM to obtain desired Error Rates
- Single Event Transient: Implements the temporal latch based shift register to mitigate transient pulse widths of up to 1 ns.

Figure 1 shows the block diagram of SASIC Mini-PnP. The clock frequency is 50 MHz. The enhanced PIC core is based on the OpenCores 16F84a RTL. It has been enhanced to support up to 8K of program RAM and a read strobe to support the Wishbone Cross Bar Switch. SASIC Mini-PnP includes two I2C interfaces based on the Open Cores I2C Core. The SPI Core is also from Open Cores and interfaces to the RISC processor through the Wishbone Crossbar Switch. The Watch Dog Timer Core is also from Open Cores and interfaces to the RISC processor via the Wishbone crossbar switch. SASIC Mini-PnP supports 8 general purpose input/output (GPIO) pins that can be individually programmed. The chip supports bootup from an external EEPROM via a SPI interface. An on-chip SPI Master block copies code from the EEPROM to Program RAM (4096x14).

The RISC processor can execute code from the program RAM or on chip ROM. The taped out chip also supports an external ROM for Post Silicon Verification. The xTEDS data sheet can be read from the EEPROM via the Open Cores SPI Master and sent back via the I2C interface to any other host. For Post Silicon Verification purposes, SASIC Mini-PnP includes a UART that operates at 38400bps with a 50 MHz clock.

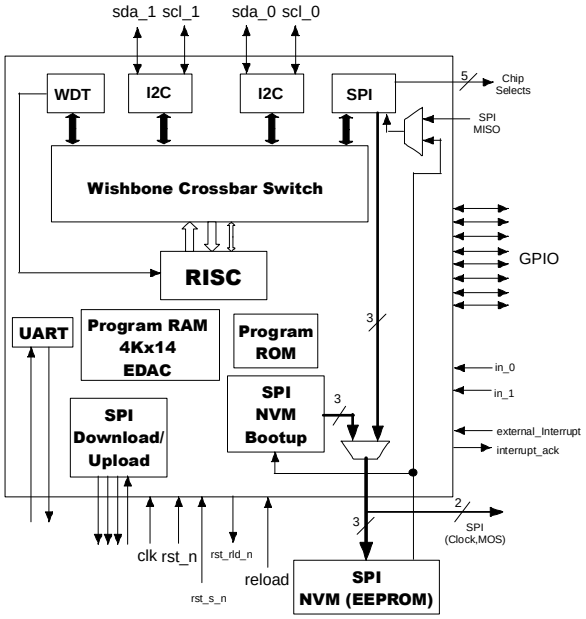

Figure 1. SASIC Mini-PnP Block Diagram

MEMORY SUBSYSTEM AND EEPROM BOOTUP

In Figure 2, the block diagram for downloading program code via a SPI interface and for loading the program code from the EEPROM is shown. Also shown in Figure 2, is the multiplexing of the SPI signals from the on chip SPI NVM Master Controller (developed by Micro-RDC) and the Open Cores SPI Master (interfaced to the RISC Processor with the Wishbone Crossbar Switch).

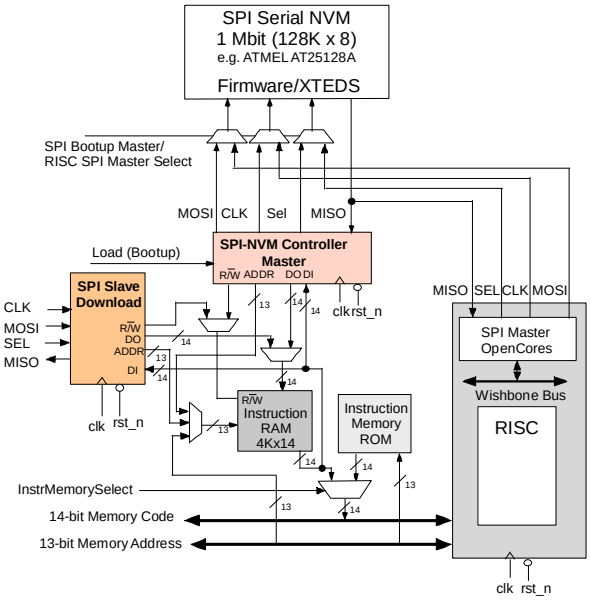

Figure 2. Memory Sub System with EEPROM Bootup/SPI Download

Figure 2 also shows the selection of program execution from either the program RAM implemented using on chip distributed RAM or ROM (which was mapped to gates). The RISC has a 14 bit program code word size. The EEPROM supports 8 bit bytes. The 14 bit code is stored as two bytes in the EEPROM. During loading from the EEPROM (bootup) the code is assembled into a 14 bit code from two bytes and stored in program RAM.

The multiplexing of the SPI interface into the EEPROM allows for firmware updates to be programmed into the EEPROM using the RISC. It also provides for reading the xTEDS from the EEPROM by the RISC.

Figure 2 also shows the capability for downloading program code from an external SPI Master (such as a USB/GPIO SPI interface) to the Mini-PnP SASIC program RAM using the SPI Slave. The code is read from a special file that is created from the Intel Checksum File of the program. The file (*spi_ram.dat*) stores an address and the two bytes representing the 14 bit code per line. The USB/GPIO Interface communicates with the on-chip SPI Slave. It programs the 14 bit code at the address via commands to the SPI slave. A C-API provided by Diolan was used to develop the program to download and upload firmware (in this case the *spi_ram.dat* file) to the program RAM via the on-chip SPI Slave.

WISHBONE INTERFACE TO I2C, SPI AND WATCHDOG TIMER CORES

The original OpenCore's 16F84 supported 64K memory mapped I/O by appropriating Port A and Port B, which had no use in an ASIC or FPGA environment. In Mini-PnP we map the Wishbone Crossbar Switch to the memory mapped I/O. In the 16F84 RTL, the memory mapped I/O data bus is a tristate bus. This simplifies the interface to peripherals. We use the capability of synthesis tools for both ASIC and FPGA designes to automatically redesign the tristate logic with multiplexers and combinational logic. In Mini-PnP we have also added a read strobe to the 16F84 RTL so that when reading from the memory mapped I/O a strobe can be generated in order to support the Wishbone interface.

INTERRUPTS

Mini-PnP SASIC supports an external interrupt signal. The external interrupt is activated by either an external interrupt signal to the chip, or the I2C cores. In addition interrupts are supported on the UART Transmit or Receive and Watch Dog Timer Core. Each interrupt can be masked. The source of the interrupt can be determined via a register read of the interrupt status.

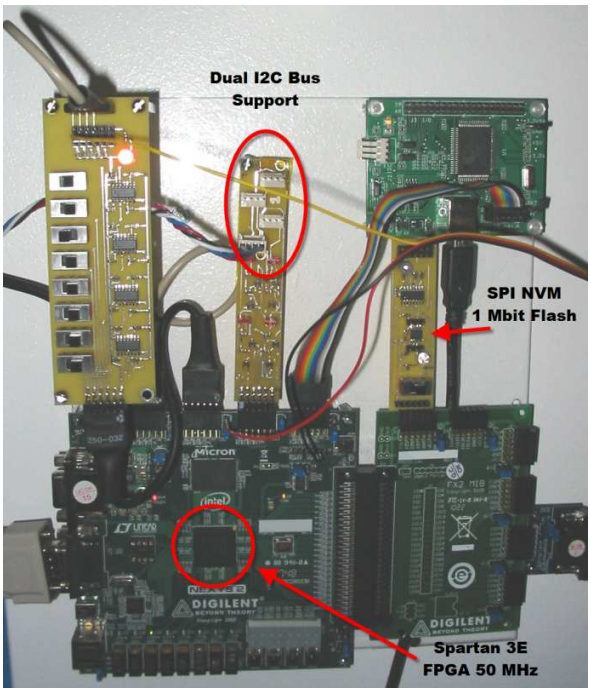

Figure 3. Mini-PnP Implemented on a Spartan 3E FPGA Running at 50 MHz Clock with I2C Hardware Support

FPGA AT SPEED (50 MHZ) IMPLEMENTATION

As part of the comprehensive verification plan for the ASIC flow, in the design and tape out of SASIC Mini-PnP, the RTL was implemented *at speed* on a Spartan 3E Xilinx FPGA running at 50 MHz. The only RTL that changed from the ASIC tapeout and the RTL implemented on the FPGA were the memory models. In the case of the SASIC Mini-PnP, the 4Kx14 EDAC RAM based on the Distributed RAM in the SASIC Fabric is used. Also to implement the GPIO, Xilinx and SASIC *Bidirect* primitives were used. Figure 3 shows a photo of the FPGA platform for Mini-PnP. The boards plug into Peripheral Modules (PMODS) (12 pin with 8 CMOS signals, power and ground). The FPGA board is a Digilent Nexys 2 board with a Spartan 3E 1200 kGate FPGA. The Dual I2C PMOD board and the EEPROM Bootup and xTEDS storage SPI NVM board were designed and built by Micro-RDC as well as the debounce switch array shown. The photo also shows the Diolan USB/I2C/GPIO board. The Diolan USB board was used to download firmware into on-chip Program RAM from a PC. Extensive use has been made of the Diolan C-API for manipulating the GPIO for interfacing to SPI devices including the SASIC Mini-PnP SPI slave for firmware download and upload.

MINI-PNP SASIC POST SILICON VERIFICATION

An evaluation Printed Circuit Board was designed for the Post Silicon Verification of the chip. The board supports multiple de-bounce switches for configuring the chip including reset and SPI download capability as well as manual and automatic bootup from EEPROM. The board has an ATMEL 1 Mbit (128Kx8) Flash SPI EEPROM (AT25FS010) that is used to store program code and xTEDS. The board also supports two I2C bus interfaces to convert the CMOS I2C signals from the chip to the I2C bus. It also supports the 8 GPIO CMOS signals routed to PMOD's as well as a Hirose FX-2 100 pin 100 MHz connector so that an external ROM can be used. The board supports three external supplies, 1.2V Core, 3.3V Chip IO, and 3.3V for the peripherals. These use BNC connectors and support individual current monitoring. Finally, the board supports a switch selectable single 5V supply with regulators for the three supplies.

The SASIC Mini-PnP die were bonded out using Gold Wire Bonding to a 172 pin Ceramic Quad Flat Pack (CQFP) package from Kyocera. The die specification and 172 pin CQFP package are presented in later sections.

Figure 4 shows the assembled Evaluation Printed Circuit Board, the Mini-PnP SASIC in a 172 pin CQFP package, socketed with an ENPLAS IC test socket. Note the socket has a top and bottom opening for Single Event Effect (SEE) testing. The board has provisions for crystal clock generators that plug into an SMA connector on the board. The SMA connector allows for clock sources of up to 100 MHz to be used to clock the chip. A separate chip buffers the clock that is supplied (with support for 2.5V IO) and also provides a buffered clock that can be used as a trigger source in measurements.

The SASIC Mini-PnP supports a 4 digit seven segment display that displays the lower 8 bits of the program counter and an 8 bit register which is very useful in code development.

The board measures 8.374 x 6.866 inches. It has 8 layers and has a height of 83.6 mils.

The test results of the taped out silicon are presented in Tables 1 and 2. All tests passed.

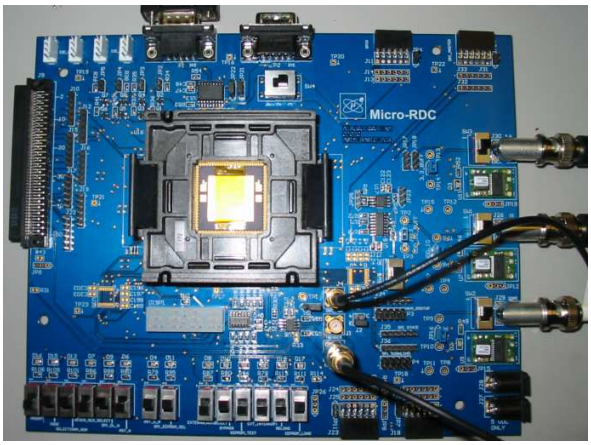

Figure 4. Mini-PnP SASIC Silicon Package in 172 pin CQFP with Socket in Assembled Evaluation Board.

Table 1. SASIC Mini-PnP Functional Tests Results for Taped Out Silicon

No.	Test Name	BlockTested	Function	Pass
1	uart	Built in UART	Output characters at 38400 bps	Yes
2	i2c_0_master	I2C Core 0 on Wishbone Bus Master	Read I2C ADC (Proximity Detector) Write DAC	Yes
3	i2c_0_slave	I2C Core 0 on Wishbone Bus Slave	Program I2C Address, Scan for Address, Verify Slave Address, Write	Yes
4	i2c_1	I2C Core1 on Wishbone Bus Master	Read I2C ADC (Proximity Detector) Write DAC	Yes
5	spi_core	SPI Core/Wishbone Bus	Read SPI EEPROM Manufacture ID/XTEDS	Yes
6	wdt_cop	Watchdog Timer Core/Wishbone Bus	Setup WDT and generate reset on mcu_rst_rld_n	Yes
7	on_chip_reg_banks	On chip register banks 96 bytes each	Write sequence and read back and check both bank0 and bank1	Yes
8	interrupt_i2c_0	interrupt flow, mask, status reg, i2c 0 core	Generate interrupt on Rx and Tx in I2C Core 0. Verify ISR for Ext. Interrupt	Yes
9	interrupt_i2c_1	interrupt flow, mask, status reg, i2c 1 core	Generate interrupt on Rx and Tx in I2C Core 1. Verify ISR for Ext. Interrupt	Yes
10	interrupt_wdt_cop	interrupt flow, wdt mask, status, WDT COP Core	Generate interrupt on WDT count down to zero. Verify ISR invoked and status showing interrupt	Yes

Table 2. SASIC Mini-PnP Complex Flows Test Results for Taped out Silicon

No.	Flow Name	Blocks Tested	Function	Pass
1	SPI_Download_PRGM_RAM_EXECUTION_WRITE	SPI Slave 4Kx14 EDAC Distributed RAM	Download code through SPI Slave, Execute from Distributed RAM, Upload via SPI Slave and Verify RAM	Yes
2	EEPROM_Bootup	SPI EEPROM Master, Muxes to Distributed RAM,Bypass Mode, Manual	Copy code from EEPROM into Distribued RAM with SPI Master, Execute and Test Distributed	Yes
3	Automatic_Reload_EEPROM	SPI EEPROM Master, Muxes to Distributed RAM Bypass Mode, Reload and Automatic Reset RAM Select, Soft Reset RISC	Copy code from EEPROM into Distributed RAM with SPI Master, Execute and Test Distributed RAM Program Memory Instruction Execution. Automatic Mode.	Yes

MINI-PNP SASIC POWER MEASUREMENTS WITH CLOCK SCALING

A key objective for the design of the SASIC Mini-PnP is to provide a radiation hardened microcontroller with I2C and GPIO interfaces with very low power requirements, for operation in spaceborne applications, where power, size and weight reduction are paramount. In this paper we present the results of measuring the core and IO current of the chip at various operating conditions. The SASIC Mini-PnP can operate with a clock frequency of 75 MHz. It was designed for a clock frequency of 50 MHz with the ability to scale the clock down to reduce power. In fact, the chip has been tested at a clock frequency of 143.229 KHz where the menu presented by the built in ROM for testing, is sent to a console via the serial port at 110 bps. In this mode, we were also able to bootup the Program Code using the on-chip SPI bootup and run the code from the on-chip RAM.

Figure 5 shows a bar chart of the Core, IO and Total Power in mW versus Clock Frequency. The Core supply was 1.2V and the IO supply was 2.5V. The measurements are also presented in Table 3.

Of note is that with no clock (standby mode), the total power consumption is 108 µW.

Another way to conserve power is to put the chip in Reset while the clock is still applied. In this case a substantial reduction of current is observed in the IO while the Core current decreases slightly. At a Core voltage of 1.32V and an IO supply of 3.3V, the IO current drops from 1.77mA to 0.070 mA. In general, keeping the chip in reset saves power but a better way is to do clock gating. In particular, for a sensor application the clock can be reduced which still allows monitoring of sensors and then ramped up.

Architectural modifications to reduce power are to allow for an idle mode where the CPU clock is turned off while the clock to the I2C cores or GPIO is kept active. On an interrupt, the chip is taken out of Idle mode. An adjunct chip can also provide clock gating and wake up on activity on the I2C bus or sensors. Based on the power results presented in this paper, the adjunct chip will consume very low power as it will operate at a very low clock speed.

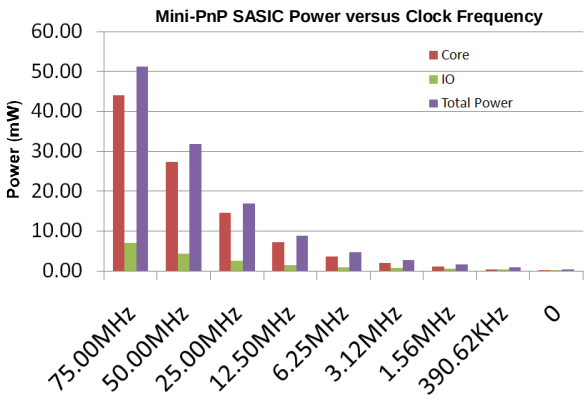

Figure 5. Mini-PnP SASIC Core, IO and Total Power (mW) Consumption versus Clock Frequency.

Table 3. Mini-PnP SASIC Silicon Current Measurements Core and IO

Mini-PnP SASIC				
Core Power, Vdd_Core=1.2V			IO Power, Vdd_IO=2.5V	
Frequency	Power (mW)	Current (mA)	Power (mW)	Current (mA)
75.00MHz	44.04	36.7	7.11	2.844
50.00MHz	27.36	22.8	4.44	1.774
25.00MHz	14.52	12.1	2.50	1.000
12.50MHz	7.32	6.1	1.55	0.618
6.25MHz	3.72	3.1	0.98	0.392
3.12MHz	2.016	1.68	0.70	0.280
1.56MHz	1.104	0.92	0.57	0.226
390.62KHz	1.104	0.92	0.57	0.226
143.229KHZ	0.276	0.23	0.48	0.197
0	0.1956	0.163	0.27	0.108

MINI-PNP SASIC DIE

Below we present the specifications of the Mini-PnP SASIC die. This information is useful in planning for packaging and MCMs.

Die Size

3.156mm X 3.543mm

- 64 micron pad pitch
- 50 micron x 50 micron pad size
- .7 mil Al bond wire recommended

Die thickness

470µm =.47mm

Mini-PnP SASIC uses 172 pins which are comprised of:

- 96 CMOS General Purpose I/O
- 17 VSS0
- 18 VSS1
- 17 3.3V Vdd IO
- 18 1.2V Vdd Core
- 6 Grounded Signals

MINI-PNP SASIC 172 PIN CQFP PACKAGE FOR POST SILICON EVALUATION (NOT FOR PRODUCTION)

For Post Silicon Validation and Evaluation purposes the 3x3mm Mini-PnP SASIC chip was packaged in a 172 pin Ceramic Quad Flat Pack (CQFP) package. The specifications for the 172 pin CQFP are shown in Figures 6 and 7.

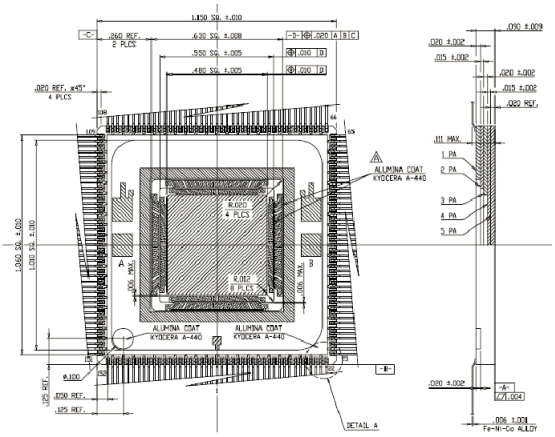

Figure 6. 172 pin Kyocera CQFP Mechanical Specifications. Dimensions in inches.

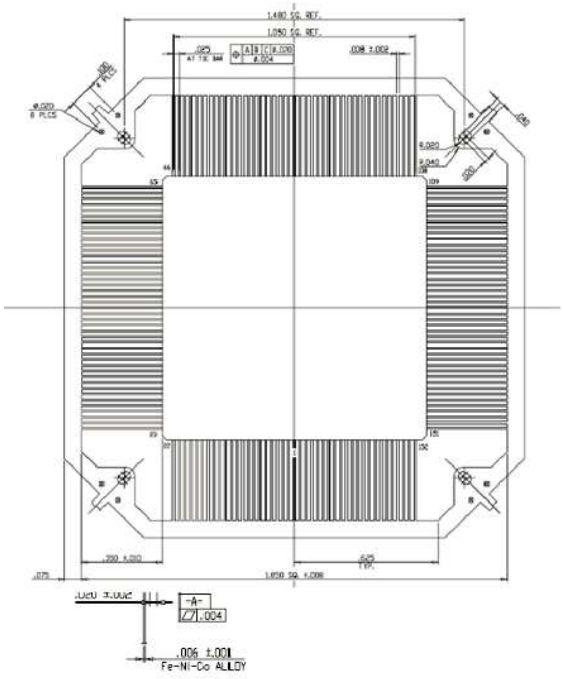

Figure 7. 172 Pin Kyocera CQFP Mechanical Specifications Continued.

MULTI CHIP MODULE DEVELOPMENT

The MCM uses Mini-PnP SASIC as the core of the MCM. The goal of the MCM investigation is to research the feasibility and issues involved with using the Mini-PnP SASIC in the simplest configuration possible. The present foot print target of the MCM is a sub 15x15mm MCM.

Figure 8 shows the pins required to meet the minimum requirement for Mini-PnP SASIC including bootup from SPI NVM. The figure shows that a Mini-PnP SASIC based MCM can be designed with 28 pins. If fewer pins are required, an I2C Master Bus can be sacrificed. Additional pins can be used to support more I/O and interrupt acknowledge freeing up the GPIO pins if necessary.

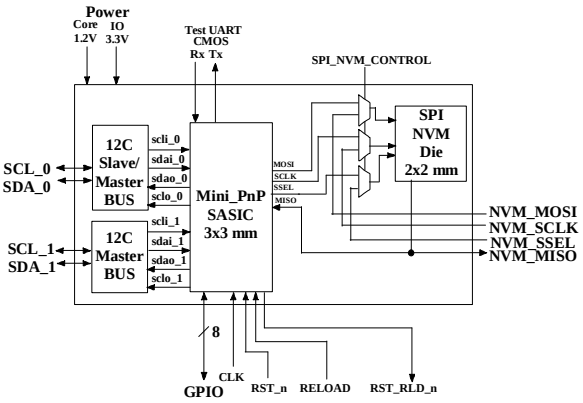

Figure 8. Mini-PnP SASIC MCM

In this paper we will show a COB design for the Mini-PnP SASIC. COB MCM's have been shown to considerably reduce the size of spaceborne electronics [9]. For considerations that need to be taken into account in manufacturing the MCM using COB and the space borne environment, see [9]. For the trends in COB in the industry see [10]. Figure 9 for illustration purposes shows a COB layout for the 3 x 3mm Mini-PnP SASIC die. Shown are the power supply rings for Core and IO supply. The ground shown is also used for die attachment. The landing sites on the PCB need to be configured for the design rules for the potential MCM manufacturer. In Figure 9, they are for illustration purposes only. For example, certain manufacturers allow for 75µ traces and spacings.

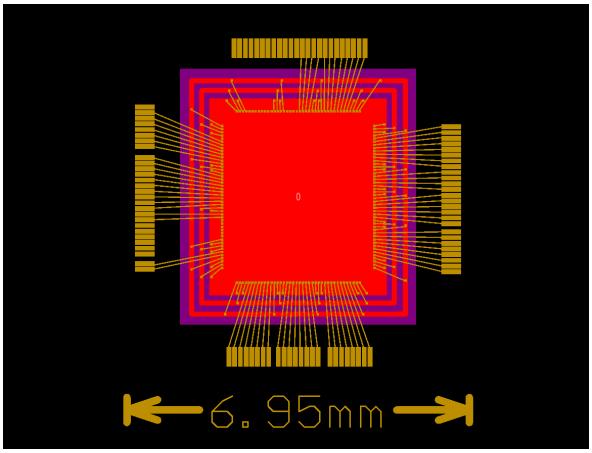

Figure 9. Mini-PnP SASIC Die COB

To achieve the smallest size and footprint for the MCM, the three dimensional techniques presented in [11] can be used. This work is the subject of a future paper. For a review of 3-D packaging technology see [12].

SUMMARY

The Mini-PnP SASIC chip has been taped out and verified in Silicon. It is a System on a Chip based on an 8-bit RISC with 4Kx14 on-chip EDAC protected Program RAM. The measurements of the current consumption in the taped out Silicon versus the clock frequency have been presented. Major savings in power can be achieved using lower clock speeds and ramping up the clock when greater processing power is needed. The Radiation Hardened Mini-PnP SASIC die can be used in MCMs to drastically reduce the pin-count and size for integration into spaceborne electronics.

ACKNOWLEDGMENTS

The work described in this paper has been funded by the Air Force Research Laboratory, Space Vehicles Directorate.

REFERENCES

1. Lyke, James, "Bringing the Vision of Plug-and-play to High-Performance Computing on Orbit", HPEC 2009

2. Lyke, J.; Space-Plug-and-Play Avionics (SPA): A Three-Year Progress Report, Proceedings of the AIAA Infotech Conference, 7-9 May 2007, Rohnert Park, CA.

3. Lyke, James, Don Fronterhouse, Denise Lanza, and Tony Byers, "A Plug-and-play Concept for Spacecraft", Proceedings of the 2005 MAPLD conference. (abstract) (presentation)

4. McNutt, Christopher, Lyke, James. CubeFlow: A Modular Open Systems Architecture for CubeSats, Proceedings of the 7th Responsive Space Conference, April 27-29, 2009, Los Angeles, CA.

5. Vera, A. , M. Sibley, S. Ardalan, K. Avery and J. Lyke, "Appliqué Sensor Interface Module Based on 90nm Rad Hard Structured Application-Specific Integrated Circuit, " AIAA Infotech Proceedings, Atlanta, GA, April 2010.

6. Mavis, D.G. and Eaton, P.H., "Soft Error Rate Mitigation Techniques for Modern Microcircuits", Proceedings of the 2002 International Reliability Physics Symposium (IRPS), pp. 216-225.

7. Mavis, D.G. and Eaton, P.H., "Temporally Redundant Latch for Preventing Single Event Disruptions in Sequential Integrated Circuits", United States Patent Number 6,127,864, October 2000.

8. G. Alonzo Vera, Sasan Ardalan, Keith Avery, "Fast Local Scrubbing for FPGA's Configuration Memories", AIAA Infotech Proceedings, Atlanta, GA, April 2010.

9. Binh Q. Le, Elbert Nhan, Richard H. Maurer, Robert E. Jenkins, Ark L. Lew, Howard S. Feldmesser, and Juan R. Lander, "Miniaturization of Space Electronics with Chip-on-Board Technology," Johns Hopkins APL Technical Digest, Volume 20, Number 1 (1999)

10. Die Products Consortium (DPC), "PCB design guidelines for chip on board (COB) applications," January, 2004

11. Saia, R.J. Wojnarowski, R.J. Fillion, R.A. Forman, G.A. Gorowitz, B. General Electric Company, NY "High Density Multichip Module Technology," Proceedings of the 1994 International Conference on Multichip Modules, 1994.

12. Said F. Al-sarawi, Derek Abbott, and Paul D. Franzon, "A Review of 3-D Packaging Technology," IEEE Transactions on Components, Packaging, and Manufacturing Technology-Part B, Vol. 21, No. 1, February 1998.