

NASA GSFC Development of the SpaceCube MINI

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ABSTRACT:

NASA, Goddard Space Flight Center is developing a radiation tolerant miniaturized space processor for use in a multitude of different space flight applications, from free flyers through embedded computing nodes. The Goddard design is building off of our expertise in the hardware/software design of the legacy SpaceCube 1 that flew on the Hubble Servicing Mission and the ISS MISSE7 experiment. The new design will physically conform to the volume requirements of a standard 1U (10cm x 10cm x 10cm) Cubesat. It will incorporate the Xilinx Virtex-5, the latest in high speed, high density, and with the SIRF variant, radiation tolerant FPGA design. Built in peripherals will include 512Mx16 of SDRAM, 96 gigabits of FLASH memory, a radiation hard Aeroflex FPGA (as a watchdog, configuration manager, and scrubber), a 12 bit analog to digital converter, and local power regulation. External interfaces are varied and plentiful with 2 SATA interfaces, 1 Xilinx MGT Interface, 4 Spacewire or 8 LVDS interfaces, 8 RS422 interfaces, and a handful of analog / single ended I/O. Power consumption will range from 5 to 15 watts. The GSFC SpaceCube MINI design even includes one expansion slot to add in an optional user I/O card. With this capability the end user can add in mission unique interfaces without having to resort to using another physical enclosure. The SpaceCube MINI has been designed to use either the radiation tolerant SIRF part from Xilinx, or a regular commercial Xilinx V5. This allows for varied mission requirements to be covered where either computing power and cost or radiation performance can be optimized using the same SpaceCube MINI design. Finally the SpaceCube MINI is designed to allow multiple SpaceCube MINI's to be daisy chained together, through Gigabit interfaces, enabling it to form an extremely powerful distributed computing node.

Introduction: The first SpaceCube designed and built by Goddard Space Flight Center (GSFC) was a small high performance reprogrammable computing engine that was conceived to perform autonomous docking of unmanned spacecraft. That SpaceCube flew on Relative Navigation Sensors (RNS) experiment during Hubble Servicing Mission 4 in May 2009, where it proved its ability to provide real-time pose estimation while the shuttle was docking with the Hubble Space Telescope.

Interest at GSFC grew as engineers and scientists realized the immense computing power and tiny size of the SpaceCube would allow both extensive and real time data analysis to be performed onboard of a satellite. This in turn would ease downlink requirements while providing better refined scientific measurements of onboard instrument data.

The original SpaceCube was based on the Xilinx V4 (FX60) FPGA, and was built using four inch by four inch printed circuit

boards in a slice configuration. Goddard engineers were looking at building a second generation of the SpaceCube at the same time Xilinx was promoting their new radiation hardened by design V5 FPGA's. This provided the perfect opportunity to incorporate the new Xilinx parts in a second generation of SpaceCube designs.

The second generation SpaceCube design at GSFC was pulled in two separate

directions. One thought was to use standard physical and electrical form factors, while the other chain of thought was to refine the original custom design into something even smaller than the original. GSFC was able to get internal research and development funding to pursue both of these goals. SpaceCube 2.0 is being designed and sized as an industry standard 3U cPCI card. The second development, SpaceCube MINI, is being developed in the very small 1U cubesat form factor (10cmx10cmx10cm).

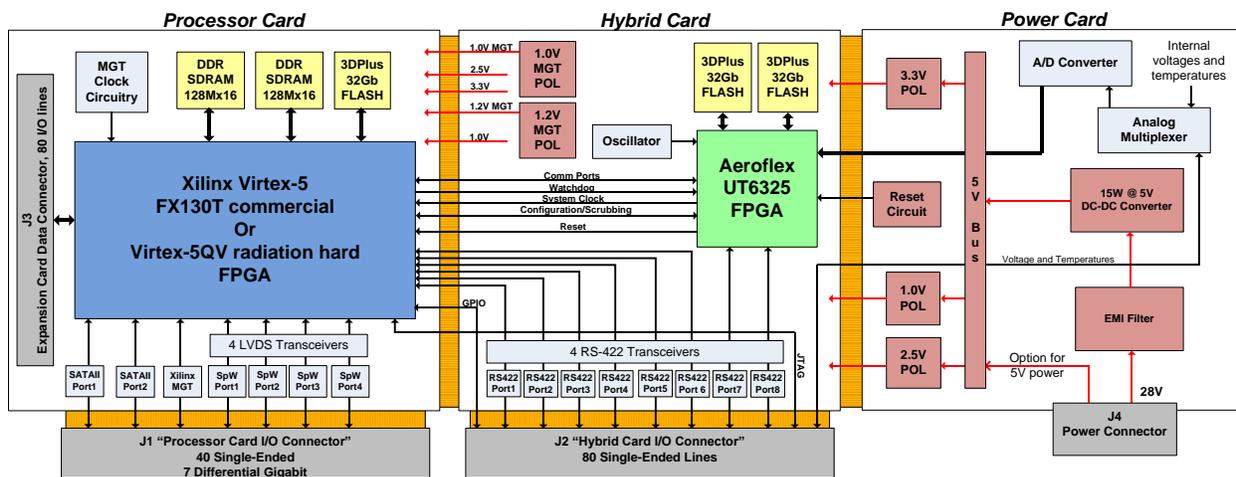


Figure 1 - SpaceCube MINI Block Diagram

Requirements: The SpaceCube MINI was designed as a follow on to the original SpaceCube and as a near functional equivalent to the SpaceCube 2, but in a cubesat 1U form factor. The driving requirements are:

- Cubesat 1U (10cm x 10cm x 10cm)
- <10 Watts
- 2000 MIPS
- < 3 lbs
- Xilinx V5 XC5VFX130T commercial, or Space-grade Virtex-5QV

Features: The SpaceCube MINI has many built in features easing application development and eliminating the need for additional hardware. Key internal features are:

- 512Mx16 of SDRAM
- 96 gigabits of FLASH
- 12 bit analog to digital converter
- local power regulation
- Expansion I/O card capable

External interfaces:

- 2 SATA interfaces
- 4 Spacewire or 8 LVDS interfaces
- 8 RS422 interfaces
- Xilinx Multi-Gigabit Transceiver (MGT)
- 2 Passive thermistors
- 5 Analog inputs
- Power 28V +/- 7V or 5V regulated



Figure 2 - SpaceCube MINI folded flat

Form Factor: The SpaceCube MINI is being built to fit in the physical envelope of the CubeSat 1U form factor. The MINI physical housing is currently being designed as a cube at just under 10cm on each side. The housing is 100 mils thick aluminum, providing strength, thermal mass, and limited radiation shielding. The printed circuit board for the SpaceCube MINI is being built using rigid-flex technology. This allows the SpaceCube MINI to be folded up to fit inside of the required volume. The SpaceCube MINI functionality requires three sections of PCB connected by two rigid-flex sections. The printed circuit board is folded into a “U” shape, with each PCB getting attached to one wall of the mechanical housing. This provides each board with direct thermal path to the structure. An optional fourth expansion PCB can be connected internally to the SpaceCube MINI design. The expansion I/O card can hold a custom electrical interface and does not need to be made using rigid-flex. The mechanical and PCB design are being analyzed to handle the harsh launch vibration characteristics of a sounding rocket launch vehicle. In addition a complete thermal analysis of the system will be performed when the layout and mechanical designs are complete.

Radiation: The SpaceCube MINI is being designed with radiation hard/tolerant

components. The system is going to be very reliable to radiation upsets, even in less benign polar or geosynchronous orbits. For radiation hardness, there is really is no comparison between the typical commercial /university cubesat and the SpaceCube MINI beyond the shared cubesat form factor. Commercial cubesats use commercial parts that have no radiation testing and are typically flown in very low earth orbits (450Km), where radiation effects are greatly diminished. This is in stark contrast to the SpaceCube MINI design which uses fully qualified military/aerospace components that are tested and certified to their datasheet extremes. The inherent TID capability of the electrical components used in the SpaceCube MINI design varied from 50 -700 krad(Si) . It is possible to shield the softer parts to obtain higher capability, depending on the environment. The heart of the SpaceCube MINI is the Virtex-5QV part which is designed to be radiation hard up to 700 krad(Si)¹. Xilinx used a different transistor cell architecture than in their commercial devices in order to harden the flip-flops and configuration memory within the device. NASA is planning to perform independent radiation testing on the Xilinx part sometime in the future. Finally, the onboard SDRAM is mitigated by using an EDAC memory controller inside the FPGA. Potential orbits and high value applications for the SpaceCube MINI are infinite.

Reconfigurability: The SpaceCube MINI is at its heart a reconfigurable computer. This is because the design is based on the Xilinx V5 FPGA. The V5QV is a sea of radiation hardened gates that can be configured for almost any mission requirement. Coupled with the large number of standard I/O interfaces in the base design, we hope that the hardware can remain unchanged between different missions, with

¹ See Reference 1.

only the VHDL/Verilog code within the V5 changing. This would permit the hardware to be built to print, saving the many engineering design/analysis hours. Time could instead be spent crafting any mission specific custom algorithms. There are many additional benefits with the reconfigurable architecture. Benefits span the range of reconfiguring the hardware in flight as to accomplish additional or enhanced scientific requirements, all the way to easing the development and testing of code in the engineering lab. Reconfigurability in flight has been proven in flight by the GSFC SpaceCube on the Materials International Space Station Experiment 7 (MISSE7) payload. The VHDL code within this SpaceCube has been reconfigured in flight to allow additional data to be collected as the scientific experiment progressed.

Power: The SpaceCube MINI is on the leading edge of the MIPS to Watt performance metric for spaceflight computational engines. When the SpaceCube MINI is populated with the commercial Xilinx V5, it has two power PC processors coupled with a huge sea of gates. The gates can be programmed as accelerators to further speed up any CPU intensive operation. This set-up provides the highest computing power per watt. When configured with the commercial Xilinx V5, radiation tolerance (scrubbing, watchdog functions) are managed through an onboard radiation hard one time programmable Aeroflex FPGA. Instead, if radiation susceptibility is the most critical requirement for a mission, then the radiation hardened Space-grade Virtex-5QV can be used. The downside of this part is that the embedded PowerPC processors are factory disabled. To compensate for this, one or more Xilinx soft core MicroBlaze processors can be embedded to provide substantial computational resources for a Virtex-5QV design.

Scalability: Is easily achieved with the SpaceCube MINI design. The configuration of the external MINI I/O includes a Xilinx Multi-Gigabit Transceiver (MGT) interface. This high speed serial channel can be daisy chained to additional SpaceCube MINI's as required. This allows for incrementally increasing the computing and I/O resources as the mission requirements dictate by adding additional SpaceCube MINI computing nodes one at a time.

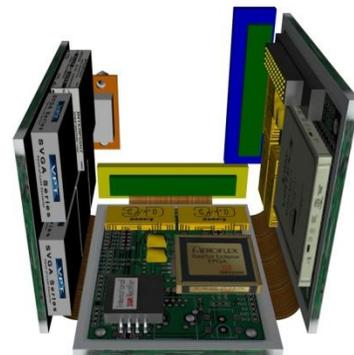


Figure 3 - SpaceCube MINI flight configuration

Cost: The SpaceCube MINI will keep overall project costs low because it is reconfigurable. The design has been built with an abundance of the most common spacecraft interfaces, RS422, LVDS which with the proper Intellectual Property can function as Spacewire, Ethernet, or any proprietary interface as desired. This allows the core circuit board to be built to print, obviating the need for engineering time to design, test, and fabricate hardware for each mission. Project risk is also reduced as the core hardware design will already have been tested and verified. If a unique electrical interface is required by a mission, then it can be designed onto the optional expansion I/O board. This only requires one interface board to be design and tested and would not change the previously verified core SpaceCube MINI design. Finally the SpaceCube MINI is designed to support

either the radiation hardened Xilinx or the low cost commercial variant which can greatly reduce the overall parts cost.

4. http://esto.nasa.gov/conferences/estf2010/papers/Flatley_ESTF2010.pdf

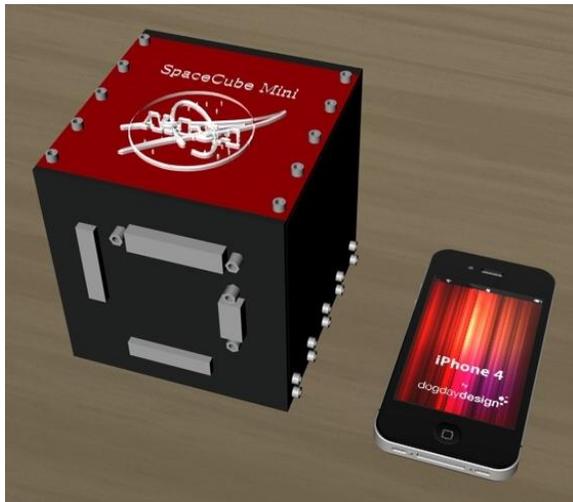


Figure 4 - SpaceCube MINI size comparison

Availability: The SpaceCube MINI design is currently in layout. The design team will complete layout over the summer months and the first production boards will be fabricated late summer, early fall. Testing / verification of the design will happen late fall.

The first SpaceCube Mini will fly as part of the Intelligent Payload Experiment (IPEX) CubeSat that will demonstrate advanced on-board processing capabilities for missions such as HypIRI. Additional SpaceCube Mini systems are baselined for GSFC Technology Demonstration CubeSats (TechCube) and the collaborative sounding rocket experiments with DoD/ORS.

References:

1. http://www.xilinx.com/support/documentation/data_sheets/ds192_V5QV_Device_Overview.pdf
2. <http://en.wikipedia.org/wiki/SpaceCube>
3. <http://gsfctechnology.gsfc.nasa.gov/SpaceCube.htm>