Reconfigurable, Radiation Tolerant S-Band Transponder for Small Satellite Applications

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ABSTRACT

Southwest Research Institute (SwRI) has developed a reconfigurable, radiation tolerant, communication system that addresses the needs for low-cost, quick turn spacecraft, as well as the reliability and connectivity required in harsh radiation environments of higher orbit systems. The core of such a Flexible Communication Platform (FCP) is a Software Defined Radio (SDR) architecture, currently providing S-Band (2 GHz) communications but expandable to other frequencies. The Digital Processing Unit (DPU) is a PC/104 slice that can be used as a standalone radio with an onboard RF chip for LEO environments or can be augmented with an RF front-end on a separate slice. The architecture of the DPU is based around an SRAM-based FPGA. SRAM-based FPGAs, however, have significant limitations in spacecraft systems due to radiation susceptibility of the FPGA programming cells. SwRI chose to implement a combination of triplicated logic (TMR) and Configuration Memory Scrubbing, specifically in an external RAD-Hard device, to mitigate radiation effects on the system. The flexible design of the DPU all ows rapid integration into multiple target mission architectures. When coupled with the RF front-end, the FCP is capable of communicating from LEO and MEO orbits using a variety of wideband signals and protocols.

INTRODUCTION

Over the last three decades, SwRI has provided advanced spacecraft electronics for NASA, the European Space Agency (ESA), and the U.S. Department of Defense (DoD). SwRI avionics systems have an unparalleled track record, having flown on over 60 missions without a single on-orbit failure. Our role as a supplier has grown from providing subsystems to providing entire spacecraft avionics.

The latest trend in spacecraft development has been away from the big flagship missions, with budgets greater than one billion dollars and schedules with 5-10 years in development, towards lower cost spacecraft with shorter development schedules. This trend is best observed through the efforts of the DoD's Operationally Responsive Space Office (ORS) which has the goal of launching <$20M spacecraft within seven days of being requested. Other low cost, quick turn spacecraft efforts also cater to extremely small satellites, like CubeSats. The military and civilian space community is investing heavily in these new mission classes.

Current lead times on S-Band transceivers are in excess of one year and these systems do not provide any capabilities for rapid reconfiguration or Level-Zero commanding, which provides basic functional control of the spacecraft through the receiver. Existing CubeSat communication subsystems have been dominated by UHF or VHF solutions that can transmit less than ten kilobits per second. While this supports the student experimental community, advanced science and DoD systems require much higher data rates which can only be supported by an S-band transceiver.
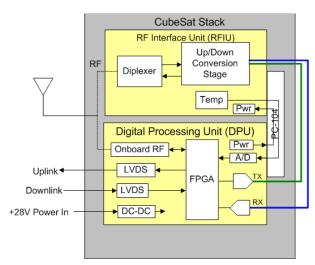

Figure 1: Radio Top Level Block Diagram

FCP DESIGN DRIVERS

Orbital Considerations

The desired orbit of a space system drastically affects the design choices available to the system engineers.

Low Earth Orbits (LEO) are orbits less than 1000km where the radiation environment is relatively benign (i.e. <5kRad 1 year mission total dose (TID)). Standard commercial off the shelf electronic components have a reasonable chance of performing well in this environment. Medium Earth Orbits (MEO) are drastically more challenging (i.e. 100KRad 1 year mission TID) and require the use of radiation tolerant or hardened electronic devices to ensure reliability and prevent the electronics from destructive latch up conditions due to radiation. The ability to tolerate a high radiation environment is a critical constraint upon the RF design due to the significant limitations in available, flight qualified parts. An RF designer must examine standard commercial parts and determine ways to ensure their suitability in the radiation environment. Accommodating both LEO and MEO environments is a critical design requirement for the FCP.

Reconfigurable Systems

The basic model for these new mission classes utilizes in-advance hardware builds that have components on the shelf and available for quick deployment. The key is to utilize reconfigurable components that can be rapidly deployed with mission specific coding. It's important to distinguish this capability from reconfigurable computing. Reconfiguration of the base system components in the FCP means adapting the modem and codec of the radio while maintaining a common software interface.

A solution for reconfigurable radios utilizes SRAM-based FPGAs. However, these FPGAs have significant limitations in space-based systems due to possible radiation susceptibility of the FPGA programming cells. Consequently, SRAM-based FPGAs are frequently excluded from any mission critical systems or instruments in current spacecraft systems. This limitation has been recognized and work to develop mitigation strategies is an active area of research. Strategies such as automated Triple Modular Redundancy (TMR) and memory scrubbing have been studied as methods of increasing the radiation performance of the parts. TMR replaces every transistor in the design with three transistors and a voting circuit, allowing the upset of up to a single transistor before functional behavior is affected. Memory scrubbing tasks require an external component to continually verify that the FPGA remains properly programmed and to correct any errors within the configuration logic should it become corrupted.
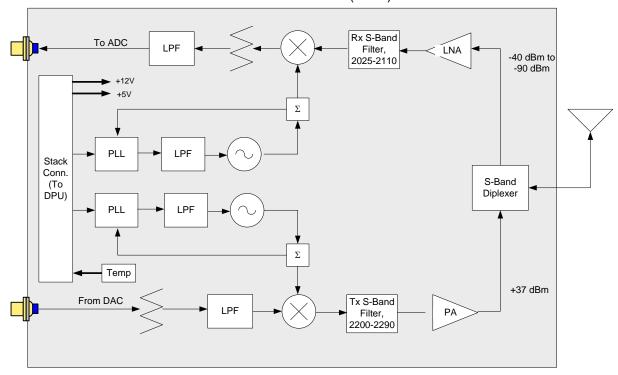
RF Interface Unit (RFIU)

Figure 2: RF Interface Unit (RFIU) Block Diagram

OBJECTIVES

The FCP was designed with the following objectives:

1. Develop a reconfigurable RF processing node that can support multiple frequency bands (S, X, Ka, etc.) and incorporates radiation mitigation provisions to ensure reliable operation in high radiation environments.
2. Create a reference design for a radiation tolerant RF front end for initial deployment of the FCP as an S-Band transceiver.
3. Implement the above items within a single PC/104 slice for a CubeSat solution.

DIGITAL DEVELOPMENT

The initial target mission profiles chosen for the FCP provide the primary input for establishing the physical and interface requirements. Targeting CubeSat missions presents the most challenging form factor requirement. To fit within the CubeSat envelope, the FCP was designed as a single, fully functional PC/104 slice radio with an onboard RF front end suitable for LEO applications. For more stringent radiation environments, radiation tolerant RF electronics are included on a separate RF Interface Unit (RFIU) slice (see top level block diagram in Figure 1) with oscillators, mixers, up / down conversion stages and amplifiers. The DPU provides spacecraft command and telemetry interfacing and reconfigurable SDR algorithm resources (i.e. FPGAs, memory, embedded processing IP cores) as well as an optional on-board RF front end.

The DPU features SMA style connectors for both IF (from FPGA to RFIU) and RF (from onboard RF chip to antenna) signal transmission, a PC/104 connector providing power delivery and debug access, and a 25-pin Micro-D for the command and data handling interface.

The DPU utilizes a PC/104 mechanical interface for input power. An IF interface is also available through the PC/104 connector in order to conform to the specification for the "CubeSat Kit Bus," established by Pumpkin, Inc. In this manner, the DPU can more readily integrate into a CubeSat Kit, and generate all the required local voltages from a single, +5V power input. Local voltages are regulated from +15V or +5V power inputs generated by a host slice, a separate power slice, or an external supply, delivered to the DPU and RFIU via the PC/104 interface.

RADIATION CONSIDERATIONS

An external FPGA is used to implement a programming/scrubbing algorithm that detects and corrects the occurrence of SEE's. The functionality of

SRAM-based FPGAs are defined by the bitstream loaded into its configuration memory on power up. The configuration bitstream provides the information to the logic cells inside the device that executes the user-defined logic operations. Both the configuration memory and the functional logic cells are susceptible to radiation effects; in fact, previous studies indicate that the configuration memory is particular susceptible.[1] Because of their versatility, much effort has been expended to develop and characterize effective mitigation techniques for SRAM-based FPGAs. SEU's in the configuration memory do not necessarily result in functional error, but they must be detected and corrected to prevent accumulation. Additionally, potential errors in the logic cells must be minimized. Xilinx Application Note XAPP987 describes several approaches designers may select for mitigation in their devices.[2] The different options discussed there are summarized in Table 1.

Table 1: Radiation Effects Mitigation Strategies

Mitigation Technique	Description
Power Cycling	Device is power-cycled, and its contents refreshed. Accumulated errors in the configuration memory and user logic are removed.
Configuration Memory Scrubbing	Configuration memory is continuously re-written with correct data by external or internal logic to detect and correct SEUs in the configuration bitstream. Prevents design alterations caused by SEUs, but not functional errors.
Triple Mode Redundancy (TMR)	Design elements are triplicated and implemented in a voting scheme. Helps mitigate SEU impacts on the user logic.
Redundant Devices	Design duplicated on multiple devices, with an external voting scheme applied on the output(s). The most effective of the mitigation techniques listed, but also the most complex & costly to implement.

For space-based designs involving SRAM-based devices, a mitigation strategy must be identified that is appropriate given the radiation environment of the target mission profile. For the FCP, power cycling and

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redundant devices were immediately dismissed. The FCP cannot tolerate the disruptive nature of power cycling the device, and the 1U form factor prevents the insertion of multiple redundant devices. This leaves TMR and scrubbing. Ultimately, a combination of TMR and configuration memory scrubbing was selected. The combination of the two techniques minimizes complexity and cost while maximizing overall mitigation strength. For the FCP, an external radiation hardened device implements the configuration and scrubbing logic. Utilization of the external hardened device provides several advantages over implementing the scrubbing logic in the target FPGA. Most importantly, the (external) approach has previously exhibited superior performance.[3] One major factor is that the scrubbing logic in the external device does not require any additional mitigation; it is protected by the hardened structure of the device. Conversely, scrubbing logic that is resident in the target FPGA is limited by the radiation characteristics of that device.

RADIO FRONT END

Modulator and demodulator (MODEM) algorithms were prototyped in Matlab for OQPSK and FSK signals with the following characteristics:

- FSK
  - Bit Rate 2 kbps
  - Frequency Shift 10 kHz
  - Intermediate Frequency 5 MHz
  - Sampling Rate 80 MSa/s
- OQPSK
  - Symbol Rate 1.5 MSym/s, Bit Rate 3 Mbps
  - Intermediate Frequency 5 MHz
  - Sampling Rate 60 MSa/s

A block diagram of the RF front-end electronics, shown in Figure 2, was completed along with link budget analysis and a preliminary radiation-tolerant part list. The FSK demodulator was updated to accommodate Doppler shift, and the algorithms were implemented in Verilog. The FSK demodulator algorithm was ported to Verilog using Xilinx cores for sine wave generation and filter implementation. Each stage of the algorithm was verified in simulation against the Matlab implementation to ensure performance. After FSK modulation was fully vetted in simulation, the simpler OQPSK modulator was converted to Verilog and verified in simulation.
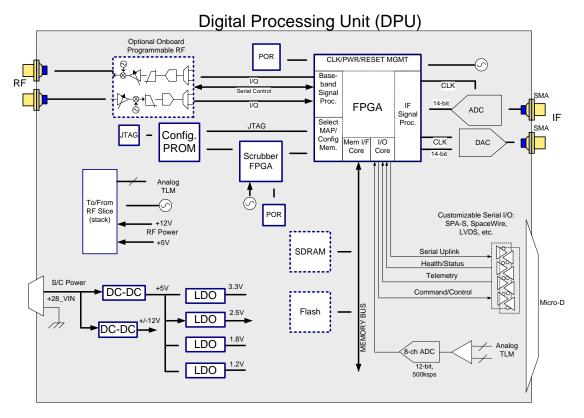

Figure 3: Digital Processing Unit (DPU) Block Diagram

DPU BOARD DESIGN

The DPU power (+5V IN) and CubeSat Kit Bus are implemented through a PC/104 connector located on the board. This design is compatible with Pumpkin's architecture, and can mate and directly interface with Pumpkin's Pluggable Processor Modules (PPMs), which would act as a host. The UART interface on the CubeSatKit bus utilizes dual ports with 3.3V I/O. For the FCP, Port 0 has been designated the Communication Interface (uplink/downlink) and Port 1 the Configuration / Control Interface. Provisions will be made for optionally selecting LVDS as the Communication Interface. The DPU block diagram is provided in Figure 3.

The SRAM-based FPGA is the heart of the DPU. The RAD-Hard PROM is responsible for storing the configuration bitstream, while the external RAD-Hard FPGA provides the configuration management and scrubbing logic. External memories are available to the FPGA to facilitate the use of future DPU baseband to IF processing needs. 128MB of SDRAM and 2GB of Flash, both with Double Error Detect, Single Error Correct Hamming code Error Detection and Correction (EDAC) protection, make up the memory bus, and the command and data handling interface is provided, utilizing LVDS signaling via a 25-pin Micro-D connector. Local voltages of 3.3V, 2.5V, 1.2V, and 1.8V are generated by a DC-DC converters from the +5V input.

PARTS ENGINEERING

Selection of the components for the FCP represented a significant challenge. Functional requirements were weighed against size, power, cost, availability, and radiation performance. Devices were chosen so that the prototype FCP could be built using either commercial or commercial-equivalent parts.

FPGA DESIGN

A modular architecture for the FPGA was chosen based upon the operational requirements of the DPU, shown in Figure 4. The Top-level Controller Core dictates the entire operation of the FPGA. It accepts inputs from all the sub-modules, determines the appropriate behavior, and drives the outputs, as necessary. Along with a set of control and status registers, a master state-machine is the primary design element in the core. A short description of the operation of each core is provided
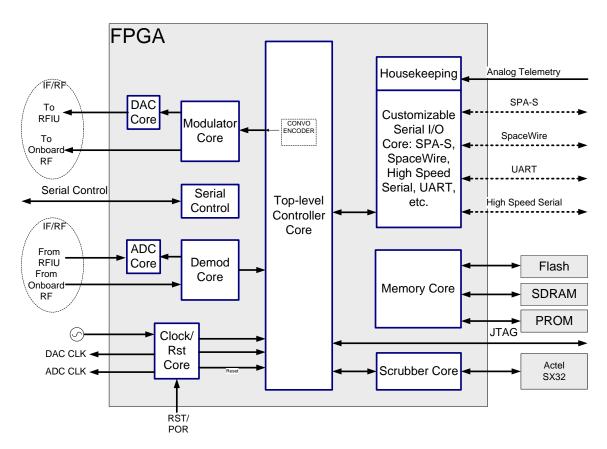

Figure 4: Flexible Communication Platform (FCP) Digital Processing Unit (DPU) FPGA Block Diagram

below:

- UART Core: Since there are 2 UART ports on the CubeSat Kit Bus, there will be two instantiations of this core. The first core will receive data and pass it on to the Modulator and DAC cores for transmission (optionally, Convolutional Encoding will be applied to the data stream). The top level controller core will also sync and transmit data (to an external host) that has been received from the ADC and demodulator cores. The second UART core will transmit/receive control and configuration data.
- Modulator Core: This core performs FSK modulation and up-conversion of the transmitted data passed to it through the Top-level Controller.
- Demodulator Core: This core performs down-conversion and OQPSK demodulation of the data from the ADC core and passes the results on to the Top-level Controller.
- DAC Core: Drives data and control signals out to the DAC.
- ADC Core: Accepts input directly from the ADC.
- Clock/Reset Core: Is responsible for processing / distributing the global clock and reset signals.
- Scrubber Core: Interfaces with the scrubber logic in the FPGA to provide configuration and scrubbing operations. SEFI counts from the scrubber logic are accepted and reported by this core.
- Memory Core: Handles operation and EDAC of the Flash and SDRAM devices.
- Tx FIFO: Provides internal storage for transmit data.
- Rx FIFO: Provide internal storage for received data.
- SpaceWire core: Provides the capability to communicate as a node over a SpaceWire link supported via the 25 pin front panel connector.

MITIGATION STRATEGIES

Configuration Memory Scrubber

The design of the scrubber logic is based in large part on 4. The application note describes in detail the method through which an external scrubber can exploit the "SelectMAP" interface to perform the necessary configuration memory accesses (readback/scrubbing). This operation enables the scrubber to detect and correct SEE's without disrupting the operation of the device. Some classes of SEE's, however, result in operational disruption. These are referred to as Single Event Functional Interrupts (SEFIs). In SRAM-based FPGAs, SEFI's in the configuration memory can originate from four primary areas:

POR SEFI: Virtex-4 behaves as though the device is powering on (indicating an upset around the PROG pin)

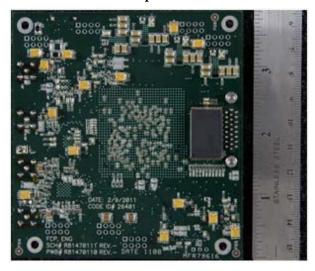**Figure 5: Flexible Communication Platform (FCP) Top View**

Figure 6: FCP Bottom View (with ruler for scale)

SMAP SEFI: scrubber loses access to the SelectMAP interface

FAR SEFI: a problem occurs with the Frame Access Register (scrubber loses access to configuration memory or cannot properly address the memory)

Global SEFI: malfunction of a handful of global signals can result in loss of configuration logic

While the external scrubber cannot correct the SEFI's described above, it has the ability to detect them, and provide an occurrence count for each of them back to the SRAM-based FPGA device. In summary, the scrubber is capable of preventing the accumulation of SEU's through partial reconfiguration, and can detect and recover from SEFI's. Recovery is achieved by pulsing the PROG pin.

Triple Modular Redundancy

Mitigation for the user logic inside the SRAM-based FPGA is implemented through application of TMR. Traditional TMR is a well established technique that involves triplication of registers in the design and insertion of a voting scheme. Theoretically, if a radiation event occurs in one of the triplicated circuits, the other two "out-vote" the erroneous signal to overcome the radiation effect on the output.

Manual application of TMR, however, can be extremely labor intensive and rife with engineering pitfalls. The current approach is to use an automated utility to apply TMR to the design. Xilinx TMRTool is the current approach.

CONCLUSION

SwRI is pleased to introduce the Flexible Communication Platform (FCP) radio (Figure 5 and Figure 6) for LEO and MEO missions. Designed with both low-cost missions, including CubeSats and small satellites, and high-reliability missions situated in harsh radiation environments, including earth orbits above 750 km, the FCP is an ideal solution for high bandwidth downlink requirements and fast intra-satellite communication links. Based on a standard PC/104 form factor, the FCP takes full advantage of reprogrammable FPGAs to provide a host of modem and codec options and employs strategic radiation mitigation techniques, including TMR and external configuration memory scrubbing. All components have radiation-tolerant counter parts that can be used as drop-in replacements for a high-reliability platform.

References

1. H. Quinn, "Tools for FPGA SEU Mitigation/Fault Tolerance," presented at the Military and Aerospace Programmable Logic Devices (MAPLD) Conference. LANL, 2009.

2. "Single event upset mitigation selection guide, application note XAPP987," Xilinx, Mar. 2008.

3. M. Berg et al., "Effectiveness of internal vs. external SEU scrubbing mitigation strategies in a xilinx FPGA: Design, test, and analysis," in Radiation and Its Effects on Components and Systems (RADECS). 4th European Conf. on, Deauville, France, 2007, pp. 516–523.

4. "Correcting single-event upsets in virtex-4 FPGA configuration memory, application note XAPP1088," Xilinx, Oct. 2009.