Fully-Integrated Electronic System for a Plasma Impedance Probe

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ABSTRACT

This paper describes a single-chip electronic system for a Plasma Impedance Probe (PIP) currently being developed for microsatellite instrumentation. The chip integrates all of the major analog and mixed-signal components needed to perform swept-frequency impedance measurements. By integrating these components onto a single chip, the weight and volume of the PIP instrument are drastically reduced. Unlike previous PIP designs, the integrated PIP performs direct voltage/current sampling on the probe's terminal. A Fast Fourier Transform (FFT) is performed by an off-chip FPGA to compute the impedance of the probe. By performing A-to-D conversion as early as possible in the signal flow chain, the design is made less sensitive to variability in analog components. By using an FFT operation, the instrument is made less sensitive to transient spikes that proved disruptive in previous PIP designs.

INTRODUCTION

The Plasma Impedance Probe (PIP) is an electronic instrument that measures the impedance of a probe immersed in a plasma environment. By analyzing the probe's impedance curve, major plasma characteristics can be deduced, including the electron-neutron collision frequency, the electron plasma frequency and the plasma's electron density¹.

PIP instruments have been studied for forty years, and a variety of technical approaches are reported in the literature. Steigies² reported a design in 2000 that measured the magnitude of the plasma impedance while sweeping over a wide range of frequencies. This data was used to determine the plasma density in sounding rocket flights.

In 2006, Hummel³ reported a PIP instrument that used a quadrature method to measure both magnitude and phase data. The magnitude and phase were extracted using an envelope detector and a phase-locked loop, respectively. By measuring the magnitude and phase of the probe impedance, a larger variety of plasma characteristics can be calculated.

Sanderson⁴ performed a detailed analysis of the quadrature PIP's design and its performance in sounding rocket flights. He found that the instrument's reliability was limited by various transient errors that upset the stability of the quadrature design. The quadrature design also relied on a Direct-Digital

Synthesizer (DDS) to produce a precise sinusoidal stimulus for the probe. The quadrature PIP's accuracy and stability were adversely affected by imperfections in the DDS signal.

PIP ELECTRONIC DESIGN

This paper proposes a new electronic PIP design in which the probe's voltage and current are sampled directly. This approach eliminates the PIP's requirement for a pure sinusoidal stimulus, and greatly relaxes the error tolerance for the DDS. The new design eliminates analog signal processing wherever possible, thereby eliminating several sources of error and instability from the system.

The impedance magnitude and phase are extracted by a Fast Fourier Transform (FFT), which is performed off-chip in a complementary FPGA device. The FFT operation is insensitive to transient errors and increases the noise immunity of the system.

System Architecture

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The new PIP architecture is shown in Figure 1. The plasma probe is stimulated by a sinusoidal voltage waveform, which is generated by a DDS component. An op amp configured as a transimpedance amplifier replicates the DDS signal on both of its terminals. The probe's current passes through the feedback impedance, Z_F , so that the op amp's output signal is $V_{\rm DDS} + IZ_F$.

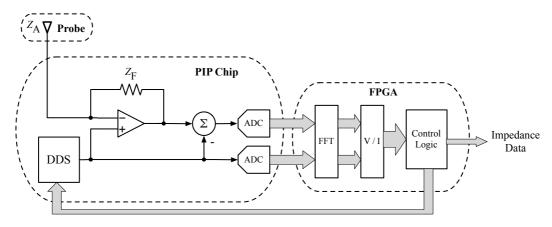


Figure 1: PIP electronic system architecture.

The DDS voltage signal is subtracted from the op amp's output. The remaining signal is proportional to the probe's current. This signal and the DDS signal are sampled by a pair of matched ADCs.

After sampling the $V_{\rm DDS}$ and $IZ_{\rm F}$ signals, the samples are delivered to an FPGA for digital signal processing. The FPGA performs an FFT operation on each signal at the frequency corresponding to the DDS's fundamental component. The two FFT outputs are then divided to produce the impedance. The FPGA contains control logic which coordinates a frequency sweep from 125kHZ to 20MHZ, and delivers impedance data to other system components (e.g. a telemetry data transmitter).

Advantages

The system has a high tolerance for common analog errors, such as non-linear distortion, clock jitter and transient spikes or glitches. The spectral effects of these errors tend to appear away from the fundamental component, so they are effectively filtered out by the FFT operation. For the same reason, the DDS signal can be any periodic waveform, not necessarily a sinusoid.

Because a precise sinusoid is not required, it is possible to use a simplified, low-power DDS design. The DDS proved to be a major consumer of power in the quadrature PIP design³. By using a low-power alternative, the instrument's power consumption can be reduced to a level that is acceptable for microsatellite deployments. After eliminating most analog signal processing, the proposed system requires only two precision analog components: the transimpedance amplifier and the ADC.

Design Methodology

Our design approach for the new PIP system is strongly focused on analog errors and variations. Revisions are costly in fully-integrated designs, so the design must be thoroughly characterized and verified before fabricating any prototypes.

To evaluate the error tolerances in the PIP chip's integrated parts, we ask two fundamental questions for each component:

- 1. What are the major errors and parametric variations associated with the component?
- 2. For each error or variation, what is its effect on the accuracy and precision of the impedance measurement?

These questions are addressed using a top-down design strategy in which every effect is evaluated within the context of a full system simulation. A complete system framework is created using Matlab/Simulink. This framework includes physical probe/plasma models, the DDS, transimpedance amplifier, ADCs, FFT, impedance computation and control logic.

To evaluate the impact of errors and variations, the Simulink framework is disturbed by inserting a component error model. We then evaluate the error's effect on the impedance calculation. For random parametric variations, Monte Carlo simulations are performed. The variation's impact is quantified by calculating the statistical variance in the measured impedance.

By evaluating each error and variation, design effort can be focused on reducing the most significant error sources. The top-down strategy also allows us to simulate errors and variations in groups, so that we can quantify the accuracy and precision of the PIP under the influence of all errors and variations. This assessment reveals the value and limitations of the PIP as a scientific instrument.

Transistor-Level Design

The top-down design strategy is useful for system modeling and for transistor-level component design. The central problem in integrated system design is behavioral verification: the entire design hierarchy must function together as a cohesive instrument.

Our component design/verification strategy is illustrated in Figure 2. For integrated component design, we use the Cadence chip design tools. Within Cadence, the PIP chips's complete design hierarchy is built using the Verilog-AMS language. Verilog-AMS is a behavioral language for modeling analog/mixed-signal components. Verilog-AMS simulations allow for a mixture of models at several levels of abstraction, including:

- Intermediate level: semi-ideal circuit models, including timing behavior, parasitics and other electrical characteristics.
- Transistor level: actual circuit simulation with physical device models.
- Post-layout: extracted circuit models from a physical chip layout.

Cadence and Matlab recently introduced a cross-link capability that allows Cadence components to be simulated within Simulink models. Thanks to this new capability, all transistor-level component designs can be tested within the Simulink system framework.

Simulink • Plasma and probe models. • Control logic. • Performance/Accuracy analysis. Cadence Verilog-AMS • Behavioral component models. • Mostly ideal circuit models. • Isolate non-ideal behaviors. Incisive Simulator • Physical circuit simulation. • Functional verification of transistor-level schematics and physical layouts.

Figure 2: Levels of abstraction and tools used for functional verification of the PIP chip design.

By maintaining a top-down environment throughout the design process, we can fully quantify the precision of the PIP's impedance measurements across its entire spectral range. Precise impedance measurements were not necessarily the primary goal of previous PIP instrument designs, which were typically interested in locating resonance frequencies and could tolerate uncertainty in the absolute impedance magnitude (e.g. Steigies²). Our PIP design is intended to support a new generation of plasma instrumentation and research in which precise impedance measurements will be essential for studying an expanded set of plasma characteristics.

CONCLUSIONS

In this paper, we have outlined the electronic system design for a fully-integrated Plasma Impedance Probe using the FFT technique. By using matched ADCs to sample the probe's current and voltage signals, we have decreased the instruments sensitivity to variations in the probes stimulus waveform.

The sensitivity to transient spikes, that proved troublesome in previous designs, has been improved by using the FFT technique. Further, integrating the analog components on a single chip miniaturizes the system and allows the customization of key components, thereby increasing the overall system efficiency.

Acknowledgments

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References

- 1. Blackwell, D.D., Walker, D.N., and W.E. Amatucci, "Measurement of absolute electron density with a plasma impedance probe," Review of Scientific Instruments, 76, 023503, January 2005.
- Steigies, C.T., Block, D., Hirt, M., Hipp, B., Piel, A., and J. Grygorczuk, "Development of a fast impedance probe for absolute electron density measurements in the ionosphere," J. Phys. D: Appl. Phys., vol. 33, pp. 405—413, 2000.
- 3. Hummel, A., "The Plasma Impedance Probe: a Quadrature Sampling Technique," M.S. Thesis, Utah State University, Logan, UT, 2006.
- 4. Sanderson, W., "The History and Dynamics of the Plasma Impedance Probe," M.S. Thesis, Utah State University, Logan, UT, 2007.