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Probe Bus Avionics Unit Development and Validation

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ABSTRACT

The THEMIS project, a NASA MIDEX program managed by the University of California at Berkeley, was launched in February 2007 and was the first NASA mission to launch five science satellites simultaneously. The low power requirements and tight volume constraints of the mission were the major drivers with the design of the Bus Avionics Unit. The Bus Avionics Unit performs the functions of a primary Bus computer, Communication I/O interface, and Power Control Electronics for the satellite. It consists of five modules, consumes less than 6.4 watts, and weighs only 2.8 kg. This optimized design was a major enabler for this mission due to its compact design and low power consumption.

INTRODUCTION

The Time History and Macroscale Interactions during Substorms (THEMIS) project, a NASA MIDEX program through the University of California at Berkeley (UCB) principal investigator team, requires the placement of five spinning satellites, or Probes, into eccentric Earth orbits. Aggressive Probe mass and power requirements drove the Bus Avionics Unit implementation to use low power electronics design and a highly efficient packaging concept. The Mission requirements, in conjunction with the instrument design drove the Bus Avionics to be magnetically clean.

This paper will focus on the specification and development of the five modules discussing the top-level block diagram and interfaces to the UCB-developed Instrument Data Processing Unit (IDPU). Of particular interest to the small satellite community will be the means of reducing power consumption in the unit. The paper will discuss the methodology for verifying the modules and the flow of the modules from the manufacturer to their build up at Swales. In addition to the unit development of the BAU, a number of BAU test sets where built up to support testing at multiple locations. The Test Set design was critical in streamlining the verification process. We will also discuss our Engineering Unit usage and how these units were used to support Integration and Test activities at both Swales and UCB. Finally, the paper will discuss the verification of the Bus Avionics and how this was achieved in a very short time period.

BUS AVIONICS REQUIREMENTS

The driving requirements for the Bus Avionics design were: low power (7 watts), high reliability (2 year mission life), 66 krad total dose tolerance, and the need to be magnetically clean. These requirements directly influenced the selection of EEE parts and the electrical design. Low-voltage CMOS devices were predominately used throughout the design, a custom DC/DC converter design was required, parts were selected with 100 krad TID tolerance where possible, and Single Event Effects (SEU & SEL) were addressed.

Flight Software reuse and the utilization of a real-time operating system were important factors in the selection of the processor. A trade was performed to select a processor that would meet the Program's C&DH requirements while consuming less than 3 watts of power. It was determined early on that the popular Rad750 platform was not appropriate for this system due to power and size constraints. The 8085 microprocessor was deemed inadequate because of demanding Flight Software requirements. The radiation-hardened ColdFire RH5208 was finally selected for its high level of integration, large addressing space, and the availability of a real-time operating system. The ColdFire-based Digital Processor Module formed the central core of the BAU implementation, incorporating the Sun Sensor interface, Solid-State Recorder Bulk Memory, IDPU interface, and high-speed DMA controller on a single module residing on the top of the BAU stack.

The Bus Avionics Unit integrates the functionality of the C&DH and Power subsystems into a single unit and provides the following functionality:

- Spacecraft Computer
  - Provides command processing and telemetry gathering functionality
  - Performs power management functions
- Bulk Memory
  - Provides storage for 1 orbit + 1 day's worth of housekeeping telemetry
  - Record and playback data simultaneously
- Uplink Command Processing
  - Performs uplink commanding functions (1 kbps uplink rate)
  - Provides hardware-decoded command functionality
- Downlink Formatting
  - Formats real-time telemetry and stored data into telemetry transfer frames
  - Routes transfer frames to downlink channel according to priority
  - Generates CRC bytes and performs Reed-Solomon encoding
  - Supports from downlink data rates from 1.024 to 1048.576 kbps
- Telemetry Acquisition
  - Digital telemetry
  - 14-bit Analog telemetry
    - 18 Current telemetry points
    - 16 Voltage telemetry points
    - 32 Thermistor telemetry points
    - 16 PRT telemetry points
- Power Control
  - Provides Battery Charge Control functionality
  - Provides High Current actuation functionality
  - Distributes power to Spacecraft loads
  - Hard Short Overcurrent protection
  - Provides Propulsion Bus Safety Inhibit

BUS AVIONICS UNIT OVERVIEW

The Bus Avionics Unit (BAU) consists of three separate sub-assemblies: the Digital Processor Module, the Communications Interface Module, and the Power Electronics Unit. The three modules are interconnected via a custom back panel assembly.

Digital Processor Module

The Digital Processor Module (DPM) is the core of the THEMIS Bus Avionics Unit. As the central spacecraft processor the DPM is responsible for coordinating all other onboard subsystems. The DPM hardware provides the following functionality:

General

- RH5208 ColdFire Processor operating at 16 MHz
- 512KB Main Memory (Static RAM)
- 512KB Program Memory (EEPROM)
- 16KB Startup ROM (PROM)
- 64MB Bulk Memory (SDRAM)
  - FSW utilizes triple voting scheme for EDAC protection
- System Timing & Synchronization

Interface

- Digital Sun Sensor interface
  - Consists of a Sun Pulse signifying the instant that the sensor is in direct view of the Sun, and an interface representing the angle of the Sun to the face of the sensor
- Thruster Command interface
  - Controls the inputs to the Thruster output drive circuitry residing in the Power Electronics Unit
- Control and Status interfaces
  - Two independent interfaces between the DPM and the CIM and PEU modules used to send commands and receive telemetry
- Downlink Telemetry interface
  - Consisting of one Telemetry Enable signal, eight Telemetry Data signals and one Synchronization bit used to send downlink telemetry data between the DPM and CIM modules

- Instrument Data Processing Unit interface
  - A Command / Telemetry interface implemented with a UART operating at 38.4 kbps, a System Timing interface consisting of an 8.388 MHz System Clock and 1PPS signal, and a High Speed Data interface capable of operating up to 2.1 Mbps
- Test interfaces
  - The DPM contains test interfaces used during ground testing for FSW loading and debug activity

Figure 1 contains a block diagram showing DPM module functionality.

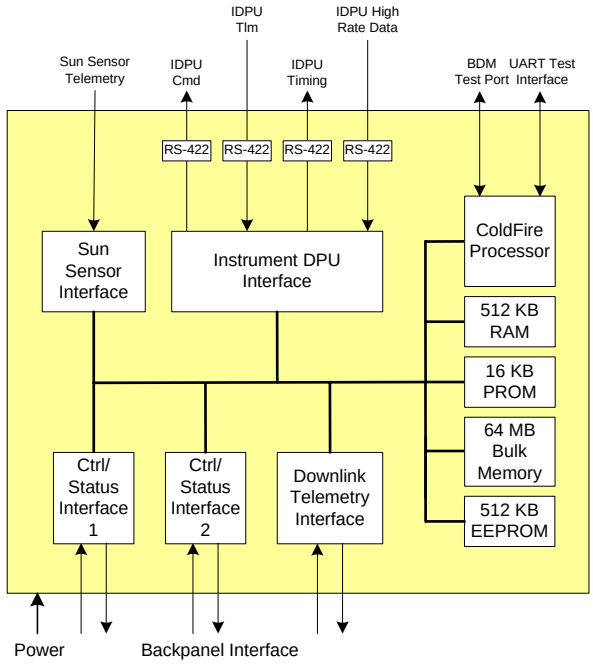

Figure 1: DPM Module Block Diagram

Communication Interface Module

The Communication Interface Module (CIM) provides Uplink and Downlink processing, as well as hardware command and DPM watchdog functionality for the BAU as follows:

General

- Receives and distributes uplink commands
- Downlinks real-time telemetry, stored housekeeping telemetry, and science data through the transponder
- Formats downlink data as CCSDS Version-1 Transfer frames implementing Reed-Solomon and using a fixed size downlink frame of 1264 bytes
- Implements downlink transfers using rates of 1024, 4096, 8192, 16384, 32768, 65536, 131072, 262144, 524288, and 1048576 bps
- Implements watchdog timer function to monitor DPM module operation, autonomously executing a Processor Reset upon watchdog timeout
- Receives, distinguishes, verifies, executes, and distributes up to 16 hardware decoded commands

Interface

- Autonomously switches between independent Uplink Transponder and Hardline command interfaces
- Provides High and Low rate downlink interfaces to the S-band transponder and a separate Hardline telemetry interface
- The primary functions of the CIM module are to process Uplink commands, monitor the DPM processor, provide hardware decoded commanding, and format Downlink telemetry.

Figure 2 contains a block diagram showing CIM module functionality.

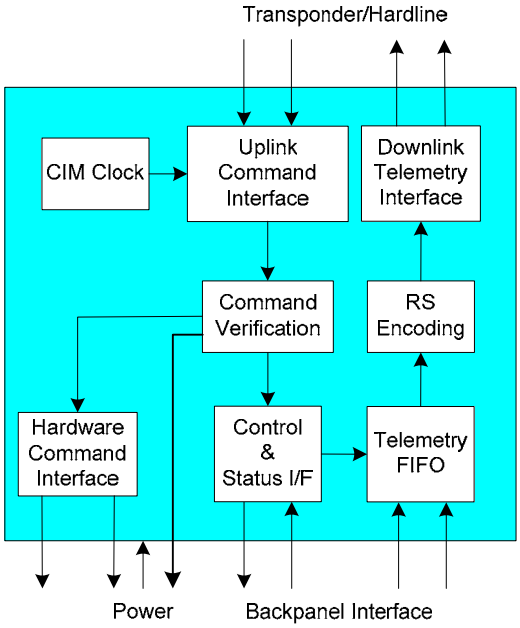

Figure 2: CIM Module Block Diagram

Power Electronics Unit

The Power Electronics Unit (PEU) functionality is distributed between three separate modules:

- The Power Control Module (PCM) interfaces to the DPM for receiving commands and transferring data. It also distributes primary and secondary power and pulse commands to bus components and the IDPU
- The Array Control Module (ACM) contains solar array power processing circuits, thermistor / PRT conditioning circuits, pressurant tank control circuits, and power distribution circuits for the IDPU and the transponder
- The Power Regulator Module (PRM) contains the DC/DC converter that generates secondary voltages. It provides pulse commands and power services for the Reaction Control System (RCS) and contains battery and bus voltage telemetry processing circuits

The Power Electronics contains the following functionality:

<u>General</u>

- Processes solar array power
- Controls battery charging
- Distributes primary power to probe components, bus heaters, and the IDPU
- Generates and distributes secondary power within and external to the BAU
- Distributes pulse commands
- Collects and processes telemetry data
- Performs propulsion control functions
- Provides hardware ACS Watchdog Timer

<u>Interface</u>

- EPS Interfaces
  - Solar Array inputs, 6 PRT inputs
  - Battery power I/Os, Linear Shunt I/Os
  - 1 analog input, 2 digital inputs, 2 thermistor inputs
- ACS Interface
  - MSSS +5v power output
  - IRU +5v/-5v switched power outputs
  - IRU rate, temperature inputs
- Transponder Interface
  - 2 - 28V power outputs
  - 12 pulse command outputs
  - 11 analog telemetry inputs, 6 digital telemetry inputs, 2 thermistor inputs
- IDPU Interface
  - 2 - 28V power outputs
  - 2 digital inputs, 4 thermistor inputs
- RCS Interfaces
  - 5 - 28V power outputs
  - 4 Latch Valve pulse command outputs
  - 4 Thruster fire command outputs
  - 1 Pyro fire command output
  - 3 analog telemetry inputs, 5 digital telemetry inputs, 13 thermistor inputs
- Thermal Interfaces
  - 7 Heater power outputs
  - 10 thermistor/PRT inputs

A block diagram of the Power Electronics Unit is shown in Figure 3.

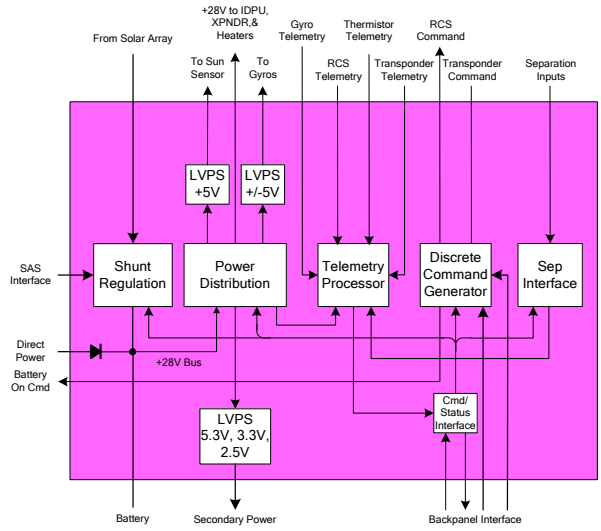

Figure 3: PEU Module Block Diagram

BUS AVIONICS PACKAGING

While many spacecraft bus avionics implementations consist of separate C&DH and Power electronics boxes, the stringent THEMIS probe mass and power requirements dictated the need for a single, integrated Probe electronics assembly. A single assembly minimized the inefficiencies in providing separate chassis, DC/DC converters, and support electronics for separate boxes.

To minimize the overhead involved with a rigid backplane / plug-in card approach, a slice concept was used. Instead of designing a separate chassis, the modules became the chassis, forming a solid five module stack. The final implementation outperformed expectations reducing the overall mass to 2.8 kg. The BAU dimensions are 8.4”L x 5.9”W x 4.7”H. The BAU packaging implementation is shown in Figure 4.

Figure 4: Bus Avionics Unit

DESIGN VERIFICATION

Developing a new avionics design and verifying that it meets requirements prior to going into the production of flight units is challenging. Building and testing five flight units in parallel, each at a different level of testing, creates scheduling issues. In addition, Flight Software development performed in parallel results in a continuous competition for resources. Addressing these issues requires multiple copies of Engineering Development Units, Test Sets, and associated equipment and cabling. Maintaining multiple versions of the same equipment requires discipline in controlling the different configurations.

The development of BAU hardware was divided into two separate developments: the DPM/CIM modules and the Power Electronics Unit. The DPM & CIM EDU modules were integrated with a special version of the PCM module to form a test bed to support Flight Software and Ground System development. To the Flight Software, this “Mini-BAU” performed just like a BAU without the telemetry capability residing in the PEU module. A large portion of Flight Software and Ground System development was completed successfully using this test environment.

The Power Electronics Unit development utilized PCM, ACM, and PRM EDU modules interfaced to a custom piece of test equipment that emulated the DPM Command/Status interface. Since both development activities occurred in parallel, contention was minimized and we were able to integrate FSW to the integrated BAU EDU on schedule. After the first EDU was integrated successfully, a second EDU was built and tested and placed on the Test Set development task. In this way, Flight Software development and testing continued unabated, Test Set development continued, and the BAU design was validated so Flight Unit production could commence.

TEST SET IMPLEMENTATION

The design of the BAU Test Set was crucial to streamlining the verification process. The Test Set was developed in parallel with EDU verification and the EDU was utilized to verify the Test Set implementation. The Test Set is comprised of components from the individual module-level test sets with additional functions to meet the Box-level test requirements. Flight Software was utilized to enhance the Test Set capabilities and provide valuable verification of the Flight Software functionality in a Flight-like environment.

The BAU Test Set was designed to support BAU Flight Unit testing in five testing environments:

- Bench Level Module Testing
- Bench Level Box Testing
- Vibration Testing
- Thermal Vacuum Testing
- Electromagnetic Compatibility Testing

Coordinating the testing of five separate BAU flight units through different test environments required the use of multiple test sets and cabling configurations. The logistics of managing the testing of several flight units at once was a challenge. Careful coordination and scheduling of test facilities and equipment to minimize the moving of test sets between facilities proved to be the key to successful testing. Three complete BAU Test Sets were built, all interchangeable, and each capable of being configured for any of the five test environments. The Test Set implementation is shown in Figure 5.

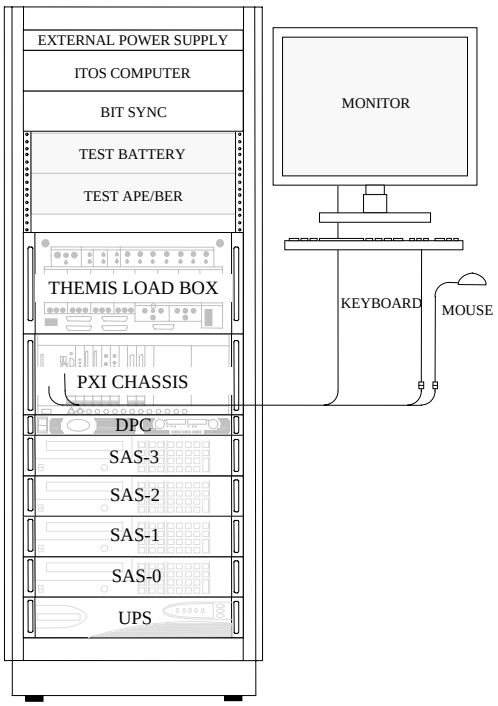

Figure 5: Bus Avionics Unit Test Set

FLIGHT UNIT ASSEMBLY & TEST

With the BAU design validated through EDU testing and the designs updated for flight, production began for Flight Unit 1. The plan was to first build up one set of modules and verify the final implementation, then build and test the next four sets of the flight modules in an assembly-line fashion. A spare set of parts for an entire sixth unit had been procured to support a timely recovery from assembly or testing anomalies resulting in the loss of all or part of a module.

The DPM, CIM, and PEU modules were identical to one another so that they would be interchangeable in case there were problems with a module during test. Individual modules were assembled and tested in a parallel fashion. After completing Module-level testing, the modules were integrated together for Open Frame functional testing. The modules were staked and conformal coated, then integrated together in a stack configuration for the initial Box-level Performance test. After completing this test all box hardware was closed out and the box proceeded to Environmental testing and Probe I&T. The BAU Flight Unit assembly and test flow is shown in Figure 6.

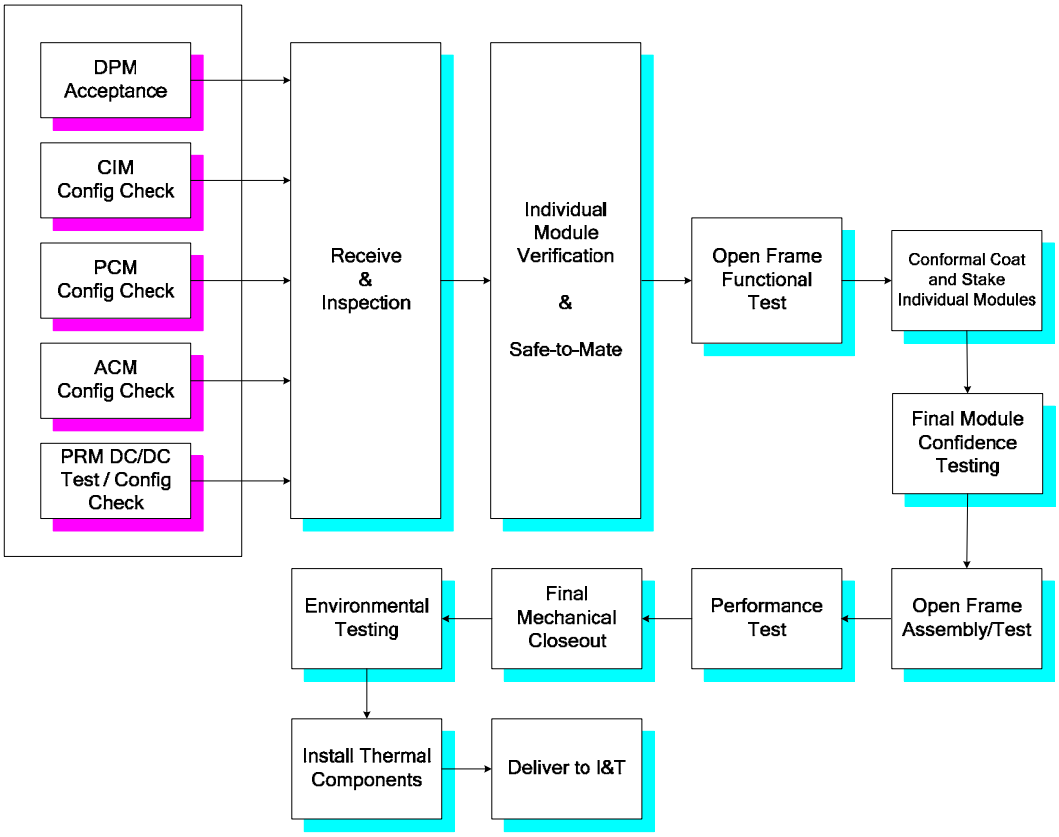

Figure 6: BAU Flight Unit Assembly & Test Flow

CONCLUSION

The THEMIS Bus Avionics Unit design met all of the requirements and goals of the THEMIS mission. The BAU implementation came in well under its mass and power allocation budget, weighing less than 3 kg and consuming less than 7 watts. Combining the entire C&DH and Power subsystem electronics with this level of performance into such a highly efficient package is a feat in itself. Five identical Bus Avionics Units were built, assembled, tested, and integrated in a timely manner in support of Program requirements.

Acknowledgements

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