Solar Cell Measurement System for NPS Spacecraft Architecture and Technology Demonstration Satellite, NPSAT1

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Abstract

Rapid changes in semiconductor technologies over the last decade have spawned new interest in developing higher efficiency solar cells which are capable of using a broader part of the light spectrum. The Naval Postgraduate School's NPSAT1, launching in the Spring of 2006, will include a subsystem which can be used to measure the performance of the new solar cells, providing an ability to combine functions previously available on only individual discrete components onto a single chip. The ability can help make space more accessible by reducing cost and complexity.

The Solar Cell Measurement System (SMS) is a radiation hardened microcontroller based system using a radiation hardened FPGA that drives and monitors a collection of sun angle sensors, temperature sensors, a current sink/differential amplifier circuit combination for each of the 22 test cells and 2 control cells to be used in the experiment. The test cells are Triple Junction InGaP/GaAs/Ge cells and the control cells are Dual Junction cells. Triple Redundant Analog-to-Digital Converters, Digital-to-Analog Converters, and memory and interrupt logic will be implemented in the FPGA. The error budget developed for the circuits predicts a maximum error of 0.28%. The controller provides a common controller architecture for NPSAT1's Electrical Power System and Attitude Control System. Future versions of the system will be able to further reduce costs by implementing a processor core into the FPGA.

Introduction

The Solar Cell Measurement System (SMS) is an experiment by the Naval Postgraduate School Space Systems Academic Group (NPS SSAG). The SMS experiment has the mission of measuring current and voltage characteristics of experimental triple-junction cells and will provide IV curve data at measured temperatures and sun angles. Data points will be measured with a maximum of two percent error. A total of 22 triple junction cells and two commercial dual junction cells comprise the test specimens. The commercial dual junction cells will be used as control for the experiment.

Background

The Naval Postgraduate School Satellite (NPSAT1) is a technology demonstration satellite that provides educational opportunities for students at the Naval Postgraduate School and is an experiment bus for integrating experiments. NPSAT1 currently holds nine experiments, seven of which are being developed by the Space Systems Academic Group. NPSAT1 is one of 5 satellites on the STP-1 mission scheduled for launch on a Delta IV in 2006. NPSAT1 will be injected into a circular orbit of 560 km and 35.4 degrees inclination, providing for an orbital period of 95.8 minutes, or about 16 orbits per day.

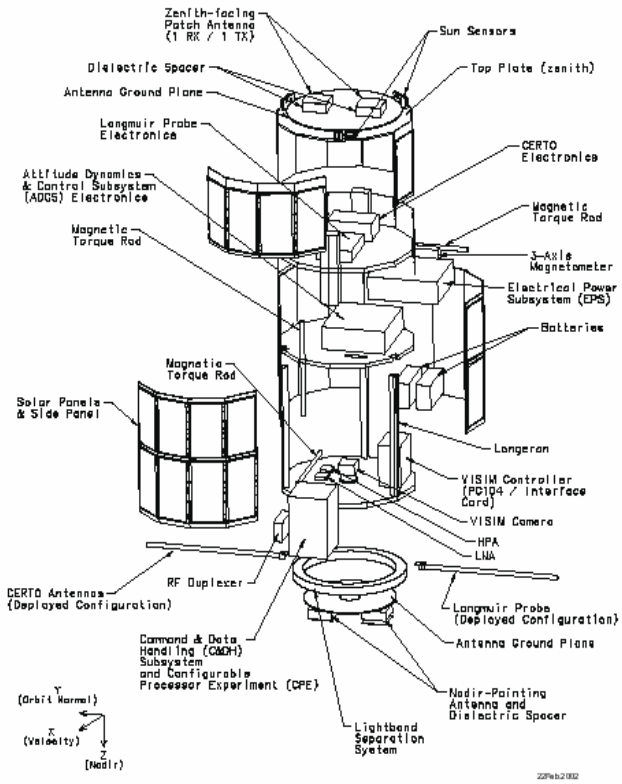

Figure 1. NPSAT1 Expanded View Diagram

In the last ten years, solar cell manufacturers have made great strides in improving cell efficiency and power production. Multi-junction cells with greater than 28% efficiency are now commercially available. In a multi-junction cell, layers of different materials and doping levels are used to extract energy from different portions of the light spectrum, converting more of the spectrum into power. Below is a diagram of a Boeing Spectrolab Improved Triple Junction (ITJ) cell showing the multiple layers grown on the Germanium wafer.[1]

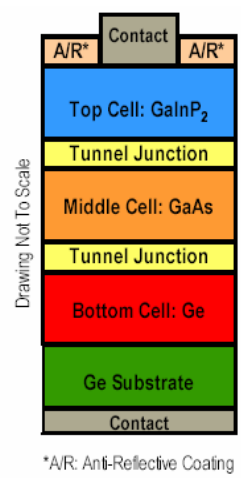

Figure 2. Triple Junction Solar Cell Layer Diagram and Electrical Model[1]

The following parameters are used to characterize solar cells; short-circuit current (I_{SC}), open circuit voltage (V_{OC}), maximum power point (P_{MAX}), efficiency (Eff_{MP}), and fill factor (Cff). These parameters can be

determined by an accurately measured IV characteristic curve of the solar cells. The IV curves are, however, a snapshot of the cell's performance at a given temperature and solar angle, requiring adjustments that will be covered later. Below is a typical IV curve for an ITJ cell as supplied by Spectrolab in the ITJ cell datasheet. [1]

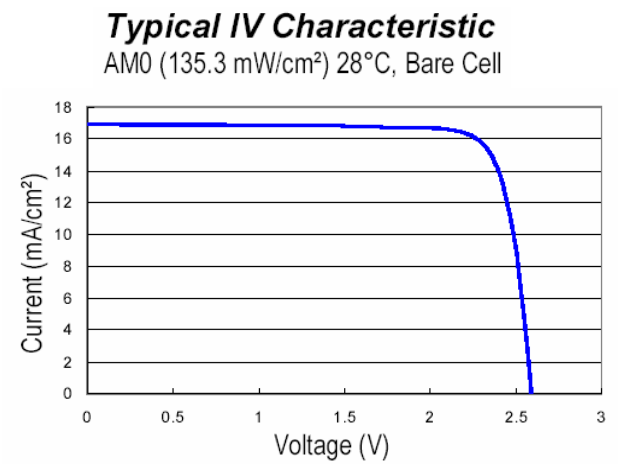

Figure 3. Triple Junction Cell Typical IV Curve

From the sample curve above the Voc is 2.565V and Isc is 16.9mA. The maximum power point is at 2.27V and 16.0mA, giving a fill factor of 0.84 and efficiency of 26.8%. The energy available from sunlight in space is referred to as Air Mass Zero (AM0). In space at 1AU, the photons contain 1.353kW/m^2. The cell information provided in Figure 3 is for a 1cm^2 x 1cm^2 cell. From this we can calculate the Fill Factor (Cff) and Efficiency at the maximum power point (Eff_{MP}) of the solar cell. The calculations are shown below. [2]

$$Cff = \frac{P_{MAX}}{V_{OC} \times I_{SC}} = \frac{2.27V \times 16.0mA}{2.565V \times 16.9mA} = .84 \qquad (1)$$

$$Eff_{MP} = \frac{P_{MAX}}{AM0 \times Area} = \frac{.03632W}{(.1353W/cm^2) \times 1cm^2} = 26.8\% \qquad (2)$$

System Development Process

The Solar Measurement System consists of three major subsystems, each with their own design flow peculiar to the type of hardware and software being developed. This section describes how these are developed and integrated together. Figure 4 shows the basic layout of a single solar cell and its interface with the data converters and system controller. The SMS is comprised of three subsystems. First is the analog cell measurement circuit. It is made up of curve tracing hardware for each solar cell, a temperature sensor and associated hardware for each pair of cells and sun angle sensors with hardware. The solar cell and temperature signals are multiplexed into the data converters and the sun angle signals have dedicated data converters. The second subsystem is the data converters and the third is the microcontroller. Each of these subsystems will be discussed in detail.

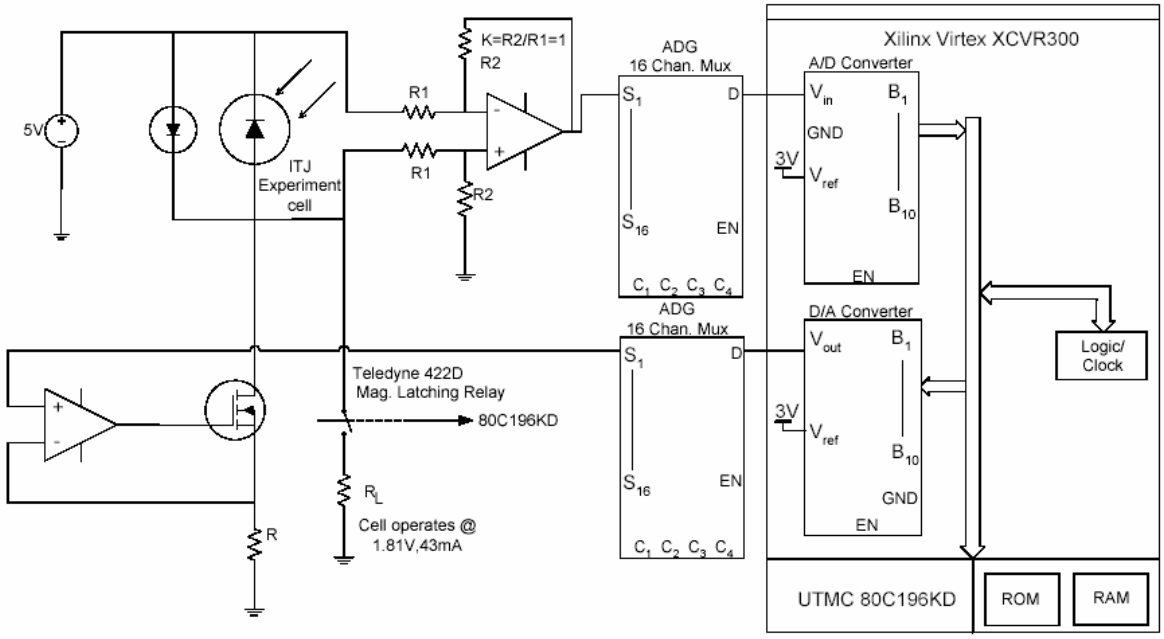

Figure 4. SMS Basic Block Diagram

Parallel Design Approach

The approach used to design the SMS is adapted from a process used by DaimlerChrylers' air bag system designers.[3] Their designs integrate microcontroller based systems using Field Programmable Gate Arrays (FPGAs) to integrate the controller with the analog sensors. The process, illustrated below, begins by determining system requirements, followed by a system level simulation which allows the design concept to be tested and further refined. This approach is especially appropriate since the SMS combines a microcontroller based system that contains an FPGA that interfaces with the analog sensor circuitry. The diagram shows the next steps, where the analog, controller and FPGA go through there design iterations, validated against the initial interface simulation and then combined at the end. The interface requirements for the SMS were developed during the summer and fall of 2002 while the system design was researched and various parts were simulated along with the initial development of a system level simulation.

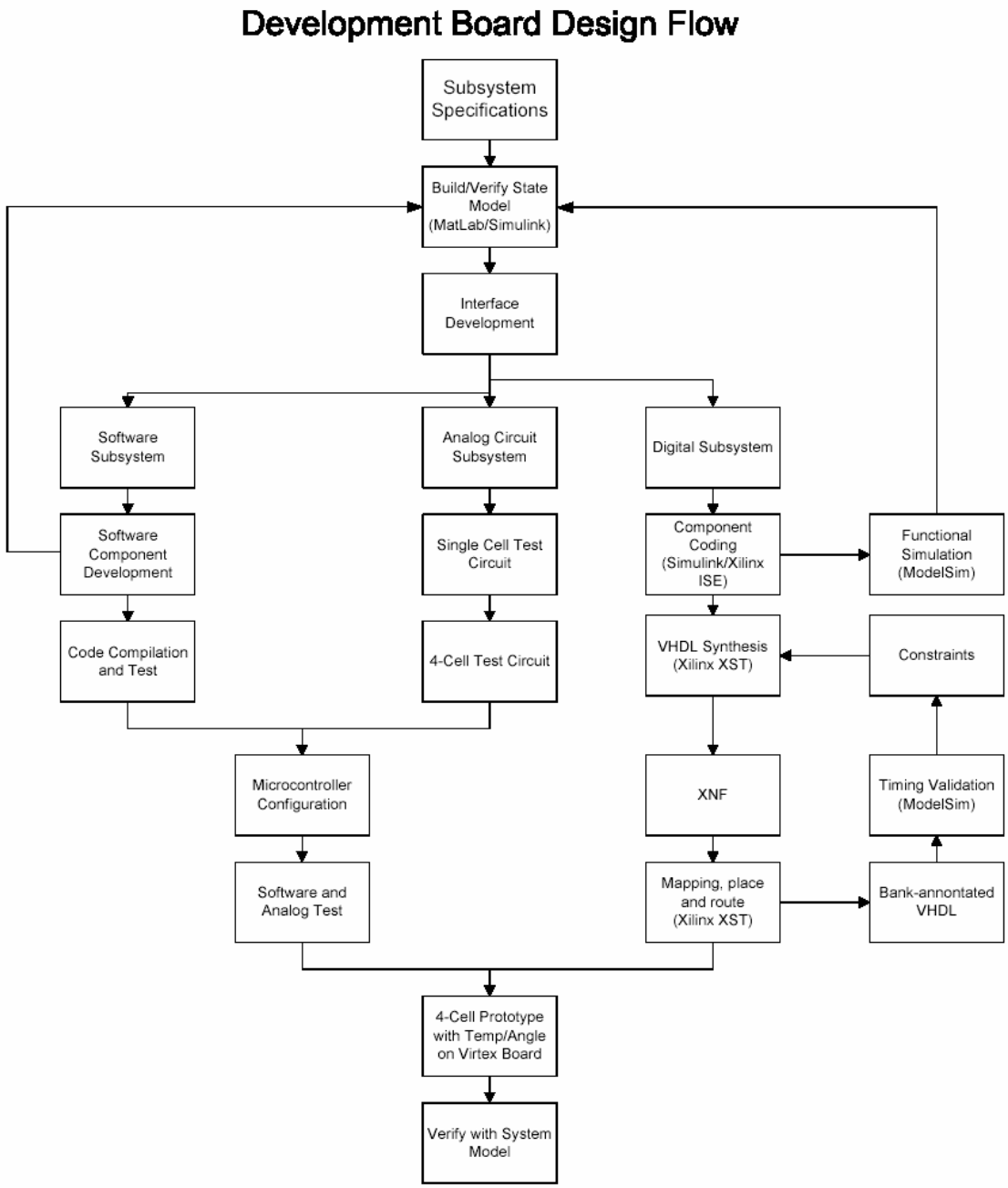

Figure 5. Development Board Design Flow[3]

System Level Simulation

MATLAB Simulink and Orcad PSpice simulations of the design were developed to provide a better understanding of the component functions and interfaces within the SMS. The design is based on the original circuit concept developed in a 1988 Thesis by Oxborrow.[4] With the use of a Xilinx System Generator Toolkit, the analog system portion of the design can be combined with the FPGA-based data converter circuit and a basic controller softcore provided in the toolkit. While this will not be a fully accurate

simulation of the analog circuit and flight controller, this process will be invaluable in the design of the FPGA. Functionality incorporated into the FPGA includes data converters, registers for storing converted data and decode logic for the controller memory and interrupts.

Analog Circuitry

Initially analog circuit simulations where created in Orcad PSpice. The PSpice simulation of the current sink design provided the basis for choosing component types for the design. The design developed in the Oxborrow thesis used a Bipolar Junction Transistor (BJT) with an operational amplifier to create the current sink.[4] Simulations showed that better control of the current was possible with an N-channel enhancement mode MOSFET over the other possible types of transistors, contributing to the experiment goal of less than 2% error on the measurements taken.

Data Converters

All analog systems which manipulate and read sensors require data conversion devices. And while conversion devices such as Digital-to-Analog Converter(DAC) and an Analog-to-Digital Converters (ADC) are available as discrete components (IC's) with multiple channels, 2.5V radiation hardened FPGAs are also available which can provide the data conversion capability of multiple discrete converters. Xilinx provides a Verilog based design for a DAC and an ADC in Xilinx Application Notes 154 and 155, respectively.[5,6] In addition, the DAC and ADCs in the SMS are designed to be Triple-Modular-Redundant (TMR) so as to increase Single Event Upset (SEU) tolerance. As can be seen from Figure 4, the FPGA design flow has its own internal iterations prior to integration with the rest of the system. The use of the Simulink toolkit has proved invaluable in ensuring the signals meet interface requirements.

Controller

As shown in Figure , the development of the microcontroller's embedded software is fully integrated into the SMS design process. The Xilinx Simulink toolkit contains a PicoBlaze™ microcontroller core with similar pin level interfaces as the Intel-based controller to be used in the SMS. This will allow a simulation of the interfaces within Simulink and provide an initial test of their functionality. Once the interfaces are verified, we will use several commercially available tools to assist in the development of software for the system. The first is a system development environment by IAR Systems. This workbench and compiler is specifically configured for the Intel 196 processor family and works directly with the Intel 196 development board. Additionally we will use a Nohau in-circuit emulator with the flight board.

Analog Circuit Design

The solar cell measurement circuit shown in Figure 6 below consists of a current sink circuit and differential amplifier. An n-channel MOSFET transistor, operational amplifier and 0.005% tolerance resistor (with a 2ppm temperature coefficient) are combined to create the voltage controlled current sink. A high input impedance instrument amplifier is used to measure the solar cell voltage. Setting a voltage at the input of the current sink amplifier and knowing the value of the current sink resistor makes it possible to set the current level being supplied by the solar cell. For each current setting the differential amplifier is used to read the voltage across the solar cell. An entire IV curve can be traced by setting the current sink to various current levels and then measuring the cell voltage, as shown in Figure 7.

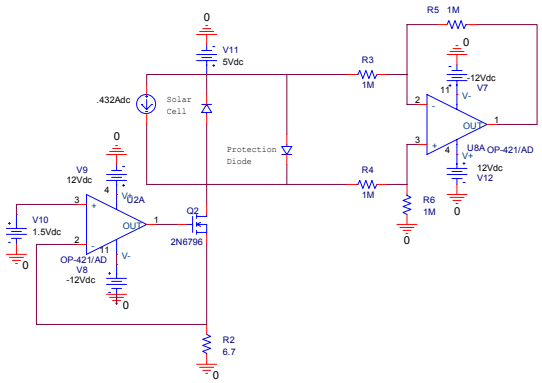

Figure 6. Initial Single Cell Circuit

The current sink resistor value is determined by dividing the maximum input voltage (maximum input voltage of the DAC), by the short circuit current of the solar cell. Given the short circuit current of each cell which is known at a normalized temperature, the current sink circuit will be designed to handle the maximum short circuit current for each of the two types of solar cells. Included in this calculation are the effects of highest and lowest expected temperatures which have been determined by thermal analysis. The circuit is designed to have the input voltage sweep the solar cell current through several points along its characteristic curve. As the current is swept the voltage across the cell is read and paired with the current calculated from the voltage and resistor value. Data gathered for each curve includes solar cell temperature, solar angle and time.

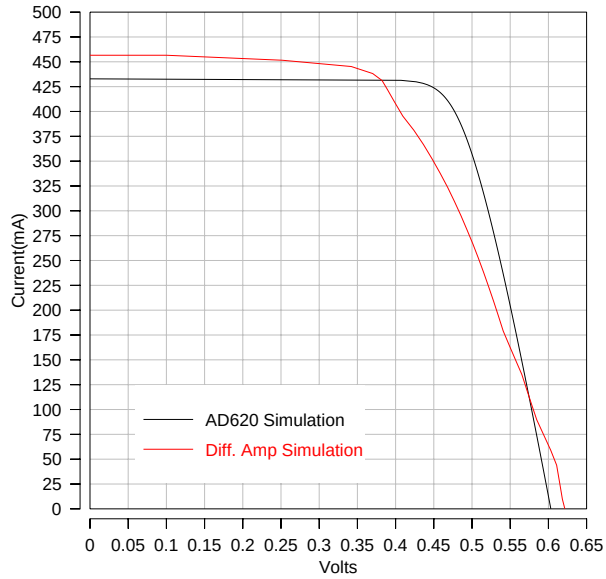

Figure 7. Orcad SPICE IV Curves from the Circuits in Figures 6 and 10.

The voltage across the solar cell is measured by a differential amplifier. The diode is a low threshold diode that ensures the solar cell is not damaged due to reverse biasing as we measure the short circuit current of the solar cell. While reverse biasing a silicon cell is not of great concern, reverse biasing of multi-junction cells can cause irreparable damage. Based on consultations with the solar cell manufacturers, a reverse bias of about 0.15V (the threshold of the protection diode) will not damage the cell. The importance of this becomes apparent when you study the IV curve of a solar cell. This circuit sweeps along the curve from V_{OC} to I_{SC}. The slope of the curve above the knee is very flat; increasing the cell current by tenths of a milliamp when above the knee of the curve, the cell can reverse bias.

Testing of the first development board for the analog circuit is complete and the second development board is in production. The development boards contain circuitry to test four solar cells and two temperature sensors as if it were testing two of the twelve panels on NPSAT1. Also included on the development

board are sun angle sensor interface circuitry and reference voltages to provide calibration points for the data conversion. Each circuit, simulation, error budget and test results will be discussed.

First Development Board

Tests were conducted to verify the accuracy of measurements by the curve tracing circuits. The first tests were made on a bread board circuit to verify that the circuit worked as designed. Then a board was laid out and built. The tests of this first board concluded that the circuit performed in line with the error budget. Additional error was found in the wiring from the solar cell to the circuit. Additionally, the solar cell bias voltage, placed in the design to help protect the cell from reverse biasing, introduced error into the circuit. The results of these tests are shown in Figure 8.

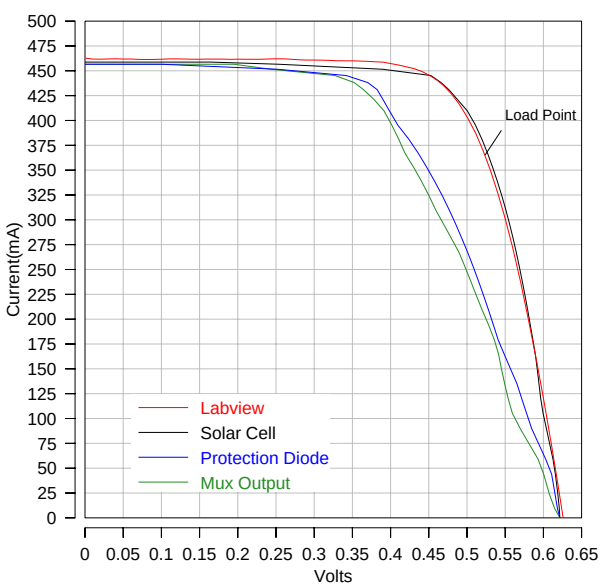

Figure 8. Silicon Cell Test IV Curves

The figure shows four IV curves of the same solar cell. The solar cell is a 2cm x 4cm Silicon cell tested under an Optical Radiation Corporation Solar Simulator 1000 with a 1600W Xenon bulb. The first curve is from a test system with a HP6626A power supply controlled by a LabView system. The second curve is from the solar cell circuit with the solar cell voltage read at the leads to the solar cell. The third is also from the circuit with the solar cell voltage read across the protection diode on the board. Notice the drop in voltage from the leads to the cell. This will be further studied in the next round of tests, so the voltage drop can be better predicted. Additionally, the flight cells have a higher voltage range reducing the effect of the voltage drop on the overall error. The last curve shows how the differential amplifier affects the error of the voltage readings. A summary of the results is shown in Table 1. The IV curves are used to give the Fill Factor and Efficiency of the solar cell as shown earlier. The wire voltage drop causes most of the error of almost 20%, but is predictable and can be adjusted in the final computations. The error of the differential amplifier is about 1.75%, or almost double of that shown in the error budget in Table 2. We attribute this difference to a small voltage drop from wiring at the output, from the 5V solar cell bias causing a floating voltage error, and the silicon cell has a V_{OC} of only 0.63V. Notice the similar shape of the circuit output with the shape of the differential amplifier output in Figure 7.

Table 1. Development Circuit 1 Test Summary

	Open Circuit Voltage (V)	Short Circuit Current (mA)	Maximum Pwr Point (mW)	Fill Factor	Fill Factor Error	Efficiency	Efficiency Error
LabView							
At Cell	0.6258	462.6983	204.6429	70.67%	----	18.91%	----
Circuit							
At Cell	0.6215	460.2668	205.2108	71.74%	1.51%	18.96%	0.28%
At Diode	0.6215	458.7442	164.7816	57.80%	-18.22%	15.22%	-19.48%
At Output	0.6215	458.7442	160.2025	56.19%	-20.49%	14.80%	-21.72%

The next round of tests, once the new board is ready with the updated solar cell circuits, will work through a set of data readings to include an IV curve, temperature and sun angles controlled by a LabView routine interfacing with the board via a data Input/Output card. This will work to verify the analog board operation.

While testing it became apparent that the differential amplifier design for the IV curve trace circuit was critical to insuring accurate readings of the solar cell voltage. During testing it was found that errors in measurement increased from less than 1% to over 7% at the knee of the IV curve. Further testing indicated that to reduce the error, impedance of the difference amplifier had to be increased and the resistor gain pairs must be matched to within 0.01%.

It was also found during testing that resistance values need to be very high (1M) and the values of the resistors need to be matched. Resistor tolerances as large as 2% can cause errors of up to 12% difference in the amplifier inputs. This is shown in the calculation below.

$$V_{out} = \frac{R2}{R1}V^{+} - \frac{R4}{R3}V^{-} \qquad (3)$$ [7]

With 2% tolerance resistors and input voltages of 2V and 1V, the output is calculated as follows:

$$V_{OUT} = \frac{1.02\text{M}\Omega}{0.98\text{M}\Omega}(2\text{V}) - \frac{0.98\text{M}\Omega}{1.02\text{M}\Omega}(1\text{V}) = 1.12\text{V} \qquad (4)$$

As the bias for the solar cell increases, so does the error. In this circuit, with a solar cell bias of 5V, the maximum output error using the .1% tolerance resistors is .98% or 25.1mV when using an ITJ cell; or 3.37% or 21.3mV when using a silicon cell

An error budget for the IV curve trace circuit was developed based on a process outlined in Analog Devices Application Note 539 (AN-539). This budget is shown in Table 1. Originally, the largest potential errors identified resulted from resistor gain pair mismatches for the differential amplifier design. Careful resistor selection minimizes this effect, focusing the remaining error on the current distortion from the current sink and the floating voltage effect from biasing the solar cell. The error budget for the development boards is shown below.

Table 2. SMS Solar Cell Circuit Error Budget

Error Source	Development 1 Circuit Calculation	Development 1 Total Error (ppm)	Development 2 Circuit Calculation	Development 2 Total Error (ppm)
12-bit Analog-to-Digital Converter	**FPGA Based ΔΣ**[5] ((1 - EXP(-1 / (freq*tau))) * ((1 - EXP(-((2^bits)-1) / (freq*tau))) / (1-EXP(-(2^bits) / (freq*tau)))) * 2^bits)	170.62	**FPGA Based ΔΣ** ((1 - EXP(-1 / (freq*tau))) * ((1 - EXP(-((2^bits)-1) / (freq*tau))) / (1-EXP(-(2^bits) / (freq*tau)))) * 2^bits)	170.62
Current Sink OpAmp ABSOLUTE ACCURACY at T_A=+25ºC Input Offset Voltage, mV Input Offset Current, nA CMR, dB Gain DRIFT TO +85ºC Gain Drift, ppm/ºC Input Offset Voltage, mV/ºC RESOLUTION Gain Nonlinearity, ppm of Full Scale Typ 0.1Hz-10Hz Voltage Noise, 40nV/√Hz	**OP421F**[9] 3.5mV/3V 8nA x 250Ω/3V Vcm/Vsig*Gain/(Alog(110dB/20)) int + ext 10µV/ºC x 60ºC/3V 50 ppm 40nV	 1166.67 .78 0.80 0 0 200 50 0.04	**OP497F**[10] 150µV/3V .2nA x 250Ω/3V 125ppm x 3V/3V int + ext 10µV/ºC x 60ºC/3V 50 ppm 40nV/3V	 50 .02 0.17 3.98 0 200 50 0.01
Current Sink FET 2N6796 Channel Resistance Channel Resistance Drift	**OP421F Error** Not a factor since voltage Set across resistance	**1588.95**	**OP497F Error** Not a factor since voltage Set across resistance	**375.71**
Current Sink Resistor Absolute Tolerance @ T_A=+25ºC Resistance Drift, 2ppm/ºC	**2N6796 Error** .1% Tolerance Resistor 1000 ppm 50 ppm x 60 ºC	**0** 1000 3000	**2N6796 Error** .005% Tolerance Resistor 50 ppm 2 ppm x 60 ºC	**0** 50 120
	Total Resistance Error	**4000**	**Total Resistance Error**	**170**
	Total Current Error	**5588.95**	**Total Current Error**	**545.71**
Voltage Sense Circuit ABSOLUTE ACCURACY at T_A=+25ºC Input Offset Voltage, mV Output Offset Voltage, mV Input Offset Current, nA	**OP421F – Diff Amp, 1MΩ, .1% Tol**. 3.5 mV/ 2.57V unk 8 nA x .5MΩ / 2.57V	 1320.75 389.11	**AD620, Reference at Neg. Input**[11] 50 µV/ 2.57V 500 µV/ 2.57V .5 nA x 250Ω / 2.57V	 47.17 389.11 0.14 194.55

CMR, dB	5V * 1 / (Alog(78dB / 20))	244.93	5V / 2.57V * 1 / (Alog(80dB / 20))	200
Gain	((1+tol)/(1-tol))-((1-tol)/ (1+tol)	4000	200 ppm	
DRIFT TO +85ºC				600
Gain Drift, ppm/ºC	50ppm /ºC	3000	10 ppm /ºC	14
Input Offset Voltage, mV/ºC	10 µV/ºC x 60ºC/2.57V	233.46	.6 µV/ºC x 60ºC / 2.57V	<.01
Input Offset Current, pA/ºC	unk		1.5pA / ºC x 60ºC / 2.57V	163
Output Offset Voltage	unk	0	7 µV/ºC x 60ºC / 2.57V	
		0		
RESOLUTION				40
Gain Nonlinearity, ppm of Full Scale	50 ppm	50	40 ppm	0.01
Typ 0.1Hz-10Hz Voltage Noise, nV/√Hz	40nV/2.57	0.02	13 nV / 2.57V	
	OP421F Error	**9238.27**	**AD620 Error**	**1647.98**
Comparator input to ADC	**AD790**[12]		**AD790**	
MAX ERROR AT FULL TEMP RANGE				
Offset Voltage, mV	.5 mV / 2.57 V	194.55	.5 mV / 2.57 V	194.55
Offset Current, nA	200 nA x 300 Ω / 2.57 V	23.35	200 nA x 300 Ω / 2.57 V	23.35
CMR, dB	0V * 1 / (Alog(88dB / 20))	0	0V * 1 / (Alog(88dB / 20))	0
Hysteresis Effect	.5 mV / 2.57V	194.55	.5 mV / 2.57V	194.55
	AD790 Error	**412.45**	**AD790 Error**	**412.45**
12-bit Analog-to-Digital Converter	**FPGA Based ΔΣ**[5]	**170.62**	**FPGA Based ΔΣ**	**170.62**
Freq = 80MHz Tau = .003 (RC LP Output Filter) Bits = 12	((1 - EXP(-1 / (freq*tau))) * ((1 - EXP(-((2^bits)-1) / (freq*tau))) / (1-EXP(-(2^bits) / (freq*tau)))) * 2^bits)		((1 - EXP(-1 / (freq*tau))) * ((1 - EXP(-((2^bits)-1) / (freq*tau))) / (1-EXP(-(2^bits) / (freq*tau)))) * 2^bits)	
	Total Voltage Error	**9821.34**	**Total Voltage Error**	**2231.05**
	Grand Total Error	**15410.29 or 1.54%**	**Grand Total Error**	**2776.76 or 0.277%**

Further tests of the board were made to find out the extent of the effects of resistor matching and the solar cell voltage biasing. The 2 cm x 4 cm Silicon cell was loaded with a 1.54Ω resistance to put the cell near the knee of the curve as shown in Figure 8. The differential amplifier was configured with 1MΩ resistors hand matched to a 0.1% tolerance and tests resulted in error readings of 7.9%. The maximum theoretical error is 31.3mV or 4.96%. Individual parts of the circuit were isolated and tested to locate the cause of the additional error. Testing was conducted using 1 MΩ resistors with better than 0.82% measured tolerance and matched to better than 0.11%, the differential amplifier gave an error of 1.07%. Further tests will be conducted with triple junction cells to determine if the error is consistent and can be lowered. Performing this test with the silicon cell is difficult since varying load points along the IV curve require changing the load resistance by fractions of an ohm. The open circuit voltage of the triple junction cell allows this range to expand to about 30 Ω, making it easy to test a range of load points. The conclusions so far are that the large errors observed in the full circuit are only partially due to the resistance variation in the differential amplifier. The majority of the error is from the effects of biasing the solar cell.

Second Development Board

During testing it was found that the prototype IV curve trace circuit has maximum errors which are too large. A design change was initiated to provide buffers at the inputs of the differential amplifier to limit the effects of the solar cell biasing. To reduce the errors the differential amplifier circuit will be replaced with an instrumentation amplifier (in amp), the AD620B, shown in Figure 9. Notice that the in amp contains input buffers, high-impedance input differential transistors and an output reference. The in amp allows the gain to be set with an external gain resistor. In this circuit, a unity gain is used, so the gain resistor pins are not connected. The instrumentation amplifiers are available in small packages and reduce the overall component count.

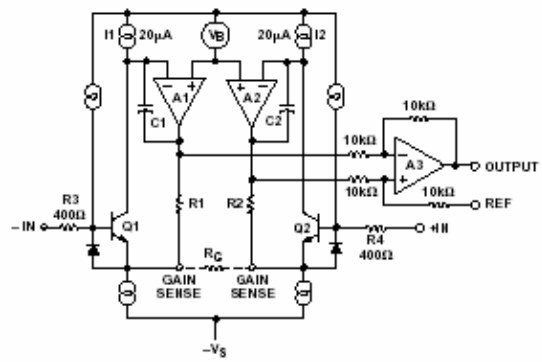

Figure 9. Instrumentation Amplifier Simplified Schematic[11]

Equation (5) describes an instrument amplifier. [7]

$$V_{OUT} = (V_{IN}^{+} - V_{IN}^{-})(\frac{2R_1}{R_G} + 1)(\frac{R_3}{R_2}) \qquad (5)$$

This equation applies to the AD620, the in amp we are using, by making R1=R2=24.7kΩ and R4=R3=10kΩ. The resistors in the AD620 are laser trimmed to ensure matching to 200 parts-per-million as shown in Table 2. This simplifies into equation (6). [11]

$$V_{OUT} = (V_{IN}^{+} - V_{IN}^{-})(\frac{49.4\text{k}\Omega}{R_G} + 1) \qquad (6)$$

with $R_G=\infty$, the gain is simply the difference between the inputs.

A second design change was made to further reduce errors. This change was to the current sink circuit where the Analog Devices OP471FY operational amplifier is replaced with an Analog Devices AD497F. This was necessary as the OP471 has a very high output offset voltage which was responsible for a large percentage of the measurement error.

The new single cell circuit is shown in Figure 10. The important parameter for the current sink amplifier is a very high common mode ratio to keep the voltage at the input terminals as close as possible and very high input impedance to minimize the voltage drop across the analog multiplexer. The last modification was to change current sink resistor to one with .005% tolerance and a very low 2 ppm temperature gradient to ensure cell current is accurately controlled.

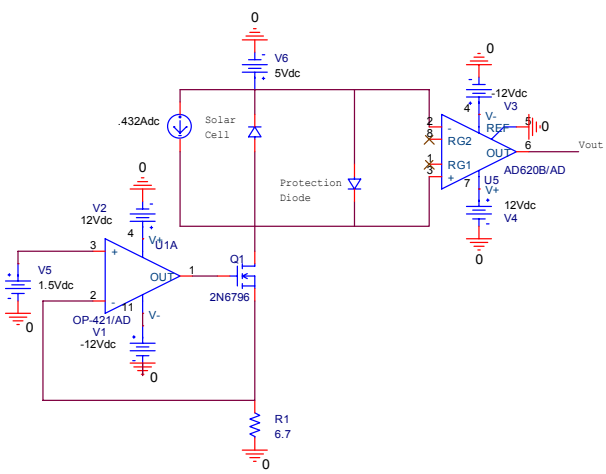

Figure 10. SMS Single Cell Analog Circuit for a Silicon Cell

The redesigned circuit yields an improved error budget. Table 1 also shows the error budget for the updated circuit. With this predicted error, the overall error, before normalization from temperature and sun angle, will be a maximum of 0.28%. The error calculations for the temperature and sun angle circuits are shown in the next sections.

Temperature Sensor and Sun Angle Sensors

Temperature

Each temperature sensing circuit employs Omega 40088 thermistor, voltage reference and an operational amplifier to form a constant current source. The voltage across the thermistor is read by the ADC and converted by software to give the temperature with a precision of +/-1˚C. As a matter of procedure, the temperature is taken at the beginning of each IV curve sweep. The normal mode of operation for the system will wait for a stable temperature once out of eclipse before IV curve sweeps are taken. Future operations will include IV curve measurements as the spacecraft exits eclipse in order to obtain solar characteristic gradients by temperature. The standard temperature for solar cell measurements is 28˚C. The predicted temperature range for the solar cells on the mission is -25 to 35˚C. Current and voltage characteristics are reported by the manufacturer to change by about 6mV/˚C and 7.3mA/˚C.[1] IV curves can be normalized to the standard temperature to (1) verify this specification and (2) provide information on the performance of the cells since they will not always be at 28˚C.

The design of the temperature sensor circuit was successfully used on PANSAT, an earlier NPS satellite, and was functionally tested in February 2003. Empirical tests will be conducted in June 2003 with the completion of the second development board to determine the accuracy of the measurements. The maximum calculated error for the current circuit design will add 0.15% to the IV curve data points. The error is based on the solar cell circuit, using the comparator and ADC errors with the 1% thermistor maximum error rated by the manufacturer.

Sun Angle

Solar cell predicted performance is determined by the angle of incidence, shown here by equation (7).[2]

$$E_{sun} = \cos(\Gamma_{sun}) \times .1353 W / cm^2 \qquad (7)$$

This simplified version of the calculation given in the Solar Array Design Handbook illustrates the basic effect of sun angle on the

performance of the solar cell. An important part of the SMS experiment is the requirement to measure the difference between the normal surface vector and the sun angle vector. The cell becomes less efficient as this difference increases. To measure this effect the SMS will perform curve sweeps on all illuminated test cells with an angle to the sun less than 60 degrees from normal. At some point in the mission the SMS experiment operations may include curve sweeps at angles up to 80 degrees. The upper limit on the maximum sun angle will be determined from tests under a solar simulator with the fully verified analog circuitry which includes sun angle sensor interface circuits. The present goal is to determine the largest angle that gives measurable results.

Six Goodrich sun angle sensors will be integrated onto NPSAT1. Pairs of these sensors will be placed as shown in Figure 1, spaced evenly around the circumference of the top of the spacecraft to give 360 degrees radial measurements and +/-64 degrees elevation measurements.[13] The sensors in each pair are placed orthogonal to each other to give the 2 axis readings. The angle for each cell will be calculated from the measurements of the two brightest light sensors (since there will always be at least one pointed away from the sun). Only those cells within the predetermined angle from normal will have sweeps taken to avoid taking measurements of non-illuminated cells. The flight sensors are calibrated by the manufacturer and can provide accurate angle measurements to +/-0.1 degrees. With the current circuit design, this gives an additive maximum error for the IV curve of 0.15%. The sun angle sensors circuit design is complete and is part of the analog development board. A non-flight sensor will be used to verify the analog interface.

Microprocessor and Data Convertor Design

Microcontroller Overview and Configuration

The SMS is a microcontroller based NPSAT1 experiment subsystem that controls temperature and sun angle sensors while collecting solar cell IV curve data. All collected data is sent on to the NPSAT1 main processor, the Command and Data Handler (C&DH). A limited amount of processing will occur in the SMS which will be described later in this paper. The processor selected for the SMS is the Radiation Hardened UTMC 80C196K. A processor based on the Intel 80C196KD microcontroller. The 196 provides 32-bit processing capability with a 16-bit Error Detection and Correction (EDAC) and four ports that can be configured to provide the designer excellent design flexibility. Processor development is supported by available design environments, development boards and emulators to help ensure proper software control and integration. The processor contains a Universal Asynchronous Receiver Transmitter (UART) serial port for its command interface with the C&DH. Memory is limited to 64KB address space, with 32KB reserved to on-chip memory and registers. The memory hardware will be space rated memory using 16-bit and 8-bit memories, decoded through an FPGA. Part of the memory space will be mapped to the data converter registers in the FPGA to help simplify the architecture. An FPGA Input/Output (I/O) port will be used to strobe the ADCs reading the sun angle sensor signals so they can be read simultaneously, helping ensure the sun angle measurement accuracy. Due to the configuration load delay for the FPGA, the processor startup sequence includes a wait for the DONE signal from the FPGA. This ensures availability of the processor memory when it boots up. Embedded software development consists of

the IAR Systems design environment, a Nohau in-circuit emulator and Intel development board.

A reprogramming capability is being designed into the SMS so that either an entire test routine or portions of a test routine can be changed on orbit. The reprogramming is accomplished by loading new software images into SMS system RAM. A new program image for the SMS will be transmitted to NPSAT1 which will be held in the C&DH's mass memory storage. Then when the SMS is powered up the C&DH sends the new RAM image to the SMS followed by a jump command to the appropriate memory start location of new RAM image. It is expected that at a minimum, this process will be used to make modifications to test parameters. Another possible technique would be to reprogram the system and FPGA PROMs in flight, however, the FPGA design will be finalized prior to flight. Reprogramming the controller ROM in flight introduces unnecessary risk into the project and the NPS staff is confident of its RAM changing technique.

Data Converters

FPGA overview

FPGAs provide the capability to reduce board space requirements since it is possible for the designer to program into one FPGA device the functionality of multiple discrete components. With next generation FPGAs it will be possible to implement either one single large processor or smaller processors in a triple modular redundant configuration (TMR) with microcontroller sized memory, decoding logic and DSP accessories in a single chip. Use of this technology in subsystems aboard NPSAT1 will allow the staff to gain experience in designing and implementing FPGA-based circuits for the next NPS satellite.

For the SMS a stand alone Digital-to-Analog Converter (DAC) and seven Analog-to-Digital Converters (ADCs) together with chip interface "glue logic" will be implemented in a radiation hardened FPGA. For design verification two tools are available to perform simulation of the FPGA based circuits prior to empirical testing. The first, System Generator, a Xilinx tool, is a Simulink toolkit which makes it possible to simulate the design and design interfaces with external components to ensure proper integration. This Simulink based design is then converted to Very High Speed Integrated Circuit Hardware Description Language (VHDL) and can be opened directly into the Xilinx XST design environment for Synthesis, Translation and loading into an FPGA. It also creates test benches which can be used to test the circuit in the second tool by Model Technology. ModelSim allows the designer to follow all of the signals through the FPGA system to ensure their proper propagation through the FPGA. It also allows the designer to introduce SEUs into the system to test the fault tolerance of the design.

A properly functioning DAC design has been verified both in Simulink and in hardware and the DAC design has also been converted into a TMR design. The initial TMR DAC was simulated successfully in Simulink. The major limitation of this simulation is that clock and power signals are not simulated. After simulation the design is converted to VHDL for use in Xilinx XST design software. From there, further triple modular redundancy is extended to the clock and power signals. A schematic of the TMR DAC is shown in Figure 11. The SMS design will be tested in the ModelSim simulator followed by testing in hardware. The same steps will be taken to design the ADC and interrupt and memory control logic for the microcontroller.

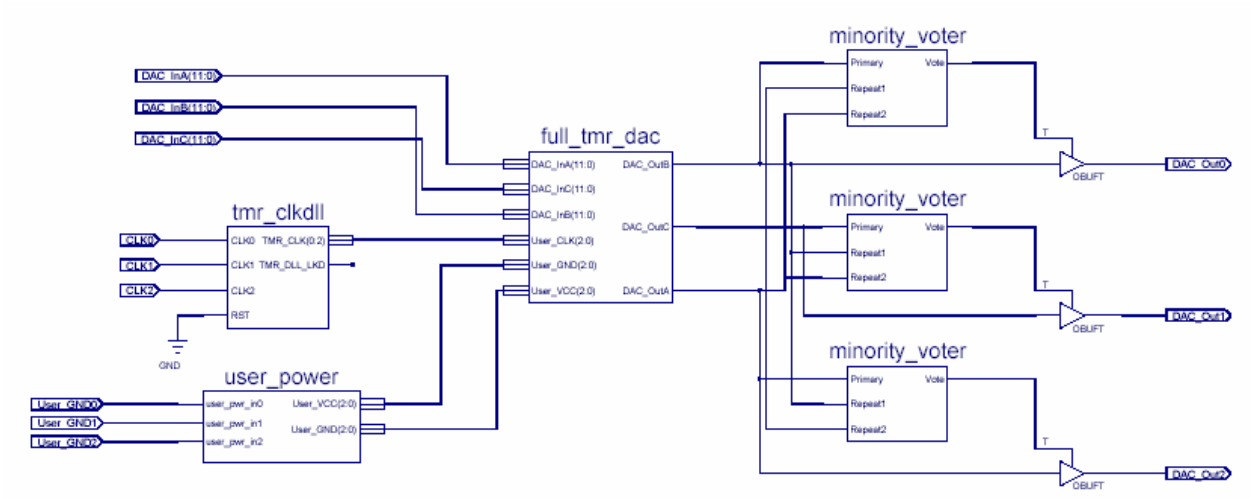

Figure 11. TMR DAC as a Stand Alone System

SEU Tolerance

FPGAs can provide additional utility to digital circuit designers. They allow the designer to build in SEU tolerance in two ways. The first is by employing multiple layers of Triple Modular Redundancy. The SMS is a good example of how these techniques can be used in a smaller design. Secondly, designs may also use a technique called reconfiguration, where the programmed configuration of the FPGA, if altered by a single event upset (SEU), can be corrected with a very limited load on the FPGA duty cycle.

Triple Modular Redundancy

Triple Modular Redundancy is the most common Fault Tolerant Design technique.[14] FPGAs now allow the designer a much simpler method to implement a TMR design. Application Note 197 from Xilinx (XApp 197) provides an algorithm and specific techniques on how to design a TMR circuit at the logic component level.[15] Synplicity's Synplify Pro, a digital logic synthesis tool, currently provides an automated version of this logic as a feature when using Actel's FPGAs.[16] Xilinx's XST version of this implementation for Xilinx's FPGAs is currently in development and takes a design post-synthesis and converts it to a TMR design at the netlist level using the philosophy presented in XApp 197. Tripling of the signal lines also includes the clock and power signals. Since SEUs are not limited to the normal signal paths, an SEU on a single power or clock line could stop a circuit until the configuration of the FPGA is recycled. This technique allows the circuit to keep running and correct itself on the fly.

Reconfiguration

Reconfiguration is a technique that reads current configuration bits of an FPGA, compares them with those loaded in the system configuration PROM and if there is a difference, corrects the program in the FPGA logic block which has the error. Partial reconfiguration is a type of configuration that allows an FPGA to be corrected without reconfiguring the whole chip. A state machine implemented in another device can cycle itself through all of the logic blocks on the FPGA to correct configuration errors as they occur. A simpler technique forces the FPGA to reload its configuration through the whole chip, called a scrub. Addressed in Xilinx Application Note 216, the partial reconfiguration technique uses a different type

of configuration PROM and uses a more complicated design, but does not require the whole FPGA to shut down.[17] It can be done periodically or continuously, depending on the orbit environment.

Due to the orbit of NPSAT1, SEUs in the SMS will be rare, especially considering that the SMS will be on only about 64 minutes a day. The design of a Partial Reconfiguration state machine will begin in July 2003. A final decision on the reconfiguration implementation technique will be made in September 2003 after further research is conducted. At this time, the scrubbing technique is expected to be used since it is simpler and the SMS will not be in a high risk environment for SEUs. However, partial reconfiguration is an option for the Attitude Control System (ACS) and Electrical Power System (EPS) since they are powered on continuously. Research on the partial reconfiguration technique is in tandem with the Configurable Fault Tolerant Processor experiment, another NPSAT1 experiment employing FPGAs, and will be used to determine the best configuration for those systems.

Using the Data

The primary purpose of this circuit is to collect data on the solar cells. The basic elements of data will be a timestamp to correlate on the ground, orbit location data from the Attitude Control System (ACS) to the location of the satellite at the time the curve sweep was performed, and also to correlate the test cell temperature, and sun angle.

IV Curves

IV curves, temperature and sun angle measurements, provide all of the data needed to characterize the cell. The endpoints of the IV curve are short circuit current and open circuit voltage. At the knee of the curve is the maximum power point, where the user wants the cell to be operating to provide the most efficient power generation. Fill factor provides a metric of the quality of the cell and is roughly calculated as a ratio of the location of the maximum power point to the product of I_{SC} and V_{OC}. Efficiency of the cell will also be calculated and is another cell metric to show how much of the photon energy entering the cell is converted to electricity. Figures 2 and 3 show a typical ITJ cell and the data collected for the IV curve.

Temperature Conversion

Typical cells have an average temperature gradient graph showing how cell IV curve characteristics change vs. temperature. According to Spectrolab's datasheet, an ITJ cell has a -6 mV/degrees C gradient, meaning the voltage across the cell drops 6mV for each degree Celsius the temperature of the solar cell increases. It also increases 6mV/˚C when the temperature decreases. The current through the cell has a gradient of 7.9mA/˚C.[1] Normalizing an IV curve based on a cell temperature means that each data point is adjusted based on the difference of temperature measured and the standard 28˚C.

Sun Angle Conversion

The algorithm to determine the sun angle at each cell based on the voltage readings from each sun sensor has yet to be determined. Goodrich provides the calculation to convert the voltage sensed from the sensor to an angle. This voltage from each sensor will be sent in the telemetry data so the calculation will be done during ground based processing. At least one pair of sensors will not be illuminated by the sun due to their configuration on the satellite. The calculation will most probably use the converted angles from the illuminated sensors in the

calculations given by the Solar Array Designers Handbook similar to equation (7).

Conclusions

Based on the current design, the SMS will measure solar cell IV curve data with a required precision of 2% maximum error. Future advances in FPGA technology will allow the digital portions of the system design to be implemented using less board area while simply scaling the analog portion to the number of solar cells and/or panels to be measured. However if panels are to be characterized, care must be taken in the design to account for switching large voltages associated with taking solar panels on and off line in flight. Additionally, scaling of the voltage readings may need to be done to work with data converters; and high current power devices need to be used to sink panel currents.

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