The Electronic System Design, Analysis, Integration, and Construction of the Cal Poly State University CP1 CubeSat

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ABSTRACT

Picosatellites demand highly efficient designs. Restricted in mass, volume, and surface area, the design of these spacecraft is particularly challenging. The electronic systems of CP1, the first satellite developed at Cal Poly State University, are designed specifically with simplicity and efficiency in mind. The satellite's design conforms to the CubeSat standard, also developed at Cal Poly in conjunction with Stanford University.

Designed and built by Cal Poly Students, the main printed circuit board (PCB) is the center of the electronic systems of CP1. This PCB incorporates the command, data handling, data acquisition, and power electronic systems.

The bus systems of CP1 are designed to accommodate numerous commercial payloads. Highly efficient bus systems allow 30% of the spacecraft's mass, volume, and power to be budgeted for payloads. This capable platform can be used to develop and flight test numerous new technologies such as microthrusters, magnetorquers, MicroElectro-Mechanical Systems (MEMS), and a variety of sensors.

This paper outlines the objectives and requirements of the mission and describes how those requirements are met in the design. The integration of the electronics with the structure and primary payload, as well as the fabrication and assembly methods employed, and modifications for in-orbit operations are covered.

Additionally, the design is analyzed to determine potential weaknesses in functionality or reliability and test results are presented to provide a characterization of the electrical and functional properties of the spacecraft.

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1. INTRODUCTION

1.1 CubeSat Project Overview

Started in 1999, the CubeSat Project is a collaborative effort between California Polytechnic State University, San Luis Obispo, and Stanford University's Space Systems Development Laboratory. The objective of the project is to provide a standard platform for the design of picosatellites. A common deployer is used, significantly reducing cost and development time and enabling frequent launches. This allows multiple high schools, colleges, and universities from around the world to develop and launch picosatellites without having to interface directly with launch providers.[1]

Currently, Cal Poly is designing, fabricating, and testing deployers, called Poly Picosatellite Orbital Deployers (P-PODs), capable of deploying up to six CubeSats each. Cal Poly is also working closely with Stanford on the identification and coordination of launch opportunities, thus allowing CubeSat developers to focus entirely on the design, construction, and testing of their satellites.

The CubeSat standard specifies each satellite as a 10cm cube of 1kg maximum mass and provides additional guidelines for the location of a diagnostic port, remove-before-flight pin, and deployment switches.[2] The purpose of the specification document is to ensure that each satellite will integrate properly with the deployer and neighboring satellites within the deployer and will not interfere with neighboring satellites or, more importantly, the primary payloads or launch vehicle.[3]

1.2 PolySat Project Overview

The Cal Poly Picosatellite Project (PolySat) involves a multidisciplinary team of undergraduate and graduate engineering students working to design, construct, test, launch, and operate a CubeSat. CP1, the first satellite developed at Cal Poly, is designed with the objective of providing a reliable bus system to allow for flight qualification of a wide variety of small sensors and attitude control devices. Possible payloads include microthrusters, magnetorquers, MicroElectroMechanical Systems (MEMS), magnetometers, and numerous other devices originating from industry, government, or internally from other research projects conducted at Cal Poly. For the first launch, CP1 carries a sun sensor developed by Optical Energy Technologies and an experimental magnetorquer developed at Cal Poly by undergraduate students.

2. REQUIREMENTS

Mission objectives, the CubeSat design specification, the expected launch and in-orbit environments, and fabrication cost drive the design requirements for the electronic systems of CP1. The design requirements define:

- Electro-mechanical interfaces
- Environmental conditions
- Communications frequencies and modes
- Payloads the bus systems must support
- The mission objective and duration

The class of components, fabrication techniques, system architectures, and testing methods are left to the discretion of the student engineers.

2.1 Electro-Mechanical

For any CubeSat, the primary design requirement is that it must conform to the CubeSat standard. While the standard does not control functionally how the spacecraft operates, it does place mass and volume restrictions and specifies three electro-mechanical interfaces, which are critical to the electronic systems design.[2]

By definition, CubeSats have a maximum mass of 1kg and are cubes measuring 10cm on all sides.[2] As shown in Table 2.1, the mass budgeted for the entire electronic systems of CP1 is only 100 grams, with 350 grams budgeted for solar panels and batteries. A quantitative objective volume for the electronic systems is not defined, but it is understood that the volume available for the electronics is extremely limited, and any reduction in volume in the electronics will enable the flight of higher volume payloads.

Table 2.1 - CP1 Mass Budget

Subsystem	Budgeted Mass
Electronics	100g
Energy Collection and Storage	350g
Structure	250g
Payloads	300g

One of the electromechanical interfaces defined in the CubeSat specification is a deployment detection switch. No circuits may be energized during integration and launch.[2] Switches must physically break the circuit of all power sources until the satellite deploys. After deployment and power-up of the satellites, a delay on the order of several minutes must be provided before any device can be deployed or any transmission is made.[2] Additionally, the specification defines deployment switch location.

To disable the satellite before and during integration with the deployer, a remove-before-flight switch must be included.[2] Once the satellites are loaded into the deployer, the remove-before-flight pin is removed. Although not specified, an actual remove-before-flight pin is preferred over other devices that must be added to the satellite prior to launch, as removed pins provide a better confirmation that the spacecraft was, in fact, enabled prior to launch.

Finally, the specification defines the location of an optional diagnostics port, which allows the batteries to be charged and the electronic systems to be checked even after the CubeSats have been integrated into the deployer and qualification tested.

2.2 Launch and Orbit Environment

As with any spacecraft, harsh launch and in-orbit environments are major obstacles to the success of CP1. A key requirement in the electronic design of CP1 is its ability to endure thermal-vacuum, shock, and vibration acceptance testing at 150% of worst-case launch levels. Figure 2.1 provides a worst-case vibration profile compiled from the published environments for several launch vehicles, including the Delta II, Pegasus, Shuttle, and Dnepr.

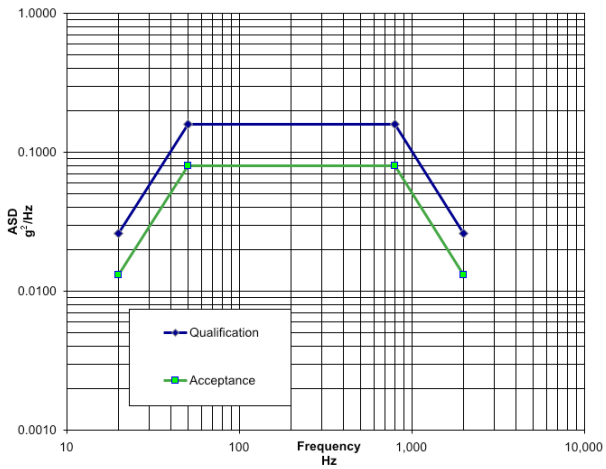

Figure 2.1 - Worst Case Vibration Environment[4-8]

For the purpose of design analysis, the following orbit parameters are assumed:

- Polar Low Earth Orbit
- Altitude of 400 to 600 Kilometers
- Orbit Period of 90 Minutes
- Eclipse Duration from 0 to 30 Minutes

While the possibility of radiation damage is considered in the design of CP1, the odds of a high-energy radiation event are assumed low, given the one-to six-month target duration of the mission. Consequently, the use of radiation-hardened components is not a priority. However, basic countermeasures against single event latch-ups, such as watchdog timers, are essential design elements.

2.3 Communications

Communications can be particularly challenging with picosatellites. For most universities, the supportive community of operators and availability of frequency privileges and equipment makes amateur radio the best solution for radio communication. The specifics of the communications system are not defined, but it is a requirement that the satellite operates on amateur radio frequencies and utilizes a communications mode common to the amateur radio community. An additional objective is that radio amateurs with satellite ground stations be able to simply and inexpensively decode telemetry data from CP1 and forward that data to Cal Poly.

2.4 Payload

Finally, payload support for a diverse group of devices is a major factor in the design requirements. The bus systems must be capable of providing ample power, digital and analog interfaces, and have the flexibility to interface to a variety of payloads. Given the mass and volume requirements of the spacecraft, the bus systems must be light and compact and consume very little power, so that these resources are available to the payload.

3. SYSTEM DESIGN AND ANALYSIS

Initial design efforts took the approach of using the same concepts and systems architecture used in 500kg commercial satellites and miniaturizing the systems to fit in the available 10cm cube of 1kg mass. The effectiveness of this approach is limited.

The key to finding innovative solutions to the design challenges in the CP1 mission involves recognizing the inherent differences between the mission profile of large commercial satellites, and that of CP1. Rather than scaling down much larger systems, a fresh approach starting from the ground up is required. In CP1, the use of software to replace hardware subsystems, the integration of subsystems to simplify the overall design, and changes in architecture eliminating traditionally essential system blocks, are all the result of this design approach.

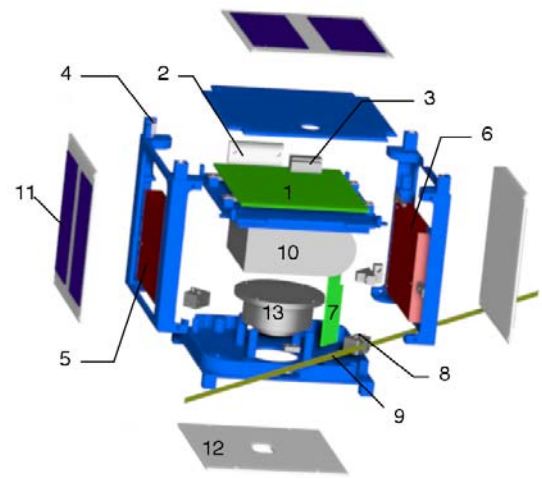

Figure 3.1 - Exploded View of CP1

Table 3.1 - CP1 System Components

1	Main PCB	8	Antenna Mount
2	Data Port Connector	9	Dipole Antenna
3	Remove Before Flight Switch	10	Battery Pack
4	Deployment Switch	11	Solar Panel
5	Transceiver A	12	Solar Panel (Sun Sensor Side)
6	Transceiver B	13	Sun Sensor
7	RF PCB		

Preliminarily, space grade components were researched. The result of this research was the realization that space grade component manufacturers are not designing for picosatellites and the vast majority of space grade components are consequently incompatible with picosatellite design.

Given the short mission duration, cost requirements, and limited development time, CP1 is constructed entirely from commercial-off-the-shelf (COTS) components. At the cost of additional risk, COTS components, compared to space-rated or radiation-hardened components, enable higher performance at a reduced cost.[9-10] The associated risk can be managed by rigorous testing and by making hardware modifications as needed. If these components are capable of surviving launch and operating in orbit for several months, their use affords highly integrated, efficient, and capable systems.

3.1 Communications

The communications system requirements specify that the satellite operate on amateur radio frequencies and utilize a communications mode common to the amateur radio community. An additional objective is that amateurs with satellite ground stations be able to simply and inexpensively decode telemetry data from CP1 and forward that data to Cal Poly.

To meet these requirements and to provide a system that is cost effective and easy to integrate with the structure, CP1 communicates on the 70cm amateur radio band and utilizes Morse code and Dual Tone Multi-Frequency (DTMF) to encode data. To simplify the design, 70cm is used exclusively and all communications are simplex. Consequently, only a single transceiver and antenna are required. Specifically, a modified Alinco DJ-C5T transceiver, shown in figure 3.2, is used. These radios are inexpensive, low power (300mW RF Output), and extremely small.

Figure 3.2 – Alinco DJ-C5T Transceiver

To provide redundancy, two identical transceivers are used, and the command computer alternates between transceivers on each communications cycle. The command computer checks the current consumption of the transceivers during transmit and receive, and has the capability to automatically disable the use of a transceiver if an over-current fault condition is identified. Additionally, if the command computer resets during transceiver operation, the fault is logged and the opposite transceiver is used for all subsequent transmissions unless commanded by ground station control. Either or both transceivers can be disabled by ground station command uplink.

To link the two transceivers to a single antenna, the RF PCB was developed. The RF PCB accepts the RF output of each transceiver, switches the two signals as commanded by the onboard computer, and provides impedance matching and balancing to the dipole antenna. Deployed using the proven method of melting nylon line with a ni-chrome heating element, the dipole antenna is constructed from measuring tape material and mounts directly to the RF PCB through a Delrin insert (See figure 3.1).

CP1 normally operates as a beacon, sending data once every three minutes. Additionally, the spacecraft can be commanded to provide a bulk data dump while within range of an authorized ground station.

A significant reduction in volume, mass, and power consumption is achieved by generating the Morse code and DTMF tones in software. This innovative approach eliminates the need for a hardware terminal node controller or modem. The microcontroller used has built-in functions for providing DTMF and single-tone signals from any digital output. Only a simple RC filter and attenuator circuit are required to deliver the audio signal to the microphone input of the transceiver.

Morse Code is used to identify transmissions, and DTMF sent at 15 characters per second is used to transmit data. Compared to modern digital modes, DTMF is extremely slow, clocking in at an equivalent data rate of 60 bits per second. The reality of the mission, though, is that high data rates are not required, because there is not a large quantity of data to be transmitted. Furthermore, it is not desirable to reduce transmission time by increasing data rates, because reducing transmission time increases the complexity of making contact during the first week of operation, the chaotic window of opportunity when the first, and often last, contact with student satellites is made.

Despite the relative simplicity of using Morse Code and DTMF, a highly efficient protocol for communicating with CP1 using these modes was devised, providing a very functional system. The communications protocol is provided to radio amateurs across the world who will be able to decode, interpret, and forward data to Cal Poly, using only their existing earth stations and a computer running tone decoding shareware downloadable from the Internet. By utilizing the existing network of radio operators, data for an entire orbit is compiled

without the need for using store and forward techniques.

An additional feature of the communications system is that the transmission duty cycle is varied by the command computer based on available power and component temperatures, to automatically balance energy consumption with collected energy and to provide some degree of thermal management.

3.2 Power Management and Distribution (PMAD)

Given the limitations in volume, mass, and energy collection capability, a new approach is used in the design of the power system for CP1. Central to this design is the use of modern COTS DC/DC converters, typically used in cell phones and personal digital assistants. These converters provide efficiencies greater than 90% and provide variable output voltages from 1V to greater than 12V for input voltages as low as 1V*. Additionally, the design is simple and requires only a few external components, all of which are surface mount. A single converter requires board space equivalent to the area of a postage stamp.

Three DC/DC converters, based on the MAX1703 controller I.C., were included in CP1. One converter provides 5V for the microprocessor and other logic level devices, while two converters provide redundant 3.6V supplies to both of the communications transceivers. To significantly improve efficiency, for loads less than 150mW, the 5V converter is configured for Pulse Frequency Modulation (PFM) Mode. With loads greater than 150mW, the 3.6V converters operate most efficiently in Pulse Width Modulation (PWM) Mode.

With DC/DC converters capable of operating down to 1V, high solar panel and battery voltages are not required. Unlike larger satellites (with longer distance power cabling), which require higher supply voltages to reduce resistive losses,[11] CubeSats are extremely compact and operating currents are quite low, so solar panel and battery voltages do not have to be as high. One downside that remains with low buss voltages, however, is that the loss in solar panel blocking diodes is more significant at lower solar panel voltages. This loss is minimized by using Shottkey diodes with 0.3V forward voltage drops, but the power loss in the blocking diode remains significant.

* Typically input voltages of greater than 1V are required for output voltages above 6V.

Table 3.2 - Battery Chemistry Comparison[12]

Characteristic	NiCd	NiMH	LiIon	LiMetal
Nominal Voltage(V)	1.2	1.25	3.6	3.0
Gravimetric Energy Density (Wh/Kg)	45	55	100+	140+
Volumetric Energy Density (Wh/l)	150	180	225+	300+
Self-Discharge Rate (% month)	25	20 to 25	8	1 to 2
Temperature Range (°C)	0 to +50	-10 to +50	-10 to +50	-30 to +55

For energy storage, lithium batteries are selected for their extremely high volumetric and gravimetric energy densities. Refer to Table 3.1 for a comparison of battery chemistries. In the search for a suitable secondary battery, one model, the PolyStor PSC340848, stood out. The cell is prismatic, measuring 8.5 x 34.2 x 48.0mm. It's mass is only 38 grams and it has a capacity of 1.2Ah. As a Lithium Ion cell, the nominal voltage is 3.6V. The PMAD system of CP1 allows these cells to be placed in parallel rather than series, to add capacity instead of voltage, providing tremendous flexibility. Depending on the profile of the mission, cells can be added or removed to satisfy the required capacity and peak currents of the mission.

This also alleviates a few of the complications in charging packs with series cells, as cell matching and cell reversal become less of an issue. On the advice of PolyStor, a custom pack was manufactured for CP1 that includes three of these cells in parallel and an integrated protection PCB.

The protection PCB prevents unsafe charge and discharge currents and disconnects the battery at low voltages to prevent over-discharge. An additional feature of the protection PCB is an integrated thermistor for monitoring battery temperature.

Quite commonly, failures in student satellites have been attributed to solar panels that fail to deploy or become damaged in flight. To extend the operational life of the spacecraft in the event of such a failure, an Electrochem Lithium Metal primary cell was added to the design. This cell is the same size as a "C" battery but the energy densities and capacity are extremely high, even when compared to Lithium Ion cells. The capacity of the cell is 7.0Ah. On launch, the satellite carries over 30Wh of energy, enough to sustain low-power operations for several weeks.

The solar cells selected for CP1 are Spectrolab Dual Junction GaAs cells with an open circuit voltage of 2.4 volts and efficiency greater than 19%. While these cells are not the most efficient available, they provide the best value, and cost is definitely an issue

in academia, as it is in industry. Electrically, two cells are placed in series, providing a nominal panel voltage of 4.2V.

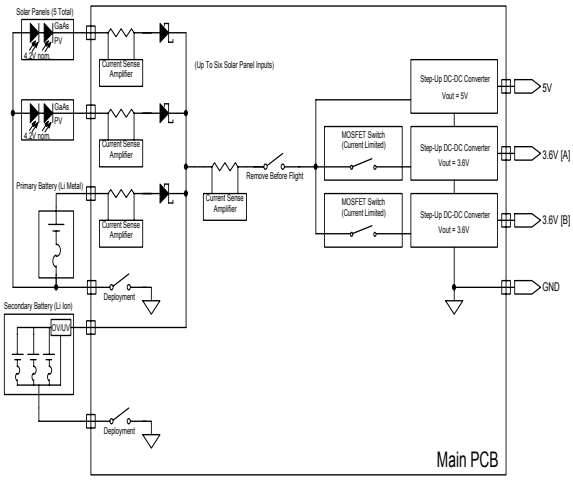

Figure 3.3 - Power Management and Distribution System Architecture

At the system level, one striking difference in the PMAD system on CP1 is the lack of charge controller, made possible by the careful choice of solar panels and secondary batteries and by the unique topology. For larger satellites, it is generally not an option to omit the charge controller.[13] Here, however, a new approach is being taken which will provide better performance during the first weeks of the mission, while the spacecraft can rely on primary energy sources. As for the long-term performance of this approach, test results under nominal conditions have been quite favorable but performance under actual conditions will not be known until flight data is collected. This approach has the potential to actually increase long-term power efficiency, simplify the design, and reduce mass and volume.

3.3 Command, Data Acquisition, Data Handling

On CP1, the Command, Data Acquisition, and Data Handling systems, are highly integrated and really quite simple. Most of the functionality of these systems is provided in software. Software solutions were provided to problems typically addressed with hardware, wherever possible without reducing the reliability or functionality of the system. While this adds to the complexity of the software, software weighs very little, requires very little space, and doesn't use much power.

The command computer is a Netmedia BasicX-24 microcomputer module. This device is similar to a Basic Stamp but has much more ram (400 bytes), much more persistent memory (32K EEPROM), and includes 16 I/O, eight of which are also analog inputs. All of this is contained on a 24-pin DIP module.

The programming environment provides a comprehensive library of high level commands and the operating system is multitasking and can perform floating-point math. This significantly reduces the learning curve and development time. At the core of this module is an Atmel 8535 RISC microcontroller running at 8MHz.

To provide diagnostic data, several temperatures, voltages, and currents are monitored. The temperature of each solar panel, of the primary and secondary batteries and of the transceiver, of the DC-DC converter, and of command computer are monitored. Additionally, the solar panel, primary battery, and secondary battery voltages and currents are monitored during several operating modes. To interface all of these analog lines to the command computer, four CD4051 analog multiplexers are used, allowing thirty-two channels to occupy only four analog inputs on the BX-24.

Several auxiliary functions are also handled by the command system. These include the acquisition of data from the payload, the electronic controls for the antenna release, and the interface for the magnetorquer.

3.4 Main PCB

Two advantages of miniaturization are the potential increase in reliability and the ease of production that results from using highly integrated systems that can be built monolithically. These advantages are apparent in the Main PCB of CP1. The Main PCB, shown in figure 3.4, is an eight-layer FR4 circuit board measuring 7 x 8 cm which includes the power management and distribution, command, data acquisition, data handling, antenna deployment control, and all other electronic systems except RF communications.

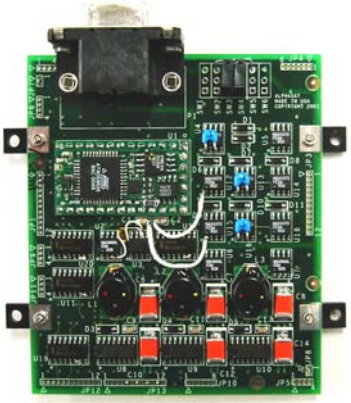

Figure 3.4 – Main PCB with Shock Mounts

Integrating many subsystems onto the same PCB greatly reduces the complexity of the wiring and it becomes practical for some components to support

several systems, reducing part count and generally simplifying the design. The Main PCB is the electrical hub of the entire satellite, as shown in Figure 3.5. Essentially, every electrical subassembly connects directly to the Main PCB in a "star" configuration. Wire count in the system is significantly reduced, improving reliability.

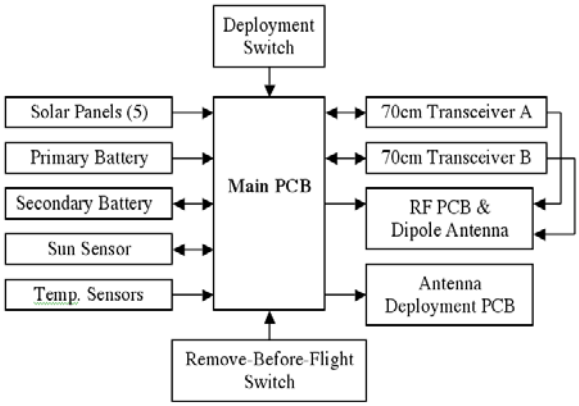

Figure 3.5 - Wiring Layout

Integration also reduces cost and the construction time involved. Rather than fabricating and populating numerous boards, each with specialized functions, a single board can be produced which functionally replaces them.

4. INTEGRATION

4.1 PCB Shock/Thermal Isolation Mounts

Two environmental conditions, mechanical shock and thermal extremes, led to the design of Delrin shock mounts to interface the printed circuit boards of CP1 with the structure. These shock mounts are simple in design but provide thermal isolation between the electronics and the structure. They also help absorb mechanical shock experienced during launch.

Preliminary thermal analysis indicated that the worst -case equilibrium temperature of CP1 would be as low as -60°C. Transient analysis identified a temperature range of –15 to +10°C. By thermally isolating the electronics from the structure, self-heating can increase the temperature of the electronics such that it is closer to room temperature. In the case of the transceivers, the command computer can actually provide thermal management by varying the transmission duty cycle based on the measured transceiver temperature.

4.2 Wiring Harness

The wiring harness of CP1 is significantly simplified by the highly integrated Main PCB. Still, however, quite a bit of wiring is involved. A unique feature of CP1 is that no connectors are used. Multi-conductor 26-gauge ribbon cable solders directly between subassemblies. This reduces mass and increases compactness and reliability. One obvious downside of this approach, however, is that subassemblies are not easily replaced.

To ensure that a direct path between subassemblies and the Main PCB exist, the wiring harness design, Main PCB layout, and structural design all occurred concurrently with a great deal of cooperation between electrical and structural engineers.

4.3 Battery Pack

The primary and secondary batteries of CP1 are integrated into a single pack to allow them to be more securely mounted to the structure. The pack includes a single Electrochem "C" size Lithium Metal primary cell and a custom built PolyStor Lithium Ion secondary battery containing three prismatic cells in parallel. The result is a single subassembly that integrates all of the power storage, protection electronics, and individual temperature sensors for the primary and secondary storage cells. Figure 4.1 shows the secondary pack and primary cell before assembly (left) and the fully assembled battery pack (right).

Figure 4.1 – Secondary Battery (left), Primary Cell (center), CP1 Battery Pack (right)

4.4 Solar Panels

To integrate well with the structure and maintain favorable electrical and thermal properties, a set of requirements was developed for the solar panels prior to their design. A primary goal was to develop a single design that would be compatible with all faces of the cube. Since the structural design of the top and bottom faces varies from that of the side faces, two fastener-hole patterns were required for mounting. Additionally, a rather large hole would have to be cut in the center of the panel on the bottom of the cube, to allow the Sun Sensor to "see" outside the spacecraft. Thermally, a good conduction path between the structure and solar cells to prevent overheating, was desired. Electrically, the panel would have to provide low resistance redundant connections to the solar cells. Additional design objectives included low mass, low cost, and simplicity.

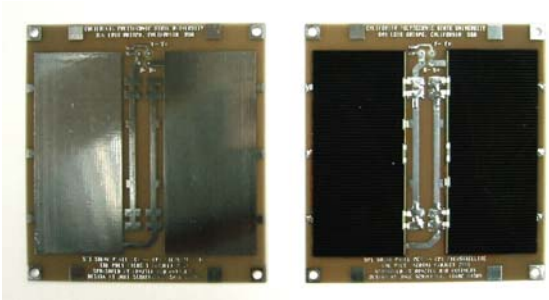

Figure 4.2 - Solar Panel PCB (left), Assembled Solar Panel (right)

The design of the panels to which the cells mount was quite challenging. After discussing the problem with numerous industry mentors, a rather elegant solution was developed. A double-sided printed circuit board, figure 4.2, was designed in which the redundant solder tabs on the cells connect directly to pads on the PCB. Large copper pours were included in the layout beneath each of two cells and on the entire backside of the PCB, providing good thermal conductivity from the cells to the structure. The cells are adhered to the FR4 panel using NuSil RTV silicone, and processes recommended by Raytheon advisors. All of the required mechanical interfaces were designed directly into the printed circuit board. Two versions of the PCB were fabricated, one with a hole for the Sun Sensor, used on one face of the cube, and one without, used for four sides of the cube.

4.5 Payload

Two payloads are scheduled to fly on the first launch. One of these payloads is a commercially developed sun sensor, shown in figure 4.3. The other is a magnetorquer developed at Cal Poly by undergraduate students. CP1 has a maximum payload volume of approximately 300cm^3. Payloads mount to two faces of CP1. The sun sensor mounts to the bottom face of the satellite, while the magnetorquer mounts to the data port/remove-before-flight Switch face of the cube, which is the one face of the cube not covered by solar cells (see figure 3.1).

Interface requirements for the sun sensor are relatively simple. The sun sensor uses a four-element sensor to detect, in two axes, the orientation of the satellite with respect to the sun. Internal to the sensor is a precision amplifier that conditions the signals from the four sensor elements to provide an output of 0 to 5 volts. These four voltages are periodically measured by the data acquisition system and stored. Data from one full orbit is FIFO buffered and transmitted on each communications cycle. Since this attitude data is not directly utilized by the spacecraft, the sun sensor data is processed on the ground.

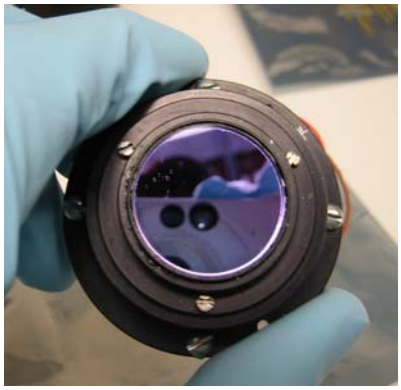

Figure 4.3 - OET Sun Sensor

Developed at Cal Poly, the magnetorquer was designed specifically for use on CP1. Long term, the objective of PolySat is to develop a CubeSat that is 3-axis stabilized with active attitude determination and control systems. Flying a magnetorquer and observing the effect of the magnetorquer using sun sensor data and solar panel current data provides a reference for future development of attitude control systems. The magnetorquer is a single electromagnet with additional control electronics that switch the power to the coil based on a digital line from the command computer. The control electronics also provide optical isolation and voltage spike protection to prevent damage from back EMFs produced by the magnetorquer coil.

5. CONSTRUCTION

The construction of CP1 begins with the fabrication of each subassembly and ends with the post-conformal coat functional test. Testing steps are included at key stages in the process, but testing during the construction process is limited. At least two identical spacecraft are constructed. The first is qualification tested at greater than 150% of worst-case loads. The second is flight hardware and is qualification tested at 150% loads and acceptance tested at 100% loads.

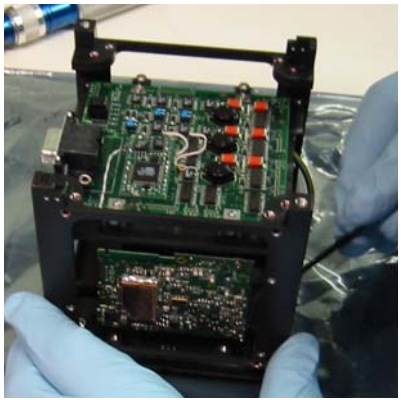

Figure 5.1 - CP1 in Construction

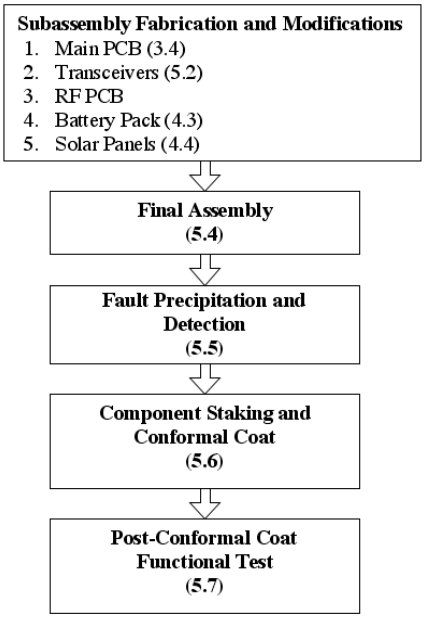

Figure 5.2 - CP1 Construction Process Diagram

5.1 PCB Fabrication and Assembly

With the schematic design of the Main PCB complete, layout began. At Cal Poly, several layout attempts were made using a four-layer strategy in which the center two layers are power and ground planes. Given the available board area of only 56 cm^2, this proved impossible. Finally, the design was sent to Solectron Corporation, where the board layout was completed in an eight layer configuration with multiple power and ground planes on the internal layers.

Following several layout design review iterations, the board was fabricated at BrazTek International, Inc. using standard FR4 material and commercial processes. The board thickness is 0.080", which for a board of such small dimensions results in very high rigidity.

The fabricated PCBs were then sent to Fine Pitch, a subsidiary of Solectron, for automated surface-mount assembly. Final assembly of the Main PCB, including the installation of all through-hole components, was performed at Cal Poly.

Commercial grade PCB fabrication and automated assembly facilities are currently in development at Cal Poly, which may enable future revisions to be fabricated and assembled entirely on campus.

5.2 Modifications

Using COTS subassemblies, such as the radio transceivers, in a satellite application requires modifications. Although testing in thermal-vacuum did not identify any component failures, modifications are essential to reduce weight, improve reliability, and provide a custom electrical interface to the Main PCB. Several non-essential components such as jacks and switches are removed from the boards.

The RF matching network used in the DJ-C5T is designed for the internal whip antenna, which is not a 50 ohm resistive load. To provide suitable matching to our 50 ohm feed line, the existing matching network is removed and a modified matching network is installed in its place to bring the output impedance to 50 ohms resistive. Since no useable RF output connectors are provided on the DJ-C5T, an RG-316 coax feed line is soldered directly to the PCB and then fixed in place with staking epoxy to prevent fatigue.

5.3 Electrical Subassembly

The electronic systems divide into five subassemblies: the Main PCB, transceivers, RF PCB, battery pack, and solar panels. Each of these subassemblies are built up and individually tested for functionality. No environmental testing is performed at this level.

5.4 Final Assembly

Final assembly involves the integration of all subassemblies into a complete system, ready to be staked, conformal coated, and then integrated into the structure. During final assembly, fit-checks are performed with the structure to verify wire lengths and routing paths.

5.5 Fault Precipitation and Detection

Once the staking compound and conformal coat have been applied, rework becomes very difficult and time consuming. To ensure that any preexisting faults are identified early on, the electronics are tested using techniques adapted from the Highly Accelerated Stress Screens (HASS) method in which latent faults are precipitated by extreme thermal cycling and then detected and fixed.[14] This is similar to "burn-in" but is far more successful at identifying latent failures that without being stressed would go undetected but would then become detectable during qualification testing, acceptance testing, or in orbit.

5.6 Component Staking and Conformal Coat

Using techniques and materials acquired through industry mentorship, all electronic subassemblies are staked and conformal coated with aerospace grade epoxy and conformal coat. The procedures used are similar to those used in industry for commercial or military spacecraft.

In the case of some subassemblies, such as the transceivers, the staking and conformal coat process must be broken down into several steps. The complexity arises from the fact that the transceiver has a "mother board" and "daughter board" which

sandwich together with a mating connector. The mating side of each PCB must be staked then conformal coated. Once that is complete, the boards can be mated and staked together. The non-mating sides of the boards must then be staked and conformal coated. Unfortunately, this process is extremely time consuming and limits the possibility of rework in the case of failure during qualification or acceptance testing.

5.7 Post-Conformal Coat Functional Test

Once the staking and conformal-coat have been applied, additional testing is performed to verify that the electrical properties have not been adversely affected. Of particular interest is ensuring that the conformal coat has not provided a medium for parasitic capacitive coupling in any of the RF circuits. With the electronics fully assembled and coated, the simplest method of verifying functionality is to run the satellite and measure the effective isotropic radiated power (EIRP) in a free space field test. The measured EIRP, diagnostic data from the data port, and data collected from the actual transmissions provide a good indication of whether the systems are operating correctly. Additional testing may include spectrum analysis of the radiated signal to verify signal quality.

6. TESTING

6.1 System Level Acceptance Test

To speed development, acceptance tests are not performed on every subassembly. Instead, the final assembly is acceptance tested. A complete satellite is built specifically for testing and that satellite will eventually be tested to destruction. Testing techniques are borrowed from the Highly Accelerated Life Testing (HALT) and Highly Accelerated Stress Screen (HASS) methodology. The basic concept is that the test loads are increased until a failure occurs. With the failure identified and documented, corrective action is taken. The test loads are again increased and the process repeats until the spacecraft is robust enough to reliably withstand launch and orbital environments.[14]

6.2 Power System Functional Test

Power system functional testing involves the steady state characterization of the power system, such that the efficiency and operating characteristics of each block are better understood. The characterization data is used to create the model that guides the development of power management algorithms for the command computer. In order for the command computer to intelligently determine the transmission duty cycle it must have an accurate indication of all critical temperatures, and at least some measure of the charge on the secondary battery.

A running tally of battery charge is difficult to implement in software, as accurately integrating the battery current in real-time requires too much attention from the microcontroller. Another option is to use the secondary battery voltage as an indicator of charge but the battery voltage in itself is not an accurate measure of charge, as the voltage is a function of charge, temperature and applied load. Utilizing the model generated from the power system characterization, an algorithm for estimating the battery charge based on the battery temperature, voltage, and applied load can be achieved.

Future hardware revisions may include a single chip "Fuel Gauge" I.C. that includes current and voltage sensing capability and communicates over a serial interface with the command computer, providing the charge on the battery.

Power system testing also provides feedback to the power system design engineer allowing an evaluation of the validity of the design concepts. Specifically, for CP1 it is important to determine the efficiency of not using a charge controller and determine how significant losses due to current sense resistors and line drops become in practical operation. Transient testing will identify potential power sequencing issues and latch-up conditions.

Table 6.1 - Worst-Case and Nominal Power Budgets

Power Source/Sink	Worst-Case (mW)	Nominal (mW)
Solar Panel Supply	+726	+726
Solar Panel Loss	-102	-102
3.6V DC/DC Rx Loss	-7	-5
3.6V DC/DC Tx Loss	-104	-39
5V DC/DC Loss	-6	-6
3.6V Rx Load	-18	-18
3.6V Tx Load	-520	-390
5V Load	-110	-110
Balance	**-141**	**+56**

A worst-case power budget is provided in Table 6.1. To obtain this budget, the maximum eclipse time, lowest possible DC/DC converter efficiency, maximum loads, and the maximum transmit duty cycle of 52% are assumed. Battery power sources are ignored as are battery charge inefficiency. The result is a power deficit of 141mW.

In practical operation, the average transmission duty cycle will vary automatically to balance the power budget. Assuming all other parameters are worst-case, reducing the transmission duty cycle to 40% provides a power surplus. Under normal operating conditions, transmission at the maximum duty cycle

with modest power surplus is possible. This nominal scenario is also provided in Table 6.1

One key design issue identified through power system analysis is the significant solar panel losses caused by the 0.3V drop of the Schottky blocking diode and the voltage drop of the current sense resistors. Future revisions of the design will focus attention on minimizing these losses.

6.3 RF Link Test

A functional test and accurate characterization of the RF communications systems must be performed to verify the design and construction methods, and to find values for unknowns that were not modeled in the design phase. Preliminarily, the RF impedance of each device in every possible operational state is measured. These values are used to verify the design of matching networks. Standing Wave Ratio (SWR) measurements provide a measure of forward power transfer, further indicating a successful impedance match.[15-19]

Field strength testing to determine the Effective Isotropic Radiated Power (EIRP) confirms the performance of the communications system. The power output of the transceiver is first directly measured. A reference antenna of known gain and pattern is connected to a spectrum analyzer for field strength measurement. From the Friis Transmission Equation[20] (Equation 6.1), the EIRP can be calculated.

$$EIRP = P_r (4\pi D)^2 / G_r \lambda^2 \qquad (6.1)$$

G_r, Gain of the reference antenna (referenced to isotropic antenna)

P_r, Power received by the reference antenna (W)

λ, Carrier wavelength (m)

D, Distance between satellite antenna and reference antenna (m)

Link testing of the RF systems on CP1 across a distance of 1.5 miles yielded an EIRP of 410mW. This result is consistent with the theoretical dipole antenna gain of 1.64 and rated transceiver output power of 300mW. The RF systems, therefore, appear to be operating as designed.

6.4 Communications Protocol Conformity Test

Used extensively in the software development for CP1 and distributed to amateur radio operators across the world, the communications protocol is a comprehensive document detailing the in-orbit operation of the satellite from a communications perspective. The protocol specifies the exact frequency, modes, content, and timing of transmissions, providing all necessary information to make contact, download data, and interpret the data.

As the final test of CP1, the spacecraft will be exercised to verify that its operation conforms to the communications protocol. The testing helps ensure that the software runs as expected and provides an opportunity for the ground station operators to tune the ground systems and gain operating experience prior to launch.

7. SUMMARY AND CONCLUSIONS

Consumer, commercial, and aerospace technologies and manufacturing methods are uniquely utilized in the design and construction of CP1. The CP1 design avoids the pitfalls encountered in scaling down large satellite system architectures for picosatellite use by recognizing the inherent differences between large satellites and CubeSats and designing new systems specifically suited to the application.

The electro-mechanical, communications, payload support, and functional requirements of CP1 are addressed in the design by utilizing the ground support resources of the amateur radio community and advanced commercial technologies that enable highly integrated systems. System characterization and environmental testing is ongoing, but all tests to date have been successful and yielded results consistent with the design analysis.

Electronic system design of the CP1 CubeSat relies on accepting and managing risk. Using the latest commercial technologies, CP1 provides a highly capable platform to support the test of emerging picosatellite technologies in space.

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