ISC (Integrated Spacecraft Computer) Case Study of a Proven, Viable Approach to Using COTS in Spaceborne Computer Systems

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Abstract. By judiciously using COTS technology a new space computer product that has lower cost, higher performance, is easy to use and retains the high reliability necessary for use in spaceborne missions was developed. Modern COTS processors and memories are used with a mixture of military and radhard components to meet the unique thermal-mechanical environment and radiation environment of space and still satisfy the need for high-reliability, low power consumption and low weight.

COTS Rationale

COTS (Commercial Off The Shelf) electronics offer compelling value not just because they are commercial or off-the-shelf. Their greatest value for use in high reliability applications lies in their high-volume production and wide-spread use: both drive down cost and drive up yield, performance and reliability.

The high-volume production of COTS products drives down their recurring component cost because of high yields and economies of scale. The wide-spread use of COTS reduces system cost. The use of COTS open standards drives down development and life-cycle support costs as well as reducing time to market for new products.

While a debate still continues in the space community regarding the merits and even the definition of COTS, most everyone can agree that adopting some aspects of the COTS electronics industry technology into the space electronics industry is a certainty.

GDIS Approach

In 1995 General Dynamics Information Systems ((GDIS), Computing Devices International at that time) embarked on a new space computer product development with four customer driven goals:

1) Reduce space computer prices by a factor of 10
2) Increase space computer performance by a factor of 10
3) Create a space computer that is easy and inexpensive to use with modern software tools
4) Above all do not jeopardize reliability

All four goals were met by judiciously using COTS, military and radhard technology to mitigate the severe space environment effects and maximize mission success. The initial trade studies indicated that adopting COTS everywhere would not meet our high reliability goal, but with extra care COTS devices could strategically be used for high-payoff functions. Trade-offs also indicated that using military components with solid radiation data instead of Class-S radhard components was the most cost effective choice for meeting natural space environment requirements.

Compared to previous generations, many modern deep-submicron CMOS microcircuits are very tolerant to total ionizing dose (TID) radiation, but they are still sensitive to single event upsets (SEU)[1]. Careful use of these modern devices within robust circuits can maximize their TID tolerance. Clever use of these modern devices within robust error detection and correction (EDAC) circuits can mitigate their SEU effects to the point they are virtually immune to SEU at the system level.

To effectively use COTS in the GDIS spaceborne computer three distinct system categories had to be addressed: software, electrical and mechanical for each of three levels of integration: chips, boards and subsystems. Design tradeoffs were influenced by the unique thermal-mechanical environment (vacuum, temperature cycling, vibration and shock) and radiation environment (electrons, protons, and heavy ions) of space combined with the need for long-term unattended operations requiring high-reliability and severe penalties for power and mass.

Folding these constraints into a life-cycle cost model for a moderate production volume product led to the development of a family of modular space computer products. This family of products is based on a combination of robust support circuits and high-payoff COTS components in an open architecture COTS-based product. This product line is referred to as the General Dynamics open architecture Integrated Spacecraft Computer (ISC) family.

The heart of the ISC design is a set of radhard support ASICs that enable the use of truly COTS PowerPC microprocessors and COTS memory devices in an architecture that provides industry standard interfaces such as JTAG, VME, PCI, 1553B and RS-422. The radhard ASICs and COTS devices are integrated with radiation tolerant high-reliability military-grade hermetic IC's and discretes.

Tradeoffs indicated that the value from COTS technology varied depending on the level of integration involved. For devices like COTS microprocessors and memories the value came from using fully packaged die from world-class high volume manufacturers; repackaging COTS die in MCM's was not cost effective even considering their potential weight and volume benefits. At the board level, the most benefits came from using open system bus protocols and COTS software. Buying complete COTS board level products was not effective because they could not meet the space mission requirements. At the system level, the greatest value was in having industry standard COTS interfaces and software that allowed plug-and-play with other subsystems.

In implementing the design of the ISC we established nine high-level radiation and performance related requirements that would enable the family of products to be viable for multiple programs (LEO, MEO, GEO, Reusable Vehicles & Expendable Launchers), and multiple applications (C&DH, GN&C, and Payload):

1) No single failure of a high payoff commercial component (non-hermetic and non-military) shall jeopardize a mission in a single string system
2) 100% detection of all errors caused by a single ion (proton or heavy ion) for the COTS processor and memory devices
3) 100% correction of all errors caused by single ion (proton or heavy ion) for the COTS processor and memory devices
4) Immunity to damage from SEL for all parts
5) >99% throughput with SEU mitigation techniques enabled
6) 100% Software compatibility with a commercial RTOS & compiler
7) SEU mitigation techniques transparent to application software
8) Designed for 15 year missions in the natural space environment for orbits less 1400 km and greater than 8000 km altitude with use of inherent shielding
9) SEUs cause less than 1 improper operation per hundred years on-orbit

Being viable for multiple programs and applications is important to achieving the target volumes needed to keep product recurring prices low. Complete computer units including enclosures can be used across the various platforms for multiple functions such as: vehicle control, mission management, payload processing and also remote terminal controllers. This commonality of use based on open and modular designs using COTS components leads to a lower life-cycle cost solution. Selective use of COTS components in a carefully partitioned flexible architecture allows us to seamlessly vary the ISC performance, radiation tolerance or reliability.

This paper will focus on the COTS microprocessor and main memory used in the ISC in the context of how they relate to the rest of the ISC as a case study in successfully implementing a space computer design with COTS components.

COTS Device Selection

Once the high level product goals and objectives were in place to guide the ISC development a baseline architecture was established and a baseline microprocessor was selected. The PowerPC™ 603e series was chosen as our preferred microprocessor.

The commercial PowerPC 603e microprocessor was chosen for several reasons:

- Immunity to Single Event Latchup (SEL)
- Built by two world-class suppliers (Motorola and IBM)
- Excellent reliability (low FIT rate)
- Excellent total dose performance,
- Excellent MIPS/Watt performance,
- Roadmap for increased performance
- Extensive software support, and
- Long-term availability

Due to its fabrication technology, the COTS PowerPC has excellent total dose performance and is immune to latchup. The GDIS designed support ASIC solves the SEU problems for the commercial PowerPC and allows

exploiting the full performance of the PowerPC and maintaining 100% software compatibility with COTS technology. Mechanically, the high-volume CBGA (ceramic ball grid array) devices are used as they come off of the commercial production line. A compliant lead system is added to the commercial packaging to increase the thermal-cycling capability of the device.

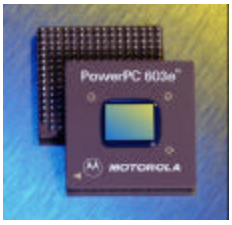

Figure 1. Photo of PowerPc 603 device from Motorola website

A COTS SDRAM memory device was also selected and like the PowerPC, SDRAM was chosen for many reasons:

- Immunity to Single Event Latchup (SEL)
- Manufactured by several world-class suppliers
- $/Mbyte 800 times better than radhard SRAM
- Better long term availability versus EDO DRAM
- Excellent total dose performance
- Better bandwidth than SRAM

Similar to the PowerPC, the COTS SDRAM has excellent total dose performance and is immune to latchup[2]. Again, the GDIS support ASIC solves the SEU problems for the commercial SDRAM which allows exploiting the full performance of the SDRAM and maintaining 100% software compatibility with COTS technology. Mechanically, the high-volume plastic TSOP (thin small outline package) devices are used as they come off of the commercial production line. These TSOP SDRAM devices are put into four high stacks by DENSE-PAC to increase the memory density on the board. These devices have been verified for composition and fabrication integrity by GDIS.

Figure 2. Picture of stacked SDRAM from DENSE-PAC website

Architecture Considerations

The CPU section of the ISC has an architecture very similar to most high-reliability commercial computers containing a PCI bus interface. The figure below shows a block diagram of the CPU and memory sections.

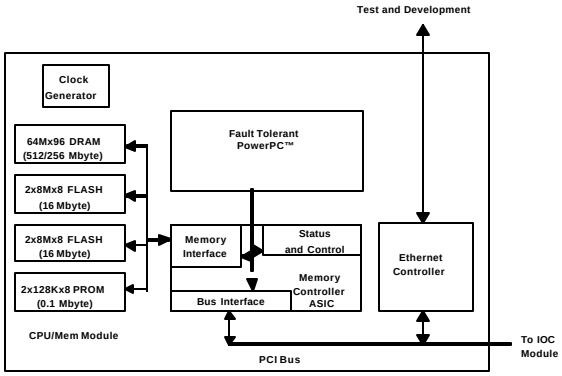

Figure 3. Block Diagram of CPU/Memory Section

Using an open architecture like the PCI bus saved development time and money. First, we were able to buy Intellectual Property (IP) to integrated into our ASICs and second it allowed us to use COTS PCI bus analyzers during initial development. We had to develop a radhard memory controller and 60X-bus to PCI-bus bridge ASIC because the equivalent commercial part (like the Motorola MPC106) was not robust enough and did not provide enough EDAC services.

This GDIS designed radhard memory controller ASIC provides EDAC for the PowerPC to make it immune to SEUs and provides the EDAC and redundancy management for the SDRAM as well as the non-volatile memory and boot EEPROM.

The CPU/memory section is connected via the PCI interface to the I/O section. This partitioning allows the CPU/memory and I/O sections to be independently developed and enhanced. Each time a new PowerPC microprocessor is introduced, the ISC architecture can easily take advantage of the increased performance and better MIPS/watt capability, often with absolutely no changes to the design. This is possible because we use commercial PowerPC devices from the commercial vendors who leverage their investment in improved designs by maintaining backward compatibility for many generations. For example, the PowerPC 603e series was improved from a 100 MHz device to a 300 MHz device while maintaining a 255-pin interface with the same 60X-bus protocol. This allowed an easy

upgrade to the 300 MHz device during the development process.

The PCI bus connects the CPU/memory section to the I/O section of the computer as shown in figure 4 below.

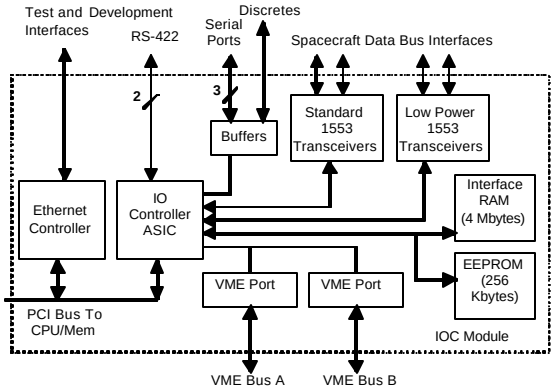

Figure 4. Block Diagram of I/O Section

The ISC uses standard external interfaces like 1553B, RS-422 and VME. Dual VME compatible busses are used to connect multiple I/O modules to the computers. This allows third party modules to be developed independently of the ISC, and be integrated into the ISC as the spacecraft is integrated.

While the ISC is electrically and protocol compatible with VME, a different physical packaging and connector system is used to optimize thermal performance, weight, and reliability. The packaging and connector system is compatible with the commercial VME standard to the extent that modules can be exchanged with the use of passive adapters.

Many spacecraft use a primary and warm or cold backup form of redundancy. The ISC system supports this by allowing two computers in an internally redundant single assembly, with each computer connecting to a dual VME bus system. While both computers can be active, one is designated by control signals to be the master. The master assignment can be changed in response to error detection. Interface modules on a VME bus can be cross-strapped to either computer. Interface modules can be either internally redundant, having two copies of the circuit, one connected to each VME bus, or be redundant by using two module, each connecting to one bus.

Software Considerations

Often in sophisticated space platforms, application software development time is the driving factor impacting program schedule. Software may also constitute a large portion of the program resources. For these reasons, we have designed the ISC EDAC approaches to have the least amount of impact on application software while still granting simple and straightforward access to the necessary hardware registers and machine states.

One of the biggest impacts to cost for an open system is the plug-n-play aspect for software. We provide a solution that has well documented interfaces, uses industry standard techniques and promotes easy upgrading of software.

The ISC software has been written in the C-language. The C-language was chosen for the following reasons:

- C-language code can interface with both C++ and Ada application code
- The C-language does not require run-time support as compared to the constructor/destructor mechanism in C++ run-time and the start-up initialization code associated with Ada
- The C-language is a well understood, widely used and well supported technology

We implemented the C-language using an object-oriented style of implementation, which gives some of the benefits of the object-oriented C++ language without the disadvantages. The ISC code defines (in *.h files) only those data structures and function prototypes that a user needs/requires to access the services provided by a driver or manager element. All other data structures and function prototypes are defined in the *.c files and are hidden from the application developer. This use of the *.h and *.c files yields the object-oriented form of implementation.

ISC software has a very modular structure and minimum dependencies on the COTS operating system (currently VxWorks™ from Wind River Systems). Our software implementation includes interrupt handling, DMA engine control, customer timer management, and similar functions that provide access to and control of on-board hardware capabilities at the lowest levels. The I/O driver and message passing features are implemented on top of these lowest level layers. The Application Programming Interface (API) provided by the ISC software CSCs are defined as functional services rather than low level access to hardware registers. These characteristics of the software allow new implementations at the hardware level to be incorporated into a design with minimal risk that the API will be altered and affecting the using application.

The use of the underlying OS is focused on semaphore use, task scheduling, and delay requests. This enables the ISC hardware to adjust to a new OS or a new release of an OS quickly.

The ISC software tool set has been selected to support use of both Windows and Unix host environments. While the number of vendors that provide that breadth of support is somewhat limited, it does allow the user to use the most cost effective development environment and/or their corporate standard development environment.

The ISC software is implemented on top of the VxWorks operating system. VxWorks has a POSIX compliant interface that the application developer can choose to use. If used, the application code also has greater portability from platform to platform.

Both an Ethernet connection and a serial connection to the development host is implemented. The Wind River Tornado™ tool set can use those interfaces interchangeably to support application development. The Ethernet interface is provided for the engineering models and typically depopulated on flight units. This was done to provide application developers the same software environment provided by COTS vendors and to allow for fast down loading of their target application software.

Electrical and Radiation Considerations

Single Event Effects (SEE)

Single Event Upset (SEU) performance of a spaceborne system is dependent upon three factors. These factors are:

- The particular ionizing environment encountered by the system,
- The susceptibility of the individual piece parts in the system, and
- The system architecture.

Both the PowerPC and SDRAM devices are inherently immune to single event latchup (SEL), but are sensitive to SEUs from both heavy ions and protons. This inherent part quality allows use to meet objectives 4 (Immunity to damage from SEL for all parts) and 8 (Designed for 15 year missions in orbits less 1400 km and greater than 8000 km altitude with use of inherent shielding) listed in the beginning of the paper.

To meet objective 1 (No single failure of a high payoff commercial component (non-hermetic and non-military) shall jeopardize a mission in a single string system) chip level redundancy is used within a module for the PowerPC and SDRAMs. This means an entire SDRAM chip or PowerPC chip can fail and not lose the functionality or degrade the performance of the computer. Objectives 2), 3), 5), 6) and 7) are met by our implementation of the EDAC scheme for the PowerPC and SDRAM. The PowerPC EDAC scheme assumes an SEU may occur anywhere inside an individual chip and propagate to any combination of outputs on the chip[3,4]. The EDAC approach detects all possible errors caused by a single ion (proton or heavy ion) in hardware and corrects the errors with a combination of hardware and software that is transparent to the user and allows for approximately 99% of the throughput of the PowerPC device.

SDRAM EDAC is implemented as a standard Hamming code SECDED (single error correction and double error detection) scheme and also an optional TECQED (triple error correction and quad error detection - with nibble correction) scheme.

To validate that the EDAC schemes worked as designed, as part of our overall SEE testing program, we exposed both the PowerPC and DRAMs to proton beams with our EDAC enabled while running dynamically at full speed. The software used was the VxWorks operating system and several different software benchmarks designed to be representative of flight code and exercise the PowerPC and memory with a wide range of operations during the test.

The figure below shows a picture of the proton SEU validation test setup at the UC Davis proton facility. This dynamic testing proved that all single ion errors could be detected and corrected reliably without adversely affecting the software timeline. Additionally, other proton tests were performed as well as heavy ion tests for SEU and SEL.

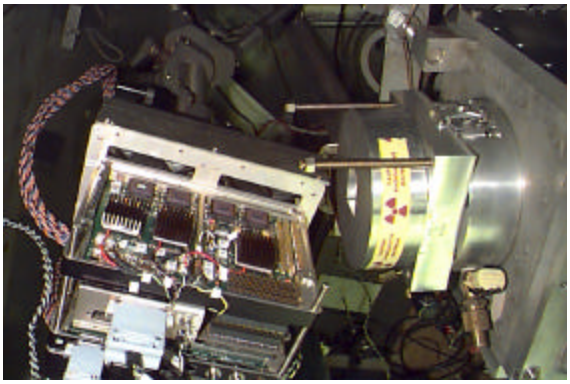

Figure 5. Picture of SEU Setup at Proton Beam

Total Ionizing Dose

The total ionizing dose (TID) performance of a spaceborne system is dependent upon three factors. These factors are:

- The mission duration and orbital environment (trapped radiation belts and solar events) encountered by the system,
- The susceptibility of the individual piece parts at the space dose rates and under their operational configuration and biasing conditions
- The system hardening techniques employed

Both the PowerPC and SDRAM devices are inherently tolerant to total dose levels adequate for orbits below 1400 km and above 8000 km for 15 years. This inherent part quality allows us to meet objective 8 (Designed for 15 year missions in the natural space environment for orbits less 1400 km and greater than 8000 km altitude with use of inherent shielding).

Even though the PowerPC and SDRAM have a significant amount of inherent total dose tolerance, their on-orbit lifetime can be extend by carefully and thoroughly understanding the total dose response of the devices. This required testing the devices in "real world" exposure and biasing conditions and measuring their performance over a range of temperatures. By the testing the devices at various speeds and temperatures we were able to design our support circuits and radhard memory controller ASIC to accommodate TID induced changes in the PowerPC and SDRAM devices in order to improve their total dose tolerance beyond what might nominally be expected.

Similar approaches were used on the rest of the circuits in the ISC as part of a comprehensive radiation testing and worst-case analysis design verification program. We used Mil-Std-1547 and 975 as guidance for derating the electrical design with additional derating as needed for accommodating total dose and proton radiation changes to device parameters.

Thermal-Mechanical Considerations

The thermal environment in space platforms is much more severe than for commercial applications, but often less severe than for many military platforms. Once past the initial shock and vibration threat from the launch environment, a satellite computer typically has a relatively gentle ride for the remaining years of the mission. However, having no air cooling requires a mechanical architecture that allows excellent conduction cooling of devices. This is particularly important for COTS devices since the manufacturer does not typically rate the parts for extreme temperatures.

In addition to conduction cooling, the mechanical design must also provide highly reliable operation over many thermal cycles. In order to maximize the use of the PowerPC CBGA package with high-volume PWB material we used a compliant lead system to mate the CBGA packages to the PWB to eliminate the TCE (thermal coefficient of expansion) mismatch problem.

This compliant lead approach allows us to reliably use the high-volume CBGA commercial package and our architecture allows us to use the commercial silicon at full speed while remaining immune to radiation SEUs.

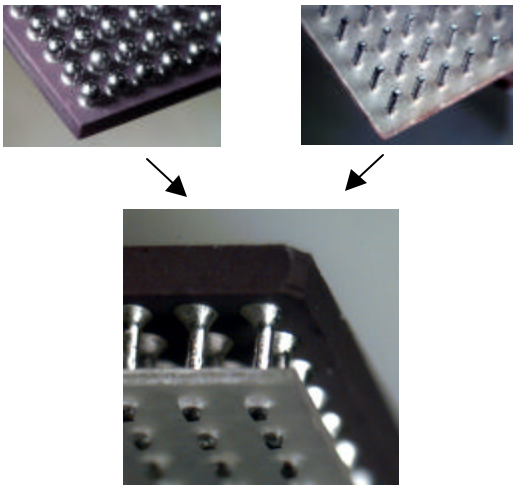

Figure 6. Picture of CBGA and compliant lead system before and after attachment

This compliant lead system was previously developed at GDIS for use in high-rel military applications that have severe thermal environments. To validate that the compliant lead system would work for our design, we tested several components in a series of vibration and thermal-cycling experiments. Functional components were tested in six modules that were stacked into a mechanical mockup to represent a full space computer subsystem. In addition to the CBGA compliant lead system, we also validated the stacked SDRAM memory parts and several other technologies that needed additional validation test data.

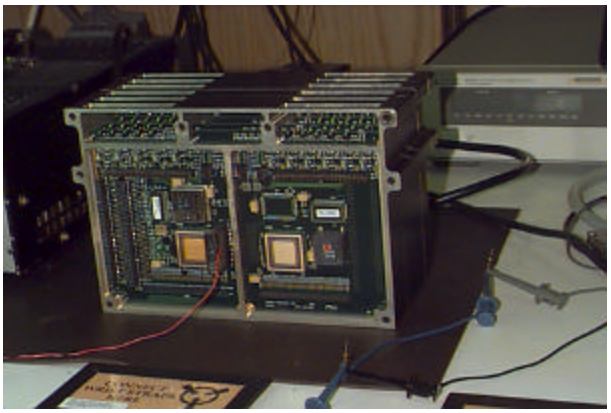

Figure 7. Picture of mechanical assembly used in vibration and thermal-cycle tests

This mechanical validation test consisted of the following sequence of steps conducted with power applied to the circuits to detect any open or short circuit failures at the earliest possible opportunity:

1) vibration testing the box of modules a ATP levels,
2) inspection of modules
3) thermal cycling the box from –40 C to +100 C over a 90 minute period for 300 cycles
4) vibration testing the box to Qual levels
5) inspecting the modules
6) thermal cycling the box again from –40 C to +100 C over a 90 minute period for 300 cycles

The figure below shows the control screen from the vibration testing chamber.

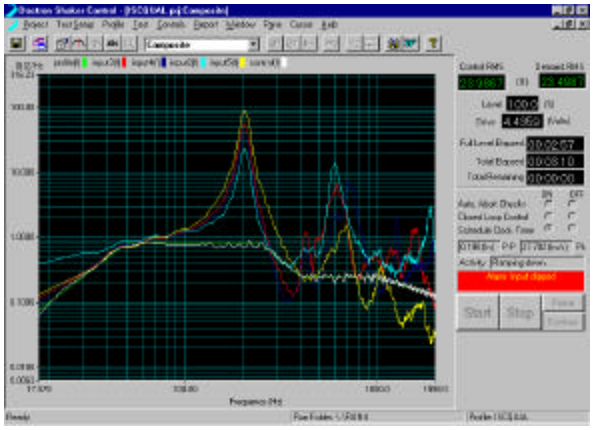

Figure 8. Control screen from vibration test

In addition to validating the PowerPC, SDRAM and other component packaging technologies, this test was used to verify the manufacturing processes and techniques used during production produce reliable products. This was the fourth such test in a series of vibration and thermal-cycling tests that have been conducted over a four year period to validate the technology used in the ISC product.

In addition to designing and qualifying the ISC to use COTS components successfully in space, we adopted manufacturing techniques for the ISC that do not degrade the inherent high quality of the COTS devices. These manufacturing techniques include humidity controls, dry nitrogen storage, part pre-baking prior to soldering, and careful selection of conformal coatings and cleaning solvents. These approaches have been successfully used at GDIS for many years to enable use of COTS devices reliably in high-rel military avionics applications

Summary

By judiciously using COTS technology we were able to create a new space computer product that has lower costs, higher performance, is easy to use and retains the high reliability necessary for use in spaceborne missions. This development effort has been a combination of using tried and true space industry practices, lessons learned, and a thorough verification and validation process. This philosophy has been implemented from initial design activities through engineering and flight unit development.

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