

Intelligent Reconfigurable Integrated Satellite Processor

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ABSTRACT

We present our Intelligent Reconfigurable Integrated Satellite (IRIS) Processor. At the heart of the system are our reconfigurable vision chips which are capable of massively parallel analog processing. The smart vision chips are capable of not only centroiding and pattern recognition but also tracking and controlling devices including MEMs devices and active pixel arrays. In addition to discussing the active optic and active electronic devices, several small satellite system applications are presented along with experimental and simulation results.

INTRODUCTION

The Intelligent Reconfigurable Integrated Satellite (IRIS) Processor System, being developed at AFRL for space imaging systems has incredible processing and control capability. At the heart of the system are our reconfigurable vision chips which are capable of massively parallel analog processing. The smart vision chips are capable of not only centroiding and pattern recognition but also tracking and controlling devices including MEMs micro-mirrors. In addition to analog processing, our Intelligent Reconfigurable Integrated Satellite Processor system includes the Texas Instrument's TMS320C6000 series DSP chips. The C67 is the fastest DSP processor in the world, clocking in at over 1GFLOP. New packaging technologies like flexible flaps, chip-on-board, chip scale, and micro-fine-line ball grid arrays (BGAs) are paving the way for revolution in lightweight,

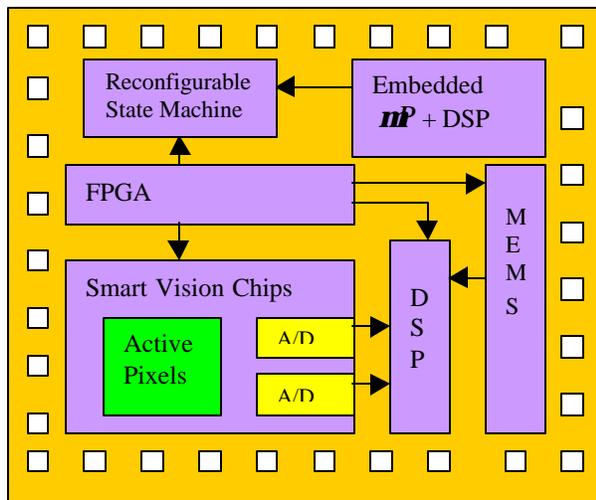
low power systems. While recognizing the cost effectiveness of legacy applications. In this paper, we describe methods to optimize the overall system implementations of multi-chip module designs, we intend to take full advantage of the newer technologies as we migrate our design from the lab to space based performance by clever control of the devices themselves as well as optimizing where and when a particular process occurs.

The massively parallel processing architecture of our system will have internal self-learning optimization characteristics. Using modified off-the-shelf software, the system will perform load-balancing and continually monitor the health of all processors in the architecture. Computation times of the different processors in the architecture will be tracked, allowing all transactions requests to be fulfilled with the required type(s) of processor(s). For example, a transaction request could be accompanied with an "accuracy" tag to allow for the most accurate computation regardless of speed, or with a "efficiency" tag to balance computation speed with accuracy. If any of the architecture components begin to show signs of fatigue or wear (i.e. significantly decreased computational characteristics), users could be automatically notified and the system would perform the necessary adjustments to compensate for the failing component.

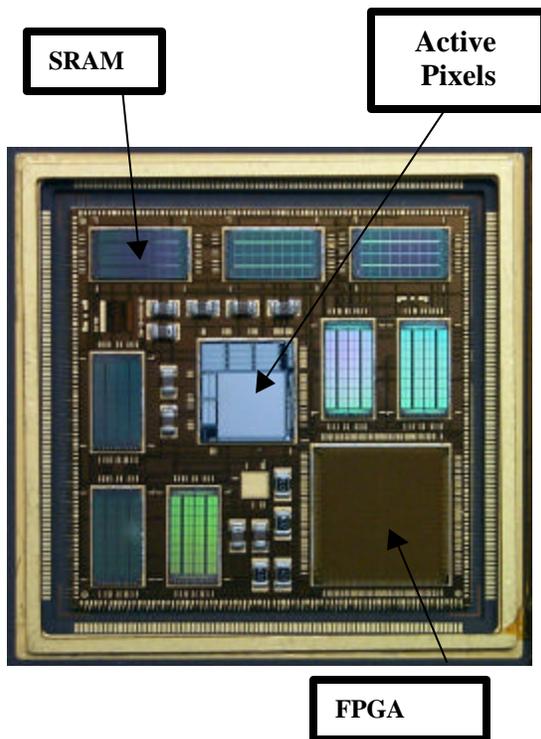
RECONFIGURABLE ARCHITECTURE

Implementing such active optic and active electronic devices in small satellite applications require a platform that fulfills the demanding low-power requirements yet has enough flexibility to enable the dynamic reconfiguration and adaptability the satellite system requires. Figure 1 illustrates an architecture that attempts to satisfy these

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(a)



(b)

Figure 1. Intelligent Reconfigurable challenging requirements along with a picture of a multichip implementation of a smart vision system in a multichip module (fabricated by Tanner Research Inc.). Integrated Satellite Processor. (a) Conceptual architecture and (b) multichip module implementation

Our Intelligent Reconfigurable Integrated Satellite (IRIS) Processor offers advantages in flexibility, low power consumption, light weight, and small size. The architecture allows several active optic and active electronic modules, to be integrated into a single system such as the multichip module imaging system shown in figure 1(b). Example modules include:

- An embedded processor subsystem for application and protocol-stack layers, which require more flexibility but have low computational complexity at relatively low update rates;
- Configurable processing/controller modules such as massively parallel smart vision chips, active pixel arrays, and MEMs devices for the more speed intensive layers;
- A parameterized and configurable digital physical layer; And
- A simple direct-down conversion front end.

Some of our previous efforts in the area of reconfigurable computing have demonstrated that a dynamic matching between application and architecture offers tremendous advantages in speed, size, cost and power consumption making such devices ideal for a wide variety of space applications. Systems designers can trade flexibility and programmability in a continuum from hardware to software. Designers must match system elements individually to implementation platforms in order to reach the optimum performance. In addition, the overall architecture must weave together these heterogeneous blocks with a flexible, yet energy efficient interconnection scheme.

Reconfigurable architectures- which utilize a “programming in space” approach – have proven to be very efficient for the signal processing component of communications processing, delivering high performance computation at an energy cost close to custom hardware implementations and maintaining enough flexibility to adapt to varying conditions of the system and environment. We are currently researching methods for the same to hold for the control-oriented components.

Preliminary analysis indicates that FPGA and configurable finite state machines implementations of the protocol stack are two orders of magnitude more efficient than embedded microprocessor or microcontroller solutions.

ACTIVE OPTIC AND ACTIVE ELECTRONIC DEVICES

MOEMS MICRO-MIRRORS

This section discusses MEMS micro-mirror devices that can be used in small satellite systems. We currently have a test die containing an 8x8 piston mirror array in fabrication in the four-layer planarized SUMMiT process at Sandia National Laboratories. Testing of this and follow-on arrays will yield a final array with optical and electrical characteristics which far exceed any piston micro-mirror currently available in any laboratory. Figure 2 shows the 8x8 mirror array test die. The main array occupies the center of the die and is connected to the outside tier of bond pads.

Figure 3 shows the details of an individual mirror design. This figure captures all of the advantages of the SUMMiT process for MOEMS. SUMMiT has a combination of features not found in other MEMS fabrication processes, such as a chemical-mechanically polished upper surface, 1 micron design rules, and four releasable layers. One of these layers is only 1 micron thick, allowing extremely low drive voltages. Current 4-flexure mirrors can be designed for actuation at less than 10V, making it possible to drive them with standard CMOS circuitry. The multiple releasable layers allow all of the wiring and flexures to be completely hidden under the polished optical surface, resulting in near-optimum active mirror area coverage. This is an important consideration not only for optical efficiency, but also in applications where stray

light leakage into the mechanism limits power handling capability.

The multiple layers also allow us to shield the wiring so the optical surface can be metalized after the release etch. Thus the optical surface of choice can be deposited without concern over its survival through the harsh release etch. Another advantage of post-release metalization is that the entire active area is covered, unlike drawn metal which requires a margin between the edge of the metal and the edge of the polysilicon upper plate. These capabilities, coupled with the hidden-flexure/post metalization design techniques, give the 8x8 test array of 100 micron square mirrors an active area coverage of 97.7%. This high active area coverage offers unprecedented diffraction-limited imaging with minimal light loss. Referring to figure 2, Figure an array of 50 micron square mirrors. Note that only mirror surfaces are visible, and the only area lost is due to the 1 micron gaps between the mirrors, the etch holes, and the anchor posts. This array has an active area coverage of 95.3%, and there are no topological effects from the underlying layers.

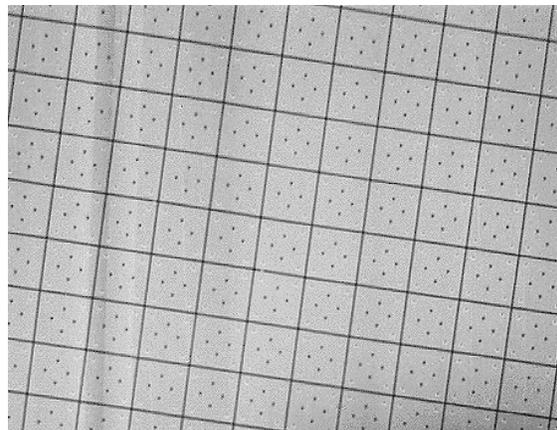


Figure 2. Array of MOEMs Micro-Mirrors

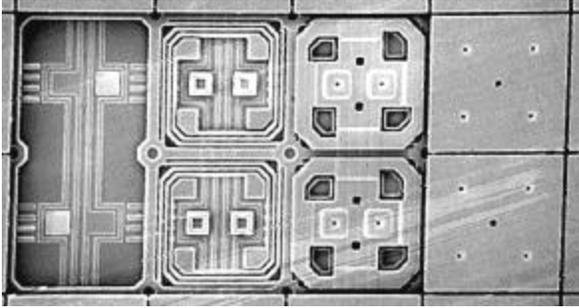


Figure 3. Details of the structure of the micro-mirrors are shown.

Referring to figure 3, the details of a typical flexure beam piston micromirror which takes full advantage of the SUMMiT capabilities. These 50 micron square mirrors achieve 95.3% active mirror surface coverage. The layers left to right are: Poly0 layer used for wiring throughout the array; Poly1 used for the flexures because it is the thinnest layer, poly1 is also used for metalization gutters (square frames surrounding the spiral flexures) to prevent post-release metalization from shorting the wiring; Poly2 is used for the lower electrode of the electrostatic actuator; Poly3 forms the upper electrode and is also the planarized surface - note the total lack of topological effects at this level.

SPECTRALLY TUNABLE FABRY-PEROT ETALON DETECTORS ARRAYS

We have recently begun a DARPA Program between Honeywell, the Air Force Research Laboratory, SAIC, and North Carolina State University to develop a MEMs based spectrally tunable detector array. As illustrated in figure 4, each MEMs Fabry-Perot Etalon can be independently tuned to only allow one spectral component to reach the photo-detector element. Referring to figure 4, each MEMs Fabry-Perot Etalon can be controlled by the smart vision chip with a method similar to that used to control the MEMs micro-mirror array discussed in the previous section. The Fabry-Perot Etalon

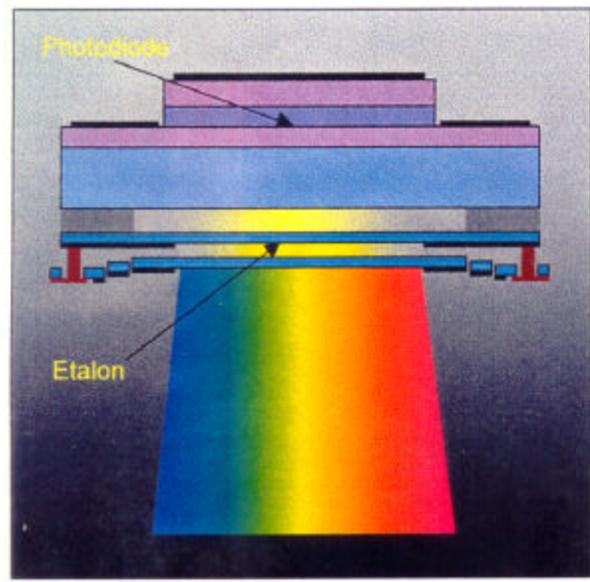


Figure 4. Conceptual drawing of a MEMS spectrally tunable detectors.

spacing spectrally filters the incoming light before it impinges on the detectors. Hence the device acts as A hyperspectral imager. In addition to controlling the MEMs Fabry-Perot device, the smart vision chip can be used for pattern recognition and tracking.

ACTIVE PIXELS

Active pixel sensors (APS) are in fact imagers in which each pixel incorporates some minimum circuitry to improve the image acquisition characteristics. CMOS based APS have been studied since 1980's by Japanese electronic industries, as an alternative for CCD cameras. Recently, the new market for multimedia cameras has created an atmosphere of struggle toward re-establishing the same concepts. Because of their low power, high dynamic range and inherent radiation tolerance, active pixel sensors are well suited for many small satellite applications.

Unlike vision chips (which are discussed in the next section) where some high level image processing is performed at the pixel level, APS only try to capture the image with a focus toward improving the image quality using standard processes. In this regard APS can be regarded as less smart sensors. APS have extensive applications for astronomical and space exploration applications, in addition to recent interest in multimedia applications, for video and still-image imaging. APS can achieve low noise, large dynamic range, high speed, random access to pixels, and so on. Most of the circuits used in APS can well be used in vision chips, because the size and complexity of the circuits that are used in APS are less than those used for smart vision sensors. Also, the higher dynamic range, lower noise, or higher speed brought by additional circuits in APSs are as essential for vision chips. Some of techniques used for enhancing the performance of APS can also be applied to vision chips.

An example active pixel sensor pixel layout (photocircuit) shown in figure 5 is an in active pixel sensors based on the charge integration method The read-out circuit used in APS is often a source follower based circuit The photodetector structure used for APS can also be based on any of the photodetector structure as illustrated in the layout of figure 5.

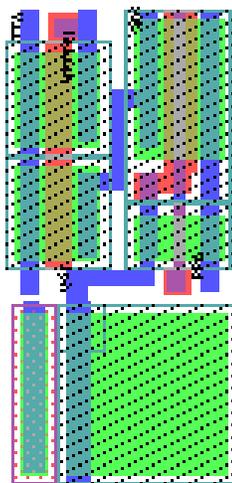


Figure 5. Active Pixel Sensor

SMART VISION CHIPS

We have developed a smart vision chip that can be used in a wide variety of small satellite applications. Later in this paper, we present three particular applications (adaptive optics, interferometric SAR imaging, and an Intelligent Star Tracker) that we are currently pursuing.

The floor plan of our smart vision chip is shown in figure 5 and resembles that of a static RAM. The major subsystems of the solver are the row decoder, the column decoder, the output buffer, the boundary cells, and the 14 x 14 array of interior resistive cells.

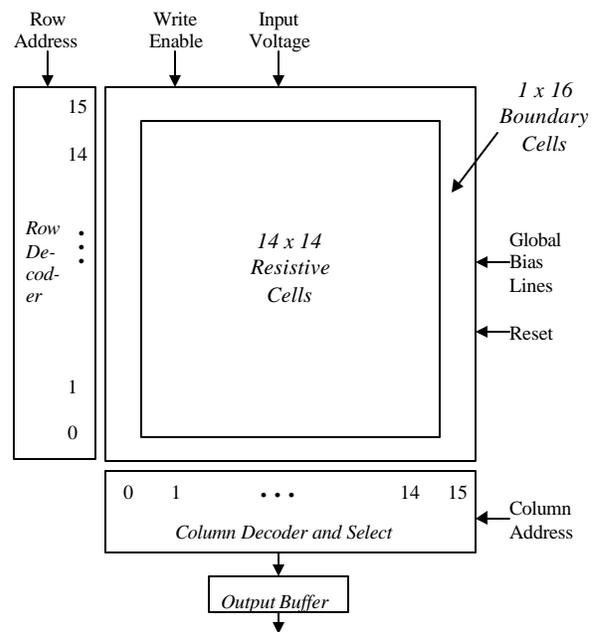
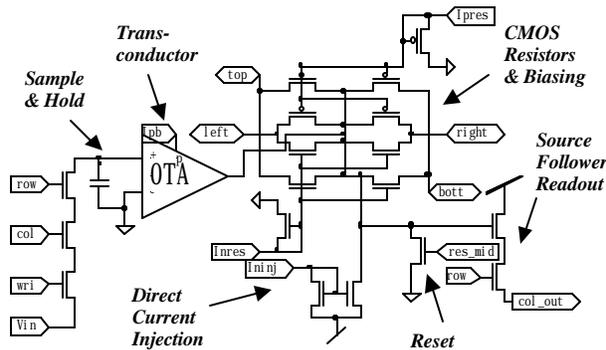


Figure 5. Smart vision chip floor plan.

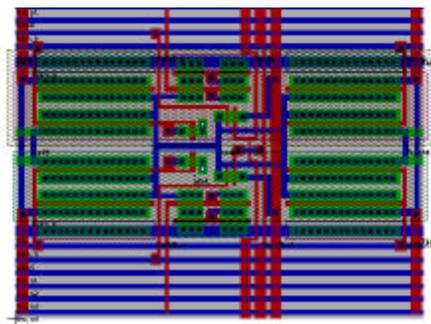
Figure 5 shows the schematic of the interior resistive cell. A sample and hold circuit stores the input voltage on an input capacitor. An operational transconductance amplifier converts the input voltage into a bi-directional current. That current is injected onto the cell node and its effect is spread to four nearest neighbors through CMOS resistors biased in the ohmic region. The output voltage is sampled using a source follower. The cell can

be reset to ground via a reset line in order to be able to compensate for the DC offset voltage in the source follower. A final feature of the interior cell is that it is possible to inject a static DC current through a current mirror for testing the array.

For new satellite system, distributive applications links a group of processors to create a virtual super computer. Distributive processing allows the various processors to utilize unused processor time to do the computations.



(a)



(b)

Figure 6. (a) Schematic of interior resistive cell. (b) Layout of a single cell.

DISTRIBUTED PROCESSING

The whole is greater than the sum of its parts. That in some ways, explains the theory behind one of the most important new technological opportunities today- Distributive Processing.

The concept of distributed computing has been around for years but never took off. Now, however, more powerful communications technologies are making it easier to link devices to perform complex distributed applications. And the increased demand for high performance computing by a growing number of commercial and noncommercial organizations is driving the demand for distributed applications. Eventually this technology will become like a utility that small satellite systems will depend on.

The individual modules on a chip can be coarse grained or fine grained. In coarse grained applications, individual modules communicate with master and proxy servers but not with each other. This approach is good for brute-force computations in which the application only has to divide calculations amongst different modules. In fine-grained applications, participating modules must communicate with each other. This is not necessary for all applications and missions. As the current satellite mission progress, changes in situations handled by one module affect situations handled by others. Modules must be able to communicate these changes to each other.

For maximum effectiveness, distributed computing technologies can run on a variety of module platforms, including FPGAs, DSP, Smart Vision Chips, Active Pixel Sensors, and MEMs devices. In some cases, designers may optimize the core algorithms for a particular platform or module. To run on multiple platforms or modules, designers must either write the core in a platform neutral language such as HDL, JAVA or design a distributed platform that can run on different types of machines.

Architecture for Distributive Computing:

Distributed computing applications typically use a hierarchical architecture in which a master server hands out tasks to various clients, which execute the tasks and send their work back to the server.

In some applications a module finishes a task and requests more data from the server. In other applications, where module activity is highly predictable, servers push data on a set schedule. In very large complex applications, proxy servers lighten the master server's load by handling many communication tasks. This permits scaling and load balancing, and helps distributed applications work around network problems.

Critical Issues For Distributive Computing:

Distributed applications have had to address two critical technical issues:

1. Fault-tolerance and Recovery :

A master or proxy server monitors network communications. If an a connection goes down or a client crashes, the server sends the task to another client.

2. Communications:

Distributed applications have two primary communication needs. Applications send a relatively small data file once a day at most. In other applications, such as simulations, in which different nodes frequently communicate their state to each other, a tremendous amount of communication is requires.

IRIS APPLICATIONS

Our Intelligent Reconfigurable Integrated Satellite (IRIS) processor can be used in a wide variety of small satellite applications. In this section, we discuss three particular applications that we are currently researching. In addition to speed, the IRIS processor offers advantages in size, cost, and power consumption.

Adaptive Optics Application

Adaptive optics can be used to compensate for optical aberration and misalignment in an optical system. The micro-mirror devices discussed in this paper can be used as a deformable mirror. This enables the optical designer to develop smaller, lighter and cheaper high performance optical systems.

A typical adaptive optic system includes a wavefront sensor that senses the optical aberrations, a wavefornt reconstructor that figures out the wavefront from the wavefront sensor data, and an active optic element to compensate for the optical aberrations. Figure 7 illustrates our silicon eye that is based on a phase diversity wavefornt sensor that is able to determine the aberrations from two out of focus images such as those shown in Figure 8. A spatial light modulator such as the micromirrors discussed in this paper then can be used to compensate for the aberrations and produce a corrected image such as the one shown in figure 8 (c). The particular spatial light modulator used to correct the image in the figure was a liquid crystal device manufactured by Medowlark Optics which had 128 pixels in a hex pattern.

Intererometric SAR Imaging

The smart vision chip we presented previously in this paper is capable of performing virtually any wavefront sensing (such as Hartmann, Shearing Interferometer, and Phase Diversity) at bandwidths exceeding 1kHz. We recently discovered that our smart vision chip is also capable of performing some real-time 3D imaging operations, including creation of maps or pictures, tailored to user needs. In addition to speed, our enhanced smart vision chip offers advantages in size, cost, weight, power consumption, and radiation tolerance. Another advantage is that the smart vision chips can be used in many applications, both government and private sector. The information revolution has shifted the focus from data collection to efficient processing, exploiting, and communicating

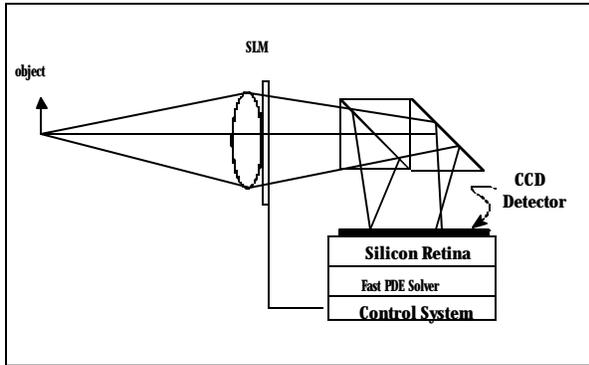


Figure 7. Silicon Eye adaptive optic system.

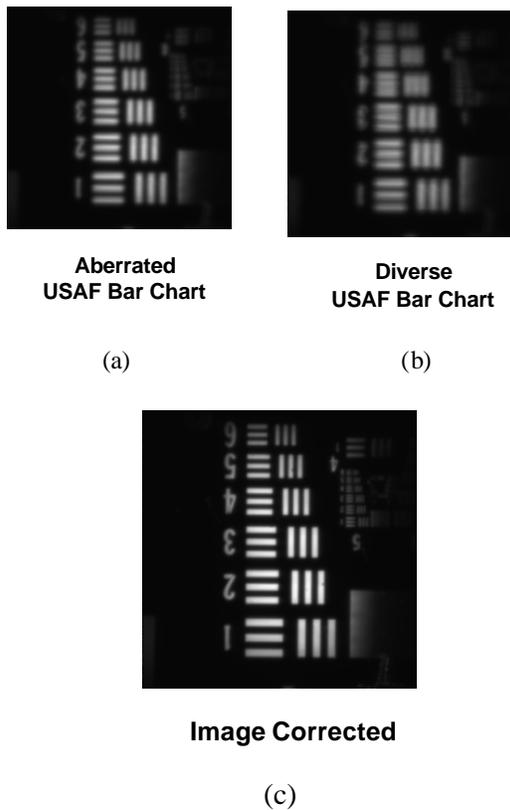


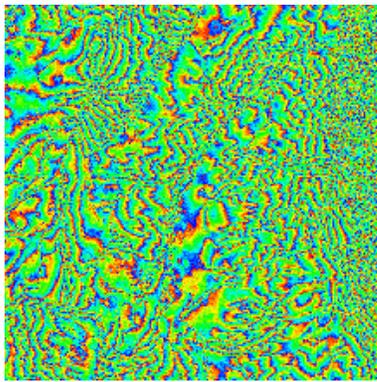
Figure 7. Experimental results from a Phase Diversity Adaptive Optic system.

data gathered from space, airborne, or other platforms to end users of intelligence. Over the past several years there has been a marked

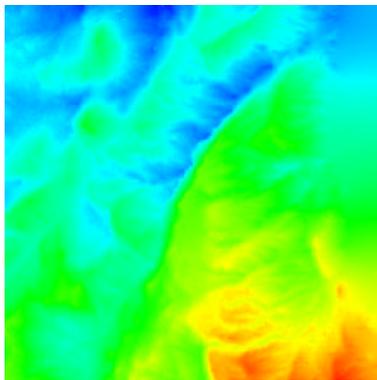
increase in the development and application of advanced techniques for coherent signal and image processing. The development of sophisticated imaging systems is considered to be the most challenging. One key problem is the fact that vision algorithms are very expensive in terms of computer cycles. Even super computers have difficulties with the computational load imposed by only moderately complex vision algorithms. Secondly, problems in vision usually require solving an inverse problem; the two-dimensional irradiance distribution on the photo-detectors must be inverted to recover physical properties of the visible three-dimensional surfaces. More precisely, inverse problems are ill posed in that they either admit no solution, infinitely many solutions, or a solution that does not depend continuously on the data.

By enhancing the smart vision chip described previously in this paper, we then are capable of performing real-time 3D imaging. In addition to speed, our new approach, based on a novel phase unwrapping technique, offers advantages in cost, size, power consumption, and radiation tolerance. The analog nature of our interferometric SAR phase unwrapping chip enables it to solve problems that digital systems cannot. Moreover, the phase unwrapping chip inherently lends itself to low cost production, thus enabling various government agencies to reduce the time and cost of developing sophisticated imaging systems.

Of all the vision applications, phase unwrapping is one of the most challenging. Two dimensional phase unwrapping is the type of problem that is typically in the domain of the mathematician. It is both complex and abstract. However, phase unwrapping is also the core technology that is used in many applications including SAR interferometry, optical interferometry, adaptive optics, and magnetic resonance imaging (MRI). Current



Mred , Mgreen , Mblue
 (a)



Mred , Mgreen , Mblue
 (b)

digital algorithms for performing sophisticated phase unwrapping such as those compared in figure 9, can take 2 hours on an IBM RS6000 computer for a 256 X 256 image. The massively parallel phase unwrapping smart vision chip can perform comparable computations at rates exceeding 100 Hz.

Virtually all of the problems associated with phase unwrapping arise when one goes from the continuous to the discrete domain. The phase unwrapping chip methods we designed is a paradigm shift from digital processing to massively parallel analog processing and thus avoids these pitfalls. but all agencies involved leading to a better end product that best suits their missions. While we have already achieved encouraging results from our 16x16 prototype (including using it in actual adaptive optic systems), we are developing some significant enhancements for the 3D reconstruction.

Range Line	63	127	191	255	383
Region Growing (Univ British Columbia)	54	96	52	51	45
Cut Line (JPL)	542	473	271	105	87
Intelligent Phase Unwrapper	270	240	153	132	168

(c)

Figure 9. Computer simulation results of the Intelligent Phase Unwrapper chip. The Intelligent phase unwrapper will operate at bandwidths exceeding 100 Hz. The JPL and Region growing algorithms take 2 hours of processing on a RS6000 computer.

Figure 9 illustrates the performance we expect to obtain, based on the experimental IBM RS6000 computer for the difficult Sardegna interferometric SAR data shown in Figure 9 (a). A comparison between two other algorithms for various map elevations (on various range lines) is shown in figure 9 (c). Referring to the figures, our enhanced smart vision chip is able to reconstruct the 3D Sardegna image quite accurately. Moreover, the smart vision chip will be able to do the reconstruction with bandwidths exceeding 100 Hz.

Intelligent Star Tracker Application:

Current state-of-the-art commercial star sensors typically weigh 15 pounds, attain 5 to 10 arc-second accuracy, and use roughly 10 watts of power. Unfortunately, the current state-of-the-art commercial star sensors do not meet many of NASA's "next-generation" spacecraft and instrument needs. Nor do they satisfy Air Force's need for micro/nano-satellite systems. In this paper we present a low cost, miniature Intelligent Star Tracker for spacecraft attitude determination and navigation. Our Intelligent Star Tracker illustrated in Figure 10 incorporates adaptive optic catadioptric telescope in a single, compact, robust Silicon Carbide housing. The MOEMs micro-mirrors are used to compensate for various aberrations as well as introduce aberrations such as defocus to ensure optimal system performance.

Leveraging off of our adaptive optics research, our active pixel position sensors enable wide dynamic range and simultaneous imaging of faint and bright stars in a single image frame. The adaptive optics telescope, using, MOEMs micro-mirrors, enables extremely accurate tracking. When coupled with our star matching scheme based on algebraic coding theory, the active optic technologies enable fast and accurate star pattern recognition to support guidance navigation and control (GN&C).

The massively parallel processing architecture designed into the Intelligent Star Tracker not

only enables very high bandwidths, exceeding 40 Hz, but also enables tracking of at least 5 stars simultaneously. Moreover, the massively parallel architecture enables the star tracker to operate autonomously without burdening the spacecraft processor and may be used to supplement the onboard processor. Because our design utilizes technologies that inherently integrate well together and lend themselves to batch processing, we estimate that the Intelligent Star Tracker will have a recurring cost less than \$100k. In addition to low cost, preliminary analysis indicates that our Intelligent Star Tracker will have a pointing accuracy Tracker will have a pointing accuracy exceeding 0.20 arc-sec, NEA better than 0.10 arc-sec, power consumption less than 2 W and a weight of approximately 0.20 Kg.

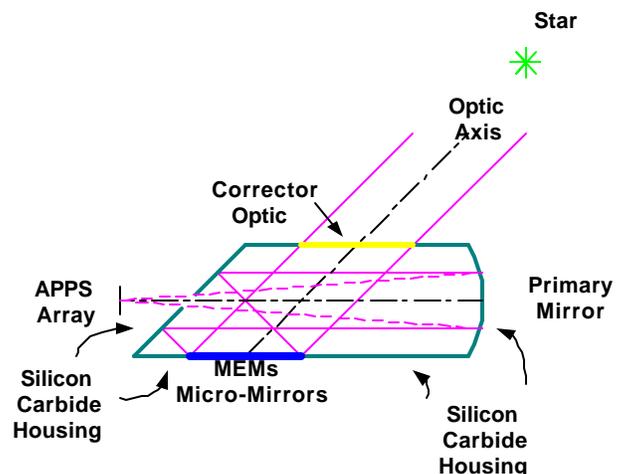


Figure 10. Intelligent Star Tracker.

ACKNOWLEDGEMENTS

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