Command and Data Handling Subsystem Design for the Ionospheric Observation Nanosatellite Formation (ION-F)

John D. Jensen, Utah State University
Dr. Charles M. Swenson (Advisor), Utah State University

ABSTRACT

This paper describes the approach taken by the ION-F student team in designing a common Command and Data Handling (C&DH) subsystem for three different nanosatellites. It outlines the requirements of the satellites and reasons behind the decision to develop a custom board. The design is based upon industrial-grade components and centered on a Hitachi SuperH RISC Processor. The C&DH subsystem contains a 16 MB telemetry buffer, a digital and analog interface subsystem, and a DMA-oriented CMOS camera framebuffer. Students are fabricating these boards with the assistance of Space Dynamics Laboratory at Utah State University. This design will be flown by three different satellites, which are all part of a single formation-flying mission.

INTRODUCTION

The Air Force Office of Scientific Research (AFOSR) and the Defense Advanced Research Projects Agency (DARPA), along with various industry partners, are jointly funding ten universities to design and assemble ten nanosatellites (~15 kg). The objective of this program is to demonstrate the military usefulness of nanosatellites in such areas as formation flying, attitude control, maneuvering, and communications. Each university will receive $100k over a two-year period for spacecraft development and construction.[1] These satellites constitute the secondary payload of an upcoming International Space Station construction mission. Due to the nature of the Shuttle's primary payload, the satellites will be deployed into a circular low-earth orbit of approximately 380 km at an inclination of 51.6-degrees. The life expectancy of the satellites is one year.

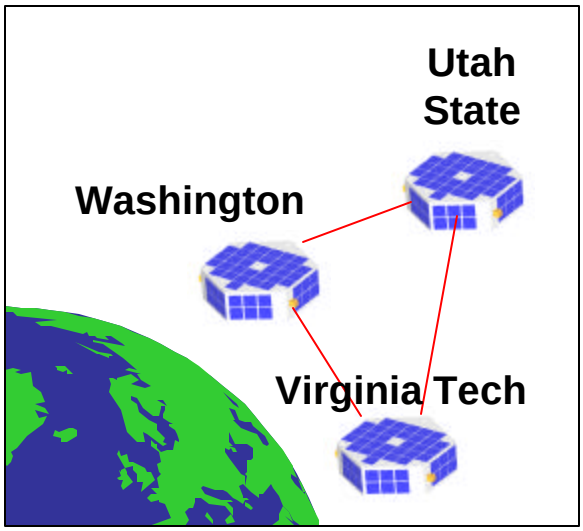

Figure 1. ION-F Formation.

In order to demonstrate formation-flying capabilities, it was necessary to form partnerships between several universities. Utah State University (USUSat), University of Washington (Dawgstar), and Virginia Polytechnic Institute (HokieSat) have teamed together to create the Ionospheric Observation Nanosatellite Formation (ION-F). Additional benefits, such as design collaboration and resource sharing, have been gained from this partnership.

ION-F is expanding the satellite frontier with innovative nanosatellite technologies. It is pioneering the development of new formation-flying algorithms and the evolution of low-cost distributed satellite clusters. ION-F will conduct the first multi-satellite study of electron density structures in the ionosphere.

The purpose of this paper is to describe the approach and design taken by the student team for the ION-F Command and Data Handling (C&DH) subsystem. This design meets the requirements for mission success. This paper is divided into three sections: Subsystem Requirements, Design Approach, and Design Implementation. The first section is Subsystem Requirements, which discusses the imposed requirements and the underlying reasoning. Next, the Design Approach section outlines the C&DH options available to ION-F and the final design choice made. This is followed by a detailed outline of the design. The last section is Design Implementation, which discusses how the design approach has been implemented.

SUBSYSTEM REQUIREMENTS

Design collaboration is a key benefit of the ION-F partnership. Each satellite in ION-F will share a common C&DH subsystem. To accomplish commonality, the C&DH design requirements must satisfy the needs of each satellite in the formation. There are eight formal design requirements. These are low cost, real-time operating system support, radiation survivability, thermal survivability, support of various interface types, large telemetry storage, low power consumption, and computational robustness.

Interfaces for Satellite Subsystems

A system-level diagram, which outlines the various subsystems of an ION-F satellite, is presented in Figure 2. Each ION-F satellite is three-axis attitude controlled, requiring sun, Earth horizon, and geomagnetic field measurements. The C&DH subsystem also provides control of thermal, power, and telemetry subsystems as well as command over various deployment mechanisms.

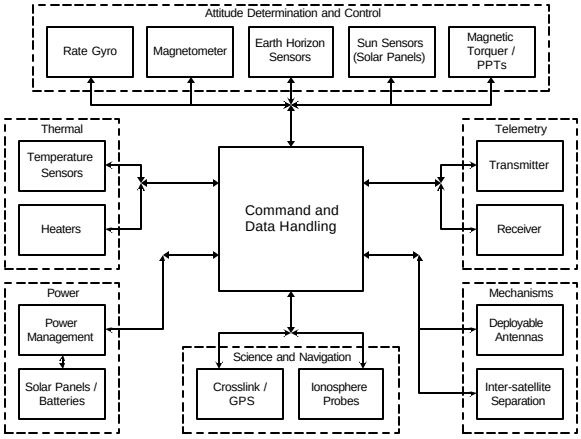

Figure 2. System-level interface diagram for C&DH subsystem.

Unique to ION-F, among small satellites, is a Crosslink/GPS system being provided by Applied Physics Laboratory. This will allow the satellites to directly determine their relative position in the constellation and pass messages to each other. Two of the satellites will use Pulse Plasma Thrusters (PPTs) to adjust their positions during formation flying. The third will use atmospheric drag and lift forces to affect its position within the formation. The Ionospheric measurement instruments require significant data handling and storage capabilities when compared to other subsystems. The C&DH design needs to support three interface types: analog, digital, and serial. Certain subsystems provide analog signals (e.g. rate gyro, magnetometer, solar panels) while others provide digital signals (e.g. magnetic torquer, PPTs, power management), hence the need for both types of interfaces. The telemetry equipment and satellite development tools require a serial interface.

To reduce the amount of cabling within the structure, a proprietary 1-wire bus (bi-directional digital bus consisting of a single wire) should be provided for various sensors distributed throughout the spacecraft.

Large Telemetry Storage

ION-F will be the first distributed satellite formation to investigate the electron density irregularities of the ionosphere. To advance our understanding of these irregularities, it is desirable to collect as much data as possible. However, access time to ground-stations limits the amount of data that can be collected. These restrictions on the telemetry subsystem also distinguish ION-F from other small satellites. Each of the three ION-F satellites must share a single frequency allocation. This requires the satellites to share overpasses round-robin style when they are close to each other in the sky.

The rate which data (scientific and housekeeping) can be collected was simulated assuming a 100kbps downlink. Later in the mission, as the formation descends, access times will shorten, and intersatellite distances will increase. This allows each satellite to be tracked individually by the ground-station, and the round-robin technique will not be needed. Various scenarios were considered based on altitude and ground-station configuration. It was determined that 1kbps of data could be collected continuously by each satellite and returned to the ground. At this collection rate, a storage buffer of 16 megabytes is required as a result of frequency allocation sharing and periods between ground-station accesses.

Low Power Consumption

Power consumption is an important design consideration because of the small physical nature of the ION-F satellites. Each satellite is hexagonal in shape with an approximate diameter of 18” and heights varying from 6” to 12”. The surface area for mounting solar cells is significantly reduced compared to conventional satellites, which results in less power generation ability. Deployable panels were not an option due to complexity and safety concerns. Each university has performed power analysis calculations, and created a power budget for the various subsystems. After taking into consideration the requirements of power intensive components, such as thrusters and the Crosslink/GPS

unit, the C&DH subsystem has been limited to an orbital average power of 3 watts. This amount is a fraction of the power consumed by conventional satellite designs, given the system requirements.

Computationally Robust
The C&DH subsystem is required to control various subsystems and perform many operations at approximately the same time. The formation-flying mission requires each satellite to perform a Kalman-filter based navigation algorithm for the entire constellation. The Earth horizon sensors generate multiple 256-kilobyte images at approximately 10 Hz. These large images must be processed to determine the satellites orientation. The C&DH subsystem also executes a Kalman-filter based three-axis attitude control model, which takes into account spacecraft dynamics and disturbance torques. Each of these calculations and models must be performed at the same time that data is collected, formatted, and stored in the telemetry buffer. These are just a few examples of the loads that will be placed on the C&DH subsystem. It is estimated that approximately 20 million instructions per second (MIPS) are required to perform these operations.

In order to achieve each of these tasks in a timely fashion, the C&DH design must be computationally robust. This includes both execution speed and resource availability.

Low Cost
Being more stringent than most other programs, cost was an important consideration during the system design of the ION-F satellites. Even though the student/university nature of the program significantly reduces the associated labor expenses, cost has a large impact on the C&DH design. This is due to the design requirements and relatively low funding of the program. Space-qualified components are historically expensive and must be used sparingly to keep within the allotted budget. As the satellite community transitions towards inexpensive distributed nanosatellites, new methodologies need to be employed to replace traditional design techniques. ION-F research will contribute to the development of these cost saving methodologies.

The goal of the C&DH design is to minimize component expenditures while still providing the reliability necessary for mission success.

Real-Time Operating System Support
Certain events, such as data collection and formation-flying control, must be executed with strict timing accuracy. These timing requirements, as well as the complexity of software design, dictate the need for a real-time operating system (RTOS). Various operating system choices are available, such as uCos, eCos, and VxWorks.

There are two important considerations to weigh during the selection of an operating system for this project. The first is providing a beneficial and educational experience for students. VxWorks is the RTOS of choice for a large portion of the embedded-applications industry. Students with VxWorks experience are attractive to these types of employers. The second consideration is supporting commonality and portability with the necessary sponsors. NASA Goddard uses VxWorks and is providing portions of the formation-flying algorithms.

WindRiver Systems, who produces VxWorks, has pledged their support by providing ION-F with VxWorks at a significantly reduced price. The C&DH subsystem design must support VxWorks through a WindRiver's authenticated board support package (BSP).

Radiation Survivability
An important issue to consider, which affects all electronic devices in space, is radiation. Radiation can lead to various types of problems. These problems range from operational malfunctions to physical damage of the devices. Radiation effects can be broken into two categories: total radiation dose and single-event effects (SEE).

Studies performed at Utah State University have analyzed the total effects of radiation based upon the given mission parameters (i.e. orbit, inclination, life expectancy, and launch date). Using radiation models developed by NASA, the studies determined that the satellites will experience a total radiation dose of approximately 25 rads. Typical CMOS technology devices can survive nearly 5 krads before physical damage occurs.[2]

However, single-event effects are significantly more hazardous to ION-F and can result in either bit-errors or device latch-up. Bit-errors are internal device memory changes that can cause erroneous operation. These are considered soft-errors and do not cause physical damage to the devices. In contrast, device latch-up is a hard-error, which leads to a high current-flow through the device. If not remedied quickly, latch-up can cause permanent damage. The USU study estimates that the satellites will experience approximately four bit-errors per day, and only a small percentage of these will result in a latch-up condition. If one in a thousand events cause latch-

up, ION-F will observe less than two latch-ups per year.[2]

Shielding electrical components can reduce the effects of radiation. ION-F's structure will provide some shielding of the C&DH subsystem, but design (i.e. size and mass) constraints of nanosatellites render this approach impractical to minimize radiation effects. Operating devices at slower frequencies also reduce the probability of single-event upsets. Designs should function using the slowest clock rates possible that yield acceptable performance.

Based on ION-F's mission parameters, the total dose effects are negligible and can be ignored. In contrast, single-event upsets significantly affect the design. The C&DH subsystem does not need to be immune to these effects, but provisions to recover from bit-errors and latch-ups are essential for a reliable design.

Thermal Survivability

Thermal issues for electronics in the space environment are significantly different than for electronics operating at the Earth's surface. When operating within an atmosphere, components can be cooled by air convection, but convection is not possible inside a vacuum. Therefore, special design attention must be given to insure that heat will be conducted away from the components.

Temperature extremes are expected for ION-F, and the C&DH subsystem needs to survive exposure to these limits. Circuit board designs need to provide conduction planes to aid in heat removal, and components need to have a wide temperature range of operation. Likewise, accommodations for internal heat generation should be provided. In addition to these measures, thermal engineers will perform system-level design analysis and make modifications to attenuate thermal fluctuations.

Requirements Summary

As the satellite industry becomes more commercialized, large expensive satellites will give way to multiple inexpensive nanosatellites. However, the requirements of nanosatellites are significantly different from their ancestors, and new design techniques are needed to meet these evolving requirements. The unique requirements of ION-F demonstrate this evolution. To summarize, the design needs to be relatively inexpensive while at the same time computationally robust. It must support the space environment by reducing susceptibility to radiation and thermal effects. It should provide the necessary interfaces for each subsystem and consume limited power. To meet the science objective, large amounts of data need to be stored, and VxWorks must be supported.

DESIGN APPROACH

Commercial Solutions

When design of the C&DH subsystem began, ION-F investigated commercial off-the-shelf (COTS) boards for use as a flight computer. Initially, ION-F's focus was towards the TattleTale® Model 8 produced by Onset Computer Corporation. The Model 8 supports the necessary interface requirements and consumes very little power. However, interfacing additional memory for telemetry data storage is nearly impossible without making significant modifications to the board. Radiation susceptibility is another problematic issue. The Model 8 stores firmware in Flash memory, which is susceptible to bit-errors. If these errors occurred in the system's boot-area, the satellite would be unable to recover and continue the mission. Replacing the Flash memory with a radiation-hard device (e.g. Fused-PROM, Rad-Pak®) would be difficult and impractical. Finally, the Model 8 did not support VxWorks through an authenticated BSP. Another solution needed to be found.

ION-F continued to search for other COTS options. Most boards complied with the interface requirements, and a few supported PROM-based firmware. Some had an authenticated VxWorks BSP, while others consumed little power. However, none met all of the necessary requirements.

Custom Solutions

The next step for ION-F was to investigate the design of a custom computer board. To begin the design, a suitable microprocessor architecture needed to be chosen. Various commercial architectures are available, such as the Motorola M-Core® and 68300, the Hitachi SuperH®, and the Intel StrongARM® (and compatible) series. Along with these micro-controllers, ION-F also investigated a few "stamp" processors, but these were dismissed because of marginal computing performance. Cost and power requirements eliminated the ability for ION-F to use Rad-Pak®-based processors from Space Electronics.

The first family examined was the Motorola 68300 series, which is also used by the TattleTale® Model 8 (MC68332). If the flight computer design is based on the MC68332, subsystem prototyping could be performed with the Model 8 and easily transitioned to the final design. However, the micro-controller's

address space is limited to 16 MB, and a paging technique needs to be employed to accommodate the storage requirements of the science mission. The MC68332 is computationally robust and consumes little power, but the existing (compatible) VxWorks BSP has not been authenticated. The remaining members of the Motorola 68300 family are similar to the MC68332, only varying by the type of internal peripheral modules available.

The Motorola M-Core series was scrutinized briefly. Only one model supports the interface requirements of ION-F, but its address space is limited to 4 MB. Interfacing this device with the amount of memory needed would be difficult and unacceptable.

While Utah State University and the University of Washington were pursuing Motorola-based options, Virginia Polytechnic was prototyping a system based on an ARM processor from Sharp Electronics. Most ARM processors fit the cost, power, computation, and memory requirements of ION-F. However, ARM devices are processor-oriented in nature and tend to lack sufficient digital interface ports. Another drawback of ARM devices is that few are supported by authenticated VxWorks BSPs. Virginia Polytechnic consulted several members of industry concerning VxWorks development. As a result of this investigation, they learned that the development environment runs slowly on most ARM processors, which is a side effect of an unbuffered serial interface. Due to the lack of ample digital interfaces and buffered serial ports, Virginia concluded that ARM processors are not an "optimal" solution. Adding these necessary features would require external components, which increases power consumption and mass.

There are numerous choices within the Hitachi SuperH® family of RISC processors. Like the Motorola families, each is based around a common core with varying peripheral modules. Selecting a suitable device for ION-F was trivial because various interface configurations exist. The most complicated issue with selecting a Hitachi processor is choosing one that can be delivered within the time allotted. Most are on allocation and have long lead-times. After consulting many distributors, the SH7709 seemed to be a viable choice. It is inexpensive, computationally robust (80 MIPS), consumes little power (330 mW), and fully supported by VxWorks. The SH7709 also provides three serial interfaces, two of which are buffered, and a large number of input/output ports for digital interfacing.

Approach Analysis

In general, COTS boards are developed for use in mass-marketed applications. To increase the potential customer base, these boards support a wide variety of general-purpose features. In contrast, nanosatellites have specific requirements. These constraints make general-purpose designs inefficient. After reviewing the options available, the ION-F team decided that it is necessary to design a custom board for the C&DH subsystem. The Hitachi SH7709 microprocessor is at the center of this design. There are three driving reasons behind this decision. The first is power consumption. The commercial products that conformed to the interface and memory requirements consumed an unacceptable amount of power. Second, to survive the effects of radiation, firmware needs to be stored in radiation-hard or redundant memory. Lastly, the boards need to be able to detect latch-ups and reset accordingly. Implementing the two latter issues on COTS boards would require significant modifications.

Due to the extraordinary cost and size restrictions of ION-F, reliability compromises need to be made within the design process. Although these compromises require accepting the risk of failure, the environment to which ION-F is exposed is relatively mild. To ensure thermal survivability, the design will be constructed with industrial-grade components. These are less expensive than the space-qualified counterparts, but rugged enough for the orbit and life expectancy of ION-F's mission. However, provisions for single-event upset recovery must be accounted for in the design. In addition, circuit boards are manufactured using the appropriate industrial processes.

The top-level diagram for the C&DH subsystem is shown in Figure 3. Because of board size limitations (4.9" x 3.0") imposed by the electronics enclosure, the C&DH subsystem is divided into four functional sections. Each section is implemented as a single board interconnected through a backplane interface. These are the CPU Board, Telemetry Board, Camera Board, and Input/Output Board. Detailed descriptions of each board are discussed in the sections that follow.

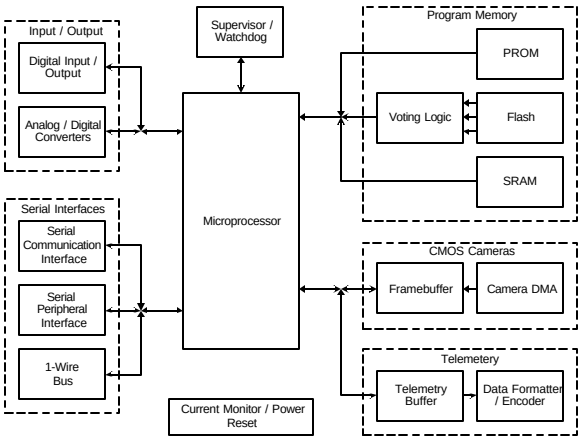

Figure 3. Top-level interface diagram for C&DH subsystem.

Single-Event Effects Recovery Scheme

Designing a C&DH subsystem that is somewhat radiation tolerant is arguably the most difficult design requirement to satisfy. Unlike larger satellites, ION-F's limited budget makes the use of only space-qualified and radiation-hardened devices impractical. The nature of ION-F's small size also eliminates the possibility of a completely redundant design. In spite of these two constraints, the design must be reliable and survive the effects of radiation. The delicate balance between cost, size, and reliability makes the ION-F design unique. As mentioned in the system requirements, total dose radiation can be considered negligible for ION-F, but single-event effects need to be considered throughout the design.

Although rare, latch-up situations present the greatest hazard to the C&DH subsystem. A latch-up event results in an abnormally high current-flow through a device. This current-flow can be several orders of magnitude larger than the device's typical operating range and generates an enormous amount of internal heat. Power-cycling the device is the only feasible remedy for clearing a latch-up condition. If not promptly performed, permanent damage to the device can result from the excessive heat. The C&DH design must be able to detect high current-flow through each board and cycle power accordingly.

The latch-up recovery design consists of two scenarios. The first scenario considers latch-ups that occur on any board other than the CPU Board. Using high-side current monitors, each board within the electronics enclosure monitors its current-flow. If the current-flow into a board rises above a pre-determined reference level, the current monitor signals the CPU Board via a shared interrupt (highest priority). The CPU determines which board needs to be reset and measures its current-flow. Finally, the CPU provides a reset signal to the board's power-cycling circuitry and logs the event. The second scenario covers the situation when the CPU Board experiences a latch-up. This scenario is similar to the first except that the power subsystem controls power cycling of the entire satellite. High-side current monitors located on the CPU Board monitor the current-flow into the board. When the current-flow into the board rises above a pre-determined level, the CPU Board notifies the power subsystem. The power subsystem subsequently cycles power to the entire satellite.

The power-cycling interface for each board is composed of redundant BJT/MOSFET pairs, which lie between the backplane power connection and the power pins of the components. A signal to the gate of the BJT controls current flow through the MOSFET. Large feature-width BJTs and MOSFETs are effectively immune to radiation.

Unlike latch-up conditions, bit-errors are difficult to detect. Bit-errors are logic value changes (binary 0 to 1 and visa versa) within the storage cells of a device. This can result in numerous side effects, such as erroneous calculations, instruction and data corruption, erratic software execution, and operation setting changes. Several approaches can be taken to detect and correct these types of errors. Two possible solutions for memory devices are error-correction coding and redundancy. Both solutions require additional storage devices, which adds a significant cost to the design.

Processors and digital logic devices also suffer from these issues. However, the same solutions typically cannot be applied. For example, error-correction coding is impossible to perform on the internal registers of an ordinary processor. In a redundant design, a malfunctioning processor could fight for control of the address and data buses. A third option to consider is the use of radiation-hardened devices. These offer a degree of immunity against radiation effects, but few processors are available in this type of package.

Software execution is an additional problem that is specific to processors. Instructions may become corrupted while stored internally (register) or externally (memory). These errors could lead to malicious or illegal instructions. Changes to the stack pointer could affect parameter passing and software execution of subroutines. Similarly, instruction pointer changes might refer to an address from which normal software execution cannot return.

Using these examples, it is clear that a monitoring technique needs to be employed to recover from software failure. Several of the above techniques are combined to form the recovery scheme for ION-F.

Modifications to software instructions stored in memory are an extremely hazardous type of bit-error. If these modifications occur in the satellite's boot-loader, the operating system would not be able to restart properly. Errors of this type must be avoided because they compromise mission success. To prevent software changes, the firmware will be stored in a radiation-hardened PROM. However, the ability to update routines and algorithms in-orbit is desirable. To allow for these updates, flash memory will be integrated into the design. Since flash memory is susceptible to bit-errors, a redundant design is implemented. This protects the integrity of software updates while maintaining flexibility. The design of this redundant scheme is discussed in the CPU Board section below.

Even though software is protected by an external memory scheme, it is possible for instructions to be corrupted within the processor. To safeguard against software stalls, redundant watchdog timers monitor the continuous execution of instructions. Two timers are implemented in the C&DH design. Periodically, the RTOS process manager produces a pulse to clear each timer. If these timers are not reset within a specified period, the watchdogs generate a signal that resets the processor. However, a software stall can be caused by bus contention between two boards. To account for this possibility, a logic circuit on the power board counts each reset event. If three reset events occur consecutively, the power subsystem will cycle power to the entire satellite.

In the event that the CPU countermeasures fail, the power subsystem performs a satellite reset at regularly scheduled intervals. A system reset can also be commanded after a telemetry session. To ensure reliability, the power subsystem logic design is implemented as redundant combinatorial cells in an Actel anti-fuse FPGA. Logic designs using combinatorial cells are significantly less susceptible to radiation.

To account for bit changes within operating mode registers, software should periodically reconfigure each digital device. Bit errors that occur in calculations and data collection do not influence overall mission success. These errors can be detected and corrected through software by performing redundant sampling and multiple calculations. The rate at which certain algorithms are performed also negates the effect of a single miscalculation.

CPU Board

The CPU Board is the heart of the C&DH subsystem and operates constantly. A top-level diagram of the design is shown in Figure 4 below. The CPU Board performs three distinct functions. These are computation, general-memory storage, and single-event effect monitoring.

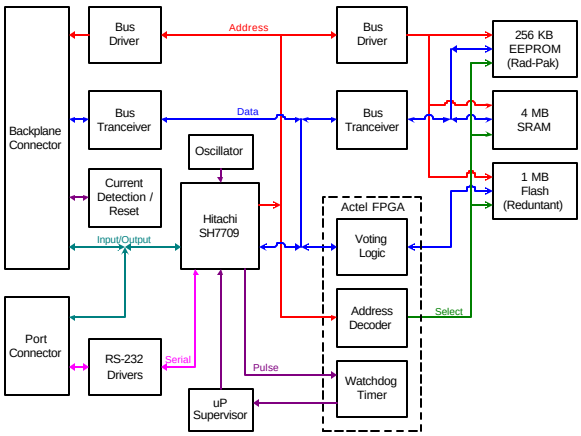

Figure 4. Top-level diagram of CPU Board.

The computation unit consists of the Hitachi SH7709 microprocessor. The SH7709 possess many features that fulfill the C&DH system requirements. It is a low power device that consumes only 330 mW of power during peak operation. Coupled with other low power components, the CPU Board draws less than 1.25 W. Although it consumes little power, the SH7709 is a powerful 32-bit RISC-based microprocessor capable of executing 80 million instructions per second. This is sufficient for ION-F's complex formation-flying and attitude determination algorithms. Portions of these algorithms require the use of a Kalman filter. To increase filtering accuracy, the SH7709 provides a 64-bit multiply-and-accumulate register.

The SH7709 offers a wide range of interface options. These include 96 digital input/output pins, eight analog channels with 10-bit resolution, and three serial communications interfaces. Unlike other micro-controllers, the function of each digital I/O pin can be individually configured. These pins have a 3.3V input tolerance and are used to interface with various subsystems inside and outside the electronics enclosure. The three serial communication interfaces (SCI) can operate in either synchronous or asynchronous modes, and two interfaces are buffered with a 16-byte FIFO. These three serial interfaces

are used by the receiver, Crosslink/GPS, and software development tools.

The microprocessor's 384-megabyte address space easily supports the telemetry requirements, and an authenticated VxWorks BSP can be supplied. The SH7709 also contains features to aid in radiation and thermal survivability. An internal watchdog complements the single-event upset recovery scheme, and Hitachi offers this device in an industrial-temperature version (-40° C to 85° C).

The CPU Board's memory configuration consists of three types of memory: EEPROM, Flash, and SRAM. The flight-version of the satellite's firmware is stored in EEPROM. Even though EEPROM is typically soft to radiation effects, this design uses a Rad-Pak® device that nearly eliminates radiation susceptibility. Power and performance were two reasons for choosing an EEPROM over a normal PROM device. The equivalent PROM component consumes more power and has slower access times. The ability to reprogram EEPROMs during prototyping is an additional benefit.

To provide the flexibility of software updates while in-orbit, AMD Flash memory has been integrated into the C&DH subsystem. Since Flash memory is typically soft to radiation effects, the CPU Board implements a redundant design (see Figure 5). This scheme is based on the majority-voting logic used by high-reliability FPGA designs. Probability is the underlying theory with this approach. The theory assumes that the probability of multiple single-event upsets changing the same bit in two different devices is extremely rare.

The data bus from three identical Flash devices is connected to one side of the voting logic, while the microprocessor's data bus is connected to the other side. The microprocessor presents a common address, as well as the respective control signals, to each Flash device. During read transactions, data output from each Flash device enters the voting scheme. The bits from each device are compared, and the assertion level of the majority result is output to the microprocessor's data bus. For write transactions, data from the microprocessor bus is passed through the voting scheme and copied to each Flash device. Direction control signals are decoding using the logic shown at the bottom of Figure 5.

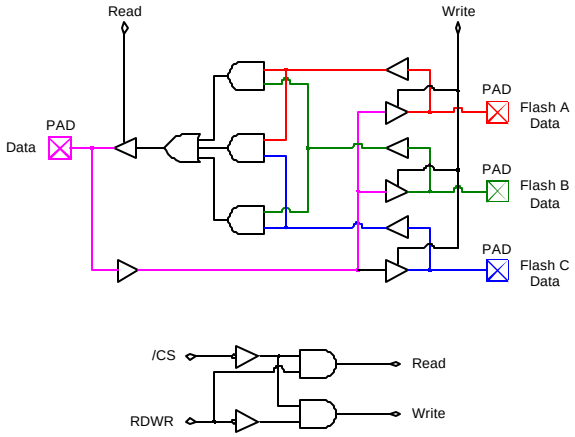

Figure 5. Majority-result voting logic for Flash memory.

An important advantage to this redundancy scheme is transparent operation. The microprocessor can fetch and execute instructions from Flash memory without checking the op-codes for accuracy. Error-correcting codes could have been implemented, but the instructions must be corrected by a software routine before the processor is allowed to fetch them. The additional memory and board spaced saved by using error-correcting codes is marginal when compared to the software complexity added.

The third type of memory provided by the CPU Board is general-purpose SRAM. This design uses new low power devices from Samsung, which consume less than 15 mW when active. Both the operating system and user processes share portions of this memory. This memory is used to store such items as variables, data, and the system stack. Because single-event errors within the SRAM section do not cause critical failures, provisions for bit-error correction are not implemented. Because software instructions are not stored in SRAM, a software-based error-correction scheme could be implemented for additional reliability. An example of this is data scrubbing. Data scrubbing is the process of reading and rewriting each piece of data in memory.

The CPU also performs single-event upset monitoring. As described in the latch-up detection scheme, the processor will measure and log the current-flow of each latched-up board. This measurement is taken using the analog inputs of the SH7709. An interrupt request line is used to notify the CPU Board of the latch-up condition. The bit-error detection scheme states that two watchdog timers are used to monitor software execution. One watchdog timer is internal to the SH7709; the other is implement in an Actel FPGA. The real-time

operating system produces a pulse every few seconds. These pulses will clear the watchdog timers. If software execution stalls, the real-time operating system will not be able to provide the necessary pulses. This will cause a reset

Telemetry Board

The Telemetry Board stores PCM pages that are to be transmitted during ground-station access. The board is implemented using a DMA-oriented design (see Figure 6). The CPU organizes data into PCM pages and stores them within the Flash memory located on the Telemetry Board. Prior to a telemetry access, starting and ending addresses of valid pages are written to registers on the board. When a telemetry access begins, the Flash memory's data bus disconnects from the microprocessor, and a FPGA located on the Telemetry Board begins reading data from the Flash memory. This data is serialized and streamed to the transmitter. At appropriate locations, frame synchronization words and real time data from the CPU Board are inserted into the stream. This process continues until all the valid data has been transmitted. If necessary, the telemetry process can be interrupted and restarted at an appropriate location. Bit-error detection and correction are not implemented on the Telemetry Board since infrequent errors in the telemetry stream are not catastrophic to mission success.

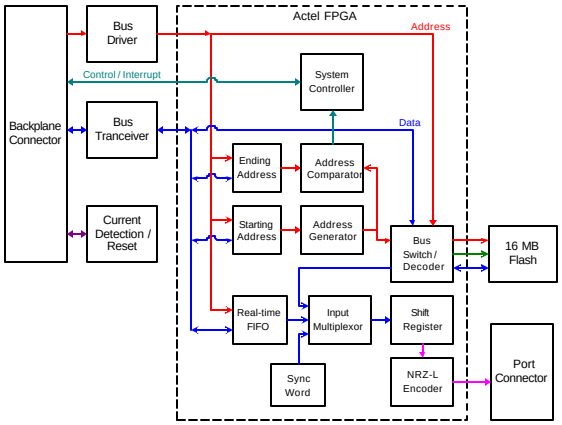

Figure 6. Top-level diagram of Telemetry Board.

Camera Board

For attitude determination algorithms, ION-F uses several (four to eight) small CMOS cameras to provide Earth horizon and sun position information. Each camera is a Fuga 15d from C-Cam Technologies.

There are two interface options for connecting these cameras to the C&DH subsystem. The first is to connect the cameras through a serial communications interface (SCI). To read a pixel (picture element) using this technique, the microprocessor transmits both a horizontal and vertical coordinate to the camera. After a short period of time, the camera returns the intensity value (8-bit) of the corresponding pixel. The microprocessor could use this data immediately or temporarily store it in SRAM. To read an entire image (512 by 512), the microprocessor could request that every pixel be transmitted sequentially, which takes approximately 20 seconds. During this time, the microprocessor continuously services the capture routine.

The second interface option is via the address and data buses. Each pixel is represented by a unique address in the microprocessor's memory space. To read a pixel, the corresponding memory address is placed on the address bus, and the intensity value is returned on the data bus. Because the Fuga 15d only operates at 500 kHz when modifying the y-address, this technique requires the insertion of several bus wait states. To capture an entire image using this technique takes approximately 600 ms. Similar to the SCI option, this scheme requires the microprocessor to actively perform image capturing.

When comparing these two options, it is apparent that the bus interface scheme is significantly more efficient. However, overall system performance is hindered by the insertion of wait states. The Camera Board implements a DMA-oriented hybrid, which removes the effect of these wait states (see Figure 7). This allows the microprocessor to perform other operations while the image is being captured and stored in SRAM. The acquisition times listed above are for a single camera. To increase performance further, the hybrid implementation performs simultaneous image capturing of each camera.

Prior to initiating a capture request, the microprocessor sets two registers on the Camera Board: the warm-up counter and the operation mode register. During periods of inactivity, the cameras are turned off to conserve power. In order for the camera's automatic-gain control to function properly, the cameras require time to adjust before capturing begins. The warm-up counter allows for a variable-length adjustment period. Once the cameras have adjusted, they are initialized with the operation mode register. Next, each pixel is sequentially read from the cameras and stored in SRAM located on the Camera Board. When the capturing process completes, the cameras are turned-off, and the CPU Board is notified via an interrupt. Algorithms can

directly access the image data stored in the Camera Board's SRAM.

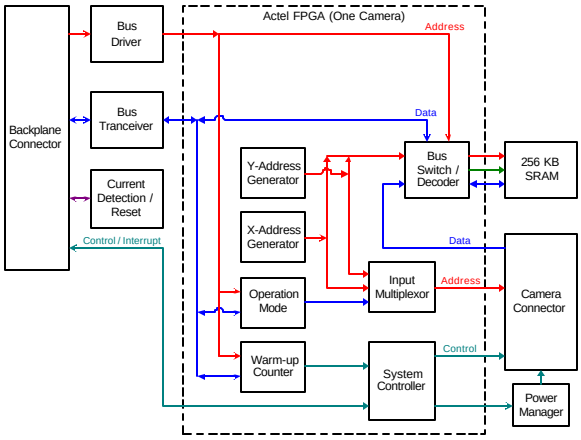

Figure 7. Top-level diagram of Camera Board.

Input/Output Board

The Input/Output (I/O) Board provides digital and analog interfaces to subsystems outside the electronics enclosure. To add flexibility for different satellite designs, each interface is configurable through software. The I/O Board supports 16 bi-directional digital lines and 32 analog inputs. Unlike the 3.3V digital interface supplied by the CPU Board, these digital lines operate at 5V levels. The analog inputs are separated into two categories based on ADC (analog-to-digital converter) precision. Sixteen of the inputs have 12-bit precision while the remaining inputs have 16-bit precision. The 12-bit inputs can be configured to one of four tolerance ranges: 0V to 5V, 0V to 10V, -5V to 5V, and –10V to 10V. However, the 16-bit inputs only accept 0V to 5V sources. Software routines select the appropriate input and tolerance range for the signal that is to be sampled. Each analog interface half is implemented using a single ADC. These are connected by a 16 to 1 analog multiplexor. By using a single ADC and multiplexor for each half, the overall part count is reduced. This aids in power conservation and eliminates unnecessary mass. Since the ADCs are sampled at low rates, this method does not hinder system performance.

A third function of the I/O Board is providing a serial peripheral interface (SPI). This interface is internal to the electronics enclosure and is used to communicate with various serial subsystems (i.e. ionosphere probes). Unlike the serial interfaces supplied by the CPU Board, the SPI bus is shared among several devices. The SPI bus can support connections with up to 32 devices, but these connections must be initiated by the C&DH subsystem.

DESIGN IMPLEMENTATION

Currently, ION-F is finalizing the designs of the C&DH subsystem. Schematic capture, FPGA design, and board layouts are being performed using VeriBest design tools. The boards will be multi-layered with a thermal core and populated with surface mount components. Space Dynamics Laboratory is assisting with the board layout and fabrication, and prototype fabrication is scheduled to start during the first week in September of 2000.

Each university in ION-F is contributing portions to the C&DH design. Utah State University is providing the CPU Board, Telemetry Board, Camera Board, and Backplane. Virginia Polytechnic is providing the I/O Board and power subsystem FPGA, and the University of Washington is providing the electronics enclosure. Each university is contributing to software development.

SUMMARY

The custom design outlined in this paper satisfies each of the system requirements for ION-F. By using the latest industrial-grade components, a low-cost and power efficient solution is provided. This solution also provides the environmental robustness and computational performance required for success of each mission objective. As nanosatellite technologies continue to progress, this design will be refined and expanded upon. The modular nature of the design allows various boards to be reused and upgraded as future applications may require.

The universities of the ION-F team would like to recognize the following government and industry sponsors for providing additional assistance in developing the C&DH subsystem:

L3 Communications (Telemetry equipment)
NASA Goddard Space Flight Center (Funding)
NASA Office for Scientific Studies (Funding)
Space Dynamics Laboratory (Funding/Mentoring)
WindRiver Systems (VxWorks)

REFERENCES

1. M. Martin et al, "University Nanosatellite Program," IAF Symposium, Redondo Beach, CA, 1999

2. Pisacane, V. L., and R. C. Moore, 1994. Fundamentals of Space Systems. New York: Oxford University Press. pp. 690-717.