LOW-COST QUICK-LOOK RADIATION TESTING OF ELECTRONIC COMPONENTS FOR THE MARS OBSERVER CAMERA

S. M. Brylow and T. A. Soulanille*
Altadena Instruments Corporation
Pasadena, California 91105

Abstract

The development of modern electronics has far outstripped the inventory of components for which radiation tolerance has been determined and published. New component characteristics require a more integrated approach to radiation tolerance in system design. The Mars Observer Camera performance requirements could not be met with a design restricted to components of established radiation hardness. A balanced approach that intimately involved radiation effects in the system design process was required. This included low-cost, quick turnaround testing of total ionizing dose and heavy ion induced single event phenomena of upset and latchup. The results were used to inform the system design, which had to adapt to real component susceptibilities. Test results directly affected component selection, radiation shielding, and the data path and software architectures.

1. Introduction

Radiation resistance of electronic components is a significant factor in system design for a variety of earth-orbiting and interplanetary missions. To illustrate how radiation concerns interact with system design, this paper discusses radiation tolerance issues in the design of the Mars Observer Camera (MOC).

The NASA Mars Observer mission, managed by the Jet Propulsion Laboratory (JPL) and planned for a late September 1992 launch, involves a year of interplanetary cruise followed by one Mars year (two Earth years) of mapping orbits. Dr. Michael Malin is the Principal Investigator for the MOC, the camera on Mars Observer. Caltech was responsible for designing and delivering the instrument; Altadena Instruments provided systems and detailed engineering for that effort.

The principal science objectives of the MOC investigation require targeted meter-scale resolution images of kilometer-scale scenes, and global coverage of Mars at kilometer-scale resolution in red and blue colors on week time scales. The MOC high resolution imager uses a CCD line array of 2048 photosensitive elements in a pushbroom configuration at the focal plane of a 35 cm aperture reflecting telescope. Its 0.42° field of view covers 3 km at 1.5 meters per pixel from a 380 km polar sun-synchronous orbit. Two wide field (140°) imaging systems use similar CCD's with 3456 photosites to cover Mars limb-to-limb in red and blue bands at 250 meters per pixel at the nadir. (The MOC investigation is described in[1] and the instrument development in[2].)

2. System Requirements

The MOC is nadir-fixed on the spacecraft. The ground-track speed, the required resolution and number of pixels in the cross-track dimension to impose a pixel rate of 5 Megapixels per second. This exceeds the spacecraft data system bandwidth by 10^3, requiring an image buffer in the MOC. It further requires an analog signal chain of high video bandwidth.

The absence of pointing control limits opportunities to image a particular target to a few per mission, requiring that the MOC be able to acquire and store multiple images. Images from the telescope are nominally 2k x 2k pixels quantized to 8 bits, so a raw image requires 4M bytes. The image buffer was required to provide three times this capacity, or 12M bytes.

Image compression was required to make effective use of the limited downlink capability of Mars Observer, as well as to extend the capacity of the image buffer. The substantial pixel-level redundancy in real images allows scientific interpretation of images with bad pixels; compressing out that redundancy results in data that is intolerant of errors. Requirements on bit error rates are therefore more relaxed for raw data than compressed data.

The MOC is required to operate autonomously for days from stored commands, and to provide extensive data editing, variable resolution, and variable image compression capabilities by command. A capable microprocessor control and data processing system was imperative.

*Members, AIAA

3. Resources & Constraints

Power, mass and volume contraints were commensurate with intermediate-scale planetary spacecraft. The MOC was initially limited to 9 kg (much of which was required by the telescope) and 7 watts average. The anticipated Total Dose (TD) of ionizing radiation behind various shielding densities was provided by JPL. It was aproximately 10 krad behind 0.4 g/cm^2 of aluminum. JPL also provided integral flux (Heinrich curve) estimates for the heavy ions that cause Single Event Upset (SEU) and Single Event Latchup (SEL) in susceptible components.

4. Component Requirements

The MOC required what were high-performance components in 1986 to meet its performance requirements within the system constraints. An op-amp of order 60 MHz bandwidth and 10 ns rise time for 100 mW, and a 5M sample per second 8-bit A/D for < 250 mW were needed for the analog signal chain. The image buffer needed a 150 ns 1 Megabit RAM for < 20 mW quiescent. Instrument control and data processing required a > 0.5 MIPS 32-bit microprocessor and over 100k bytes of RAM and ROM. Digital Application Specific Integrated Circuits (ASICs) clocked at 20 MHz were required to provide control and data paths to tie the system together.

Most of these were not available as proven radiation-resistant components in 1986. For example, a 4 kbit space-qualified SRAM was available[3] and a 16 kbit component was under development. An impractical 4,000 of these latter components would have been required to implement the minimum image buffer. We were forced outside the confines of the Preferred Parts Lists.

5. System Approach to Rad Resistance

The realities of using ordinary military and commercial components in space required a system approach to radiation resistance. The decision was made early in the program that it was not effective to demand all system level radiation performance requirements be met at the component level. The selected approach was to design a radiation tolerant system rather than simply design a system and populate it with radiation hard components. This does not eliminate the need to find and utilize radiation tolerant components but it does allow the designer more flexibility in designing for a potentially damaging radiation environment. For example, rather than require an absolutely radiation resistant RAM with which to construct the image buffer, Altadena Instruments sought a radiation resistant buffer design that could be built using real components.

The shielding provided by the telescope and electronics enclosure was calculated for different locations within the electronics package and affected parts placement. Spot shielding of individual components was an option to reduce mission TD to < 5 krads where needed.

Heavy ions of solar or galactic origin can produce enough ionization per unit length of travel (Linear Energy Transfer, or LET) to disturb a small-geometry IC with the passage of a single ion. A transient or persistent logic state change can result, referred to as a Single Event Upset (SEU). If a PNPN structure exists between the power rails, as is incidental to many CMOS processes, the deposited charge can turn on this parasitic SCR if certain conditions are met. This effect is termed Single Event Latchup (SEL).

The metric for the significance of SEU in various components was its effect on science data return. Pixel error rates of 10^{-3} are quite acceptable, so the analog processing chain could be allowed occasional transients, and raw pixel data could be stored in SEU-sensitive memory. An error in compressed image data could scramble a quarter million pixels, so some measure was required to protect those data. Likewise, damage to stored instrument commands could cause the loss of multiple images.

An upset in logic circuitry in the control/data path could damage an image acquisition. An upset in the CPU or the stack would cause unpredictable errors, possibly damaging data or causing a program crash. A bit flip in the program execution store is more serious still, requiring a program reload from on-board ROM or from the ground in the worst case. Component SEU and system error detection and recovery requirements had to be balanced in response to these considerations.

Latchup

The effects of latchups were similarly considered, with the additional problem that an uncontrolled component latchup might crash the power supply or destroy the part by overheating. Some components are intrinically immune to SEL by design, e.g. single transistors and CMOS silicon on insulator IC's do not contain 4-layer PNPN structures. Others have demonstrated SEU/SEL immunity. CMOS on sufficiently thin epitaxial layers with sufficient substrate conductivity can be latchup immune. CD4000 series CMOS logic, with its huge feature size, is available SEU/SEL immune.

Since latchup of incidental PNPN structures requires a certain sustaining current, if that current is sufficiently higher than the operating current the component can be prevented from latching up by series resistors in the power leads. Where the only parts that can do the job are latchup susceptible it is necessary to sense and clear latchups by power cycling the component, a technique rarely used in 1986[4].

6. Testing Program

Candidate components that met the other system criteria of performance, power consumption, package suitability and anticipated reliability were tested for radiation resistance. These included op-amps, analog switches, a voltage to frequency converter, 8-bit flash A/D converters, several static and dynamic RAM, UVEPROM, and a microprocessor.

Total Dose

Total dose testing was performed by exposing components to 1.17 and 1.33 MeV photons from ^{60}Co decay, at Sandia National Laboratory's Gamma Irradiation Facility and in a ^{60}Co cell at UCLA. Dose rates ranged from 150 rads per minute up to 2500 rads per minute at the upper doseages, necessarily far exceeding those expected during the three-year mission.

In testing digital components, ten samples of each part were typically used, with eight being irradiated and two kept as controls. During irradiation three devices were powered with inputs biased high, three powered with inputs biased low, and two unpowered. No measurements were made while the devices under test were being irradiated.

Component testing outside the radiation cell was alternated with irradiation inside, with time outside limited to less than 1 hour per cycle. Irradiation proceeded in increasing incremental doses until all components failed or functionality to 100 krad had been demonstrated.

Some of the analog components were tested in-situ in this fashion. Some late tests were conducted by irradiating samples and testing them on the bench a few days later. In this case samples of 12 devices were typically used, with two unirradiated controls and two of each device type removed from exposure at each of five radiation levels.

Fixturing

Test fixturing for the memories was implemented on a plug-in card in an IBM PC type computer. Access times could be varied and the devices read and written under program control. Memory bit integrity tests were implemented in software, and results were recorded to floppy disk. DRAM refresh times were measured and found to correlate with dosage[5]. Device I_{DD} was measured and logged.

Candidate A/D's were tested in another plug-in card. A 4k x 10 bit RAM was read out into a 10-bit video D/A converter whose output was buffered into the devices under test. That system was operated at the 200ns per sample required of the A/D in the MOC, and the converter output captured by another RAM. The stimulus RAM was written and the response RAM read by the PC. A slow ramp was used to test DC linearity, with sawtooth and step stimuli to determine dynamic performance.

The microprocessor was tested in a small standalone system that had an RS-232 serial connection to the test PC. The clock speed was switch-selectable. An EPROM in the test system contained a test program that announced its results via the serial port.

Op-amps were irradiated in amplifier configurations that served as test fixtures for input bias. Amplified bias was measured by digital voltmeter. Irradiated components were tested later on the bench for video characteristics. The voltage to frequency converter was tested in a fixture that operated it at a reference voltage. Output was measured with a frequency counter.

Results

Results of digital component testing are summarized in Table 1. We had the good fortune of discovering a high-capacity (in 1986) DRAM that provided a significant margin in total dose resistance over the expected environment.

Table 1 — Total Dose Testing of Digital Devices

Device	Type	Manuf	Parameter	Function to*
MM884256-15	DRAM	Fujitsu	bit faults	6 krad
D43256C-10L	DRAM	NEC	bit faults	15 krad
TC55257PL-10	DRAM	Toshiba	bit faults	6 krad
M411024PP-15	DRAM	ATT	bit faults	>80 krad
M41256HPM-15B	DRAM	ATT	bit faults	>61 krad
TC511000P-10	DRAM	Toshiba	bit faults	15 krad
SMJ27C256-15	EPROM	TI	bit faults	6 krad

*For purposes of this table, functional is the level up to which no memory errors were seen. Performance may have been acceptable to higher levels, but this is the earliest point at which data was lost.

The EPROM tested showed some bit errors at a dose approximately equal to the expected mission dose, but recovered ("annealed") in the subsequent weeks. We nevertheless made system adaptations described below.

Table 2 shows the results of total dose testing of analog devices.

Table 2 — Total Dose Testing of Analog Devices

Device	Type	Manuf	Parameter	Function to*
SD215	DFET	Topaz	V_{gs}	40 krad
CDG308	Ana. Sw.	Topaz	R_{on}, V_s, V_d	40 krad
HA5141	Op-amp	Harris	V_{os}, I_b	25 krad
HA5147	Op-amp	Harris	V_{os}, I_b	40 krad
HA5152	Op-amp	Harris	V_{os}, I_b	25 krad
EL2020	Op-amp	Elantec	V_{os}, I_b	100 krad
LM131	VCO	NatSemi	f_{out}	40 krad
CA3318	A/D	RCA	linearity	6 krad

*For purposes of this table, functional is the level up to which the measured parameters remained within their maximum allowable data sheet values. Performance in a particular application may have been acceptable to higher levels.

SEU/SEL

Testing for SEU and SEL requires a different approach. The radiation effect is not cumulative with exposure, since the issue is the susceptibility of components to single ionizing events, which is a function of the amount of charge deposited in the sensitive region of the device. It is necessary to test with a range of ionization densities, or LET's. The device under test must be operated during exposure, and must be under vacuum with the die exposed in order to use laboratory sources of suitable ions.

Device susceptibility to SEU or SEL is described in terms of an effective cross-section for the effect as a function of LET. The expected event rate for that component in a particular environment is calculated by integrating the product of expected flux and measured cross-section across the LET spectrum. A given device will have a threshold LET below which there is no effect, and typically for simple devices such as memories, a saturation LET above which the cross-section does not increase. At the higher LET end of the spectrum the flux in space drops off exponentially, so the integration can be performed over a finite range of LET. The testing problem then is to find the LET threshold and measure the cross-section from that LET up to saturation. For devices which do not show SEU or SEL in testing the problem is to establish by exposure to a sufficient fluence of a sufficiently high LET that the probability of upset or latchup in the expected environment can be considered zero for engineering purposes.

Sources

Traditional single event testing employs large accelerators such as the cyclotrons at Berkeley or Brookhaven. They provide good control of LET and flux over a range of LET from 0.002 MeV / (mg/cm^2) to beyond 40 MeV / (mg/cm^2). Unfortunately, time on these machines must be scheduled months in advance and costs tens of thousands of dollars a day[6]. We were constrained by schedule and budget to using other sources.

We used three sources of ions for single event testing. Americium provided the low end of our scale; Am^{241} decays with half-life 458y by emission of 5.5MeV α particles of LET = 0.6 MeV / (mg/cm^2). Californium provided the high end; Cf^{252} decays with half-life 2.65y, 97% by α emission and 3% by spontaneous fission producing fragments of LET clustered about 43 MeV / (mg/cm^2)[7].

The Caltech tandem Van de Graaf accelerator was operated to provide ions in the range of 0.7 to 7 MeV / (mg/cm^2). This left the range from 7 to 42 MeV / (mg/cm^2) unmeasured, requiring that we make the worst-case assumption that the cross-section observed at 42 MeV / (mg/cm^2) was the cross-section for all LET above 7 MeV / (mg/cm^2).

Fixturing

The stand-alone microprocessor system used in total dose testing was adapted for operation in vacuum to provide a fixture for processor and memory single event testing. The lid was pried off the package of the device under test, and the die was exposed to the ion source in a vacuum chamber. Software provided a continuous memory test that reported and cleared upsets at each pass through the memory, allowing rapid testing (> 500 upsets per second) at high ion fluxes. A microprocessor test program was used when the processor was in the beam, which tested not only the normal registers but instruction decode, the ALU data path, and whatever else could send the processor execution awry. A deadman timer provided a reset when the program got lost. Results were reported via the serial port, across a vacuum feedthru and into a test PC for logging.

Since latchup was an issue during exposure as well, SEL testing was conducted simultaneously. A latchup during SEU testing would otherwise seriously confuse the upset measurement process. The

power supply for the device under test was instrumented to provide a voltage proportional to the current being drawn. This voltage was measured by an A/D converter card within the test PC. Test software provided an adjustable current threshold for latchup detection. When the threshold was exceeded the device was allowed to dwell in that condition for a fraction of a second to provide measurement of the current drawn in the latched condition, a quantity needed for the design of the flight latchup detection circuitry. Software then commanded the power supply off and back on to clear the latchup, and logged the event.

Results

The measured cross-sections for upset and latchup were multiplied by the expected environment, under the pessimistic assumption that the cross-section in the LET range between two measurements was equal to the higher measurement (always at the higher LET). The integral of this product as a function of LET gave expected mean rates for SEU and SEL for the mission, shown in Table 3.

Table 3 — Single Event Testing of Devices

Device	Manuf	SEU at Mars	SEL at Mars
SMJ27C256-15	TI	1.7×10^{-4}	1.7×10^{-4}
NS32C016	NatSemi	4.3×10^{-1}	4.8×10^{-1}
UTD212R	UTMC	3.0×10^{-6}	3.0×10^{-6}
M411024PP-15	AT&T	8.4×10^{1}	2.9×10^{-4}
HC6264B	Honeywell	3.0×10^{-6}	3.0×10^{-6}

7. Design

The system design grew from the ends toward the middle, top down from architecture and bottom up from component capabilities and susceptibilities. In accord with the philosophy of not requiring the components to meet all of the system-level radiation requirements, designs were studied which would allow tolerance of radiation effects.

The AT&T 1M bit DRAM was selected for the 12M byte data buffer, providing a design margin for total dose greater than a factor of five. The SEU and SEL susceptibilities presented design problems. The expected SEU-induced bit error rate of 8×10^{-5} per day was acceptable for uncompressed images, but some form of error correction was required for compressed data. A block Error Correction Code (ECC) was selected that corrects two bad bits in 256 for an overhead of 16 bits. Flight software writes and reads blocks of error-sensitive data through routines which apply the ECC and use it to correct errors. We adopted a requirement to provide compression of the 5M pixel per second data stream between the A/D converter and the data buffer, producing error-sensitive data much faster than software could apply the ECC to it. Consequently the pixel data path hardware was required to calculate the ECC.

The expected mean SEL rate of 1 latchup in the 96 DRAMs every 36 days required latchup sense and recovery. The data path architecture produced two buffers of 3M words 16 bits wide. The current draw of the M411024 in the latched state is only of order five times operating current when being accessed, so 16 current sensors were employed per buffer, one for each bit position. Any of these can trigger a power cycle. A mosfet switch in the V_{DD} line that supplies the 48 devices in a buffer, normally saturated on, is cycled off for aproximately 2 ms to clear the latchup. During that time it is necessary to gate low all logic connections to the unpowered DRAM's to keep from holding up the power rail through their input protection diodes. Since the bits are stored as charges on capacitors rather than currents through transistors as in SRAM, data in the DRAM is retained through the SEL-clearing power cycle.

The microprocessor system presented a different problem. Sandia National Laboratories completed development of the SA3300, a "war-protected" version of the National Semiconductor NS32C016 that we had tested, in time for us to incorporate it in the design. According to their testing this part would have a mean upset interval longer than the mission duration, as well as providing a total dose margin of a factor of more than ten. In this era Honeywell developed a 16k x 8 CMOS SRAM with similar hardness, providing a place for the opcode store, processor stack and working variables.

For efficiency in testing, and to avoid having to upload what turned out to be 256k bytes of program and data tables during flight, non-volatile memory to retain the program was required. The flight software development schedule did not allow the use of mask-programmed ROM, so the tested EPROM was used. Despite the observed post-irradiation annealing, we elected to provide spot shielding to lower the expected dose to half the dose at which bit errrors were first observed. We further decided that this device was not suitable to respond to opcode fetches, and adapted the system architecture as follows.

When power is applied to the MOC, the system is cold-reset and the processor starts execution at its standard startup address. Its address and data busses connect only to an ASIC, the Control Gate Array (CGA). The CGA services read requests in the startup address range by reading from three separate EPROMs and triplicate-voting the result to arrive at the value provided to the processor. The bootstrap

routine executes in this way. The body of the flight software is stored in the EPROM with the same ECC as used in the DRAM buffer. It is read out and errors are corrected by the bootstrap program, and stored in hard SRAM, to which execution is transferred when it is in place.

Power considerations left no choice but to use the CA3318 CMOS SOS flash A/D, despite its susceptibility to total dose. It was placed near the center of the board to receive maximum shielding from the 3.5kg primary mirror directly above it, and surrounded the package with as much spot shielding as we could fit. The expected total dose to this component was thereby limited to 3kRad, a factor of one-half of the dose where degradation was observed.

Latchup in analog components was addressed by multiple means. The analog switches had a low enough operating current that series resistors in the power leads could be used to keep the device below its latchup sustain current. To provide overall protection of the analog power rails, overcurrent power cycling was integrated with low-headroom dual tracking linear "skimmer" FET post-regulators, incidently providing 20 dB rejection of the power supply switching frequency, and logic-level on-off control of the circuit block. The turn-on dV/dT was limited to 250 V/s to keep well below the rate where charging the bypass capacitors would trigger an overcurrent cycle.

8. Summary

Modern space systems in constrained resource environments can benefit from an integrated system-level approach to radiation resistance. This requires determining the radiation susceptibility of candidate components. Radiation susceptibility can be determined to a level sufficient to interact with the system design process in a rapid and comparatively inexpensive fashion. Altadena Instruments' development of the Mars Observer Camera has demonstrated this approach in a NASA planetary space mission context.

9. Acknowledgements

The authors wish to thank Alan Rice for his skillful operation of Caltech's Tandem Accelerator. Alan Danziger provided hardware and software design of test fixtures. Most especially we thank Dr. Malin for having the courage to go beyond accepted planetary instrument practice in order to achieve significant science, and his and Ed Danielson's faith in us to do it.

The work described was supported by Caltech contract 65Q-784942.

10. References

[1] M. C. Malin, G. E. Danielson, A. P. Ingersoll, H. Masursky, J. Veverka, M. A. Ravine and T. A. Soulanille. *Mars Observer Camera.* J. Geophys. Res., Vol. 97, No. E5, 7699-7718 (1991).

[2] M. C. Malin, G. E. Danielson, M. A. Ravine and T. A. Soulanille. *Design and Development of the Mars Observer Camera.* Int. J. Imag. Syst. Tech., Vol. 3, 76-91 (1991).

[3] T. G. Steffey, J. V. Ryciak, W. R. Scott, and R. E. Covey. *JPL Preferred Parts List: Reliable Electronic Components.* JPL Spec. ZPP-2061-PPL, p. 41 of Microcircuits section, 20 July 1982. [Edition in force during MOC electronics design]

[4] H. B. O'Donnell, J. M. Loman, P. Ritter, and J. R. Stahlman. *Spacecraft Hardness Assurance Programs.* IEEE Trans. on Nuclear Science, Vol. NS-33, No. 6, pp. 1359-1364, Dec. 1986.

[5] D. K. Myers, A. S. Danziger, and T. A. Soulanille. *Radiation Tolerant Memory Selection for the Mars Observer Camera.* IEEE Trans. on Nuclear Science, Vol. NS-34, No. 6, pp. 1467-1469, Dec. 1987.

[6] J. H. Stephen, T. K. Sanderson, D. Mapper and J. Farren. *A Comparison of Heavy Ion Sources Used in Cosmic Ray Simulation Studies of VLSI Components.* IEEE Trans. on Nuclear Science, Vol. NS-31, No. 6, pp. 1069-1072, Dec. 1984.

[7] J. T. Blandford, Jr., and J. C. Pickel. *Use of CF-252 to Determine Parameters for SEU Rate Calculation.* IEEE Trans. on Nuclear Science, Vol. NS-32, No. 6, pp. 4282-4286, Dec. 1985.