IN-ORBIT RADIATION EFFECTS MONITORING ON THE UoSAT SATELLITES[1]

Craig I. Underwood
Research Fellow
UoSAT Spacecraft Engineering Research Unit
University of Surrey
Guildford, U.K.

Since the summer of 1988, radiation effects, in particular single event upset (SEU) phenomena, have been monitored in the three mass semiconductor memory systems on-board the University of Surrey's UoSAT-2 satellite, which is in a 700 km, near-polar low-Earth orbit. Almost 5000 events have now been logged by the spacecraft, and these have been assembled into a database for analysis by ground-based software. This software has allowed the SEU sensitivity of different device types to be analysed, and the relative performance of the Mostek 4116, Texas 4416 NMOS DRAMs, the Toshiba TC5516, Harris 6564 and 6516, and the Hitachi 6264 and 6116 CMOS SRAMS, has been evaluated. The logs of in-orbit SEUs on UoSAT-2 have provided several interesting statistics, allowing direct comparison of static and dynamic RAMs ranging in capacity from 4 kilobits to 64 kilobits per chip. An unexpected result has been that none of the 288K bytes of 8-bit wide static RAM on UoSAT-2 have shown multiple-bit (per byte) upsets over the monitoring period. Also, the orbital analysis of UoSAT-2 SEUs shows an overwhelming concentration of events in the South Atlantic Anomaly for all device types. Further studies are now underway with the University of Surrey's UoSAT-3 satellite. This spacecraft carries over 4M bytes of semiconductor memory as part of its store-and-forward communictions payload, together with the Cosmic Particle / Total Dose Experiments (CPE / TDE), providing direct measurments of the space radiation environment.

INTRODUCTION

The UoSAT-2 spacecraft is the second technology-demonstration / educational 'lightsat' (60 kg) designed and constructed at the Spacecraft Engineering Research Unit at the University of Surrey, UK[1]. It was launched into a 700 km, near-polar, Sun-synchronous orbit in March 1984, on-board a DELTA launch-vehicle, as a secondary payload to the NASA Landsat D' mission. Of the many systems on-board the spacecraft, three contain substantial (in 1984 terms) quantities of semiconductor memory.

[1]Prepared for the 4th Annual AIAA/USU Conference on Small Satellites, August 1990, Logan, Utah.

These are the Primary On-Board Computer (OBC) system[2], based around a CDP-1802 8-bit microprocessor; the Data Store-and-Readout (DSR) bulk memory system[3], and the Digital Communications Experiment (DCE)[4], based around an NSC-800 8-bit microprocessor. The memory systems associated with these are all, to some extent, susceptible to single-event upset (SEU), and each is protected and monitored by a mixture of hardware and software error-detection and correction (EDAC) coding schemes.

In summary, the primary OBC monitors 576 kilobits of NMOS dynamic RAM (DRAM), organised as 48K-by-12-bit bytes (i.e. 8 data bits and 4 EDAC bits per byte), via a hardware-implemented EDAC coding scheme. The DSR comprises 1536 kilobits of CMOS static RAM (SRAM), organised as two banks of 96K-by-8-bit bytes, but without EDAC. The DCE monitors 752 kilobits of CMOS SRAM in total, shared between two sub-systems: the RAMUNIT, organised as 96K-by-8-bit bytes, of which 94K are monitored by a software-implemented EDAC scheme, and the PROGRAM RAM, organised as 16K-by-12-bit bytes, of which 12K are monitored by a hardware-implemented EDAC scheme similar to that in the OBC.

This gives a total monitoring capability of 589,824 bits of NMOS DRAM, together with 1,703,936 bits of CMOS SRAM.

Single-Event Upsets (SEUs)

SEUs are temporary bit-state reversals induced in semiconductor devices through the action of ionising radiation. Such events may be caused directly by an in-comming particle if it deposits sufficient energy within a critical volume of the semiconductor lattice, or may be caused as the result of secondary ionisation due to the recoil of particles resulting from induced nuclear reactions.

It is now recognised that SEUs, caused by the heavy-ion component of cosmic-rays, and by the trapped particle populations (particularly protons) in the geo-magnetic field, are a major concern in spacecraft microelectronics[5,6,7,8,9,10]. Such effects are becoming increasingly important as device geometries are reduced to the micron and sub-micron scale. Total-dose effects are also extremely important, as the extended operational lifetimes required of modern spacecraft can give rise to very large (megarad) accumulated doses, albeit delivered at relatively low dose-rates compared to other ionising environments, such as the interior of nuclear reactors, and on the nuclear battle-field.

Semiconductor devices on-board Earth-orbiting spacecraft have SEU rates which depend upon device technology, geometry and manufacture, solar activity, local shielding provided by the spacecraft structure, and the precise orbital characteristics of the vehicle. Modelling the interactions between the space-radiation environment, the spacecraft structure, and a particular device, is a complex process, with little experimental data to work on as the relatively long exposure, low dose-rate environment - typical of space - is particularly hard to simulate on Earth in a cost-effective way.

Thus, it is difficult to make any realistic predictions as to the behaviour of a particular device in space, and much more experimental data is required on the *actual* performance of modern semiconductor devices in *real* space environments.

With this in mind, a varied selection of memory device types was chosen for the UoSAT-2 spacecraft, so that experience could be gained with a variety of different device sizes, technologies and manufacturers.

SPACECRAFT SYSTEMS AND MONITORING STRATEGY

Primary On-Board Computer (OBC)

UoSAT-2 uses a CDP-1802 microprocessor as its primary on-board computer, and this has access to all the major sub-systems in the spacecraft. To facilitate UoSAT-2 spacecraft operations and provide a degree of autonomy to on-board task scheduling, the OBC executes a multi-tasking operating system known as the DIARY. The DIARY software supports multi-tasking, uplink command decoding, command macro expansion, event scheduling (up to one year in advance), telemetry logging and reporting, attitude determination and control and synthesised speech generation.

In addition to this, under a research contract with the European Space Agency (ESA-ESTEC)[11,12], DIARY routines for SEU detection, logging and reporting were developed at Surrey and implemented on the spacecraft during 1988.

Table 1
OBC MEMORY DEVICES

Manufacturer	*Part*	*Chip Size*	*Quantity (ICs)*
Mostek	*MKB4116J-83*	*16K x 1-bit*	*12*
Texas	*TMS4416-15NL*	*16K x 4-bit*	*3*
Texas	*TMS4416-20L*	*16K x 4-bit*	*3*

The OBC memory is divided into two main areas, a 16K-by-12-bit byte area for program storage, and a 32K-by-12-bit byte area to hold data collected from on-board experiments. These memory areas are built from NMOS dynamic RAMs; the 16K byte area is built from twelve 16K-by-1-bit DRAMs (4116 type), and the 32K byte area uses six 16K-by-4-bit DRAMs (4416 type). Both areas are protected by hardware error detection and correction (EDAC) circuitry.

The EDAC system is a Hamming code generator which calculates four check bits for each 8-bit data byte. When a byte is written to RAM, four Hamming check bits are generated and stored, resulting in 12-bits being stored for every byte. When a byte is read from RAM, a Hamming decoder checks the integrity of the data. If the data contains a single bit error, the Hamming bits are used to generate the correct data, and the corrected data are passed to the CPU. Each time that the decoder detects and corrects an error, an SEU counter is incremented. Errors which involve more than one-bit upset per byte are not indicated. However, this is not a problem as the key program memory has the 12-bits of each byte spread over 12 devices, ensuring a large degree of physical and electrical separation, making it extremely unlikely that a single particle could cause more than one bit-upset in a byte. That said, the internal geometry of the 4-bit wide devices, is such that they may well be susceptible to multiple-bit per-byte upsets. However, the evidence from UoSAT-2 suggests that such events must be quite rare.

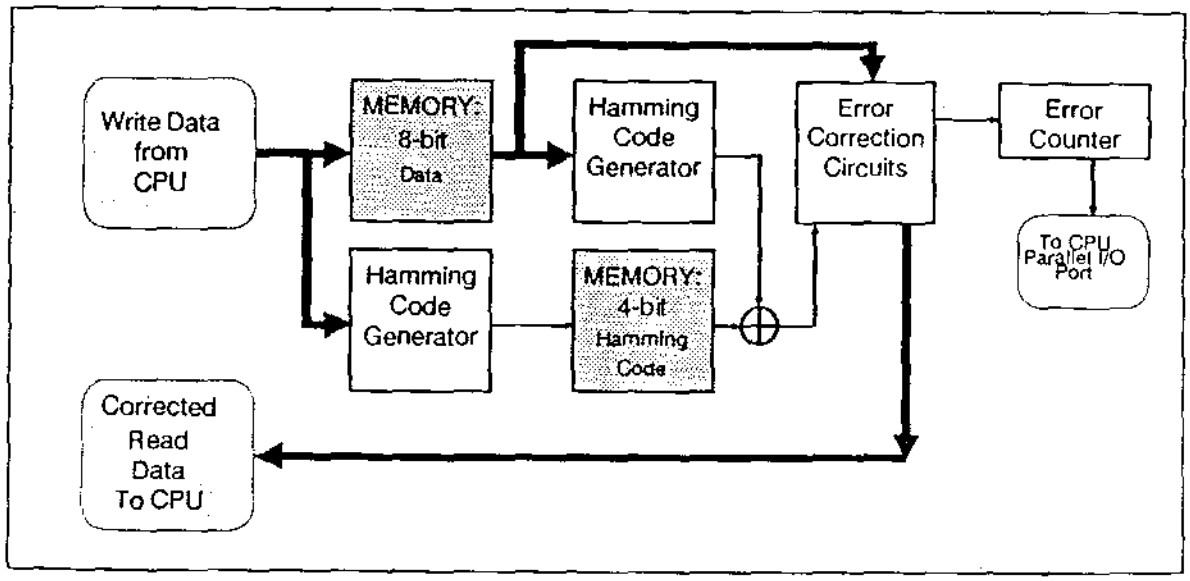

Fig. 1 Hamming Error Detection and Correction for the OBC Memory

The EDAC system does not automatically correct data stored in RAM. When an SEU is detected, the correct data byte is sent to the CPU, but it is not stored in the RAM, i.e. the RAM itself still contains the SEU. Correct data and code bits are only stored when the CPU writes a byte to the RAM. If a byte experiences an SEU, and then experiences another before the first has been corrected, the byte will contain two bit errors, and the Hamming code will not be able to correct it. Therefore, to ensure that errors do not accumulate in the memory, a software memory 'wash' is implemented. The memory wash reads each memory location in turn and then immediately writes the value back into memory. Thus, SEUs are actually corrected in the RAM before further SEUs can occur.

The wash forms part of the DIARY interrupt code. One byte is 'washed' on every call to this code, provided that there is no previous SEU still to be logged by the 'EDAC Error Logging Task' in the DIARY's main loop. The wash software monitors the EDAC counter before and after each byte is read, as the counter will increment if a SEU is detected. If the counter increments, an 'error- flag' is raised by the wash routine, which is serviced by the error log task. This task records the address of the error, the total number of errors since program initialisation, and the current time and date, as defined by the OBC's hardware clock. These data are stored in a circular buffer which can accommodate 32 such events.

The time taken to wash the entire memory is approximately 8.25 minutes. This is sufficiently fast to give a very low probability of two or more particles affecting a particular byte before any previous error has been corrected.

Whenever UoSAT-2 is within range of the command groundstation at the University of Surrey, downlink data are automatically collected and stored on the hard disc of an IBM-compatible microcomputer. The raw data include telemetry, long-term data surveys, and the OBC EDAC error log data. The raw error log data are processed by ground-station software, and are eventually combined with data from an orbital model to form records in the OSIRIS[2] database. These data are then amenable to further statistical, temporal and geographical analysis. Data on the SEU behaviour of the OBC memories have been collected continuously since September 1988.

Data Store-and-Readout (DSR) Experiment

The Data Store-and-Readout (DSR) Experiment consists of two 96K-by-8-bit byte banks of CMOS SRAM which can be serially loaded and read under hardware logic control. Each DSR bank contains 48 2K-by-8-bit CMOS SRAMs (TC5516 type). One of these banks has been dedicated to SEU monitoring, whilst the second bank has been left free for other on-board experiments, with occasional monitoring for SEUs.

Table 2
DSR MEMORY DEVICES

Manufacturer	*Part*	*Chip Size*	*Quantity (ICs)*
Toshiba	*TC5516AP-2*	*2K x 8-bit*	*96*

The data sources for the DSR experiment are the OBC, the CCD Earth-Imaging Camera Experiment and the Particle-Wave/Electron Spectrometer Experiment. Data from the DSR may be output to either the OBC or directly to the spacecraft's downlink. Downlink transmissions from the DSR memory (usually at 4.8 kbps) can be initiated by ground-command or by OBC DIARY scheduling.

Unlike OBC downlink data, DSR data are sent in addressed, error-protected packets. The 96K bytes of data are divided into 768 packets, each containing 128 bytes of data. The packets are prefixed with an address indicating where in memory the packet came from, and a 'cyclic redundancy check' (CRC) is transmitted at the end of each packet. The CRC is checked by the receiving software in the groundstation, and any packets which contain reception errors are rejected. Because the DSR is not a computer-controlled system, no acknowledgements are sent by the groundstation to the DSR during data transfer; the DSR simply sends 768 data packets and then starts again with the first packet. The groundstation software receives packets, files those which are error-free, and waits until an entire DSR image has been built up. If the entire image is not received, there will be 128-byte gaps in the data. These gaps must be detected so that they do not interfere with SEU monitoring.

[2]Orbiting Satellite Ionising Radiation Interactions with Semiconductors

As the DSR contains no microprocessor or EDAC system, it cannot be programmed to monitor SEUs, and the serial links with the OBC are too slow to make OBC monitoring of SEUs in the DSR practical. Therefore, the complete DSR memory image is downlinked each week and checked for SEUs in the command groundstation.

In order to facilitate this a program was written for the OBC to generate a fixed pattern of data, and write it across the serial network of the spacecraft for storage in the DSR (Bank 'A'). This pattern constitutes the initial 'reference image', against which any bit changes can be detected. It was loaded into the DSR Bank 'A' memory on the 21st July 1988, and SEU activity has been monitored ever since.

Groundstation software compares each week's downloaded memory image with the reference image, and any differences between the two indicate SEUs. The possibility that there may be gaps in a received DSR image complicates the SEU detection procedure. However, this is dealt with by keeping a reference file, containing the most recently-received copy of each packet. Each packet in a newly-received image is compared to its corresponding reference, and any differences are logged as SEUs. SEUs must have occurred between the reference date and the current date, and in most cases, this will be one week. In practice, because very few packets - if any - are missed during the weekly download, the maximum time-span between consecutive checks of a memory location is two weeks.

Digital Communications Experiment (DCE)

The UoSAT-2 Digital Communications Experiment (DCE) is a proof-of-concept store-and-forward digital message transponder, which provided one of the first civilian demonstrations of low-Earth orbit store-and-forward communications between inexpensive satellite terminals attached to standard personal computers [13,14,15].

Table 3
DCE MEMORY DEVICES

Manufacturer	*Part*	*Chip Size*	*Quantity (ICs)*
Harris	*H6564*	*4K x 1-bit*	*3 hybrids equivalent to 48 HM-6504s*
Harris	*MI6516-9*	*2K x 8-bit*	*1*
Hitachi	*HM6264LP-12*	*8K x 8-bit*	*8*
Hitachi	*HM6116L-3*	*2K x 8-bit*	*8*
Hitachi	*HM6116-3*	*2K x 8-bit*	*8*

The NSC-800 microprocessor uses both hardware and software EDAC to monitor SEUs. SEU logs are communicated to the command station using the store-and-forward automatic-repeat-request (ARQ) communications protocol, and subsequent data analysis is performed by groundstation computers [16].

SEU Monitoring in Hardware-EDAC Protected 'PROGRAM RAM'. Programs and critical data are stored in the Harris 6564 hybrid memories. Each 8-bit data byte in this memory is protected by a 4-bit Hamming error detection and correction (EDAC) code in the manner described for the OBC. A memory wash routine similar to that used in the OBC runs on the DCE and protects the hardware-EDAC memory against

accumulating SEUs. As the underlying memory devices are 1-bit wide, the chance of getting a multiple-bit per-byte error due to a single particle is extremely remote.

As with the OBC, the SEUs are logged in terms of address and time of occurence. The DCE does not contain a real-time clock, and so time stamps for the DCE SEU log are read by the NSC-800 CPU from the UoSAT-2 serial telemetry stream. This telemetry clock is derived from separate hardware to that for the OBC clock used for time-stamping errors in the OBC memory, and so the time-tags have to be treated separately when calibrating the logged-times to true GMT.

A permanent 'hard'-failure occurred in this area of memory between orbits 12844 and 12857 in 1986 [11], and since then only 12K bytes (i.e. 144 kilobits) of the 16K bytes (192 kilobits) have been monitored and in active use. Since it takes approximately 5.25 minutes for the DCE to completely wash the remaining 12K bytes of EDAC-protected memory, the DCE may log an SEU up to 5.25 minutes after its actual occurrence.

SEUs are logged in an on-board circular buffer which is capable of recording 32 events, and since the event rate is normally very low (approximately one event per ten days), there is little danger of this buffer being overrun between downloads. The log is kept in an area of hardware-EDAC memory, and the command station downloads it using the DCE message system store-and-forward communications protocol, as part of the normal message traffic.

SEU Monitoring in the Software Protected 'RAMUNIT'. As well as the 16K bytes of hardware EDAC-protected program memory, the DCE has 96K bytes (i.e. 768 kilobits) of memory used for storing messages. This memory is referred to as the 'RAMUNIT', and is comprised of 8-bit-wide CMOS SRAMs. Eight of the devices (6264s) store 8K bytes each and sixteen devices (6116s) store 2K bytes each.

The RAMUNIT has no hardware EDAC, therefore a software EDAC system has been developed and installed.

The NSC-800 uses the RAMUNIT as a RAM disk, writing-to and reading-from the RAMUNIT in 256-byte blocks - analogous to the sectors of a computer's disk drive. Therefore, a block code was the logical choice of EDAC code in this environment. Other criteria used in the selection of a code were:-

1) computationally efficient encoding and decoding,
2) low coding overhead,
3) ability to detect burst errors (because of the possibility that a single charged particle might cause a number of simultaneous bit-upsets in a single byte or block of memory).

To meet these various requirements, Dr. M.S. Hodgart and Jeff Ward of the University of Surrey, devised an efficient implementation of a multiple-polynomial generalised Burton code which can identify and locate a single- or multiple bit upset confined to a single byte anywhere in a 253-byte data block. The code detects but will not correct a burst error of not more than 9 bits spread over two bytes, and the code is guaranteed to detect (but not correct) any error which upsets two bytes in a block.

Any event worse than this is virtually guaranteed to be detected, but may be incorrectly identified as a less severe error. By far the most common events are single bit events, *all* of which are detected and corrected by this code.

In order to implement this code, each 256-byte RAMUNIT memory block is broken into two 128-byte sub-blocks, and each of these is encoded using the Hodgart-Burton code. The overhead created is 3 bytes for every 128, or approximately 2%. Because of this very low coding overhead, the check bytes (which protect themselves from SEUs) are actually stored in the DCE general memory (GMEM) area made up of the Harris 6516 ICs.

Each memory sub-block (128 bytes) is periodically decoded to check for SEUs. In each cycle of the wash, one 12-bit-byte from the PROGRAM RAM, and one 128-byte block from the RAMUNIT are washed. A complete wash of the RAMUNIT (768 blocks) takes approximately 19 seconds, so the time-localisation of any SEU in the RAMUNIT is very good.

Severe Error Characterisation. Because of the possibility that a really severe error, with a great many SEUs per block, could be misinterpreted by the software EDAC scheme as a *less* severe error, a further check is implemented, whereby blocks of memory which are not in active use for message storage are filled with a known bit-pattern. As well as checking the EDAC code, the wash routine also checks the blocks to make sure the bit-pattern corresponds to the known fixed pattern. If it does not, a 'Severe Error' message is generated, detailing the bits which have changed.

Although the vast majority of errors picked up by the software EDAC scheme are single-bit errors, occasionally an 'extended' error is reported - i.e. more than one bit has been upset within a particular block. If an 'extended' error occurs within one of the un-used blocks, the resulting severe-error message can be used to extract further information. Throughout the monitoring period to the end of 1989, only three 'extended' errors occurred. Of these, only one could be analysed via the 'severe' error log, and this showed that a single bit, in each of two adjacent bytes, had been affected.

A hard failure was detected in one of RAMUNIT's 2K-by-8-bit HM6116 memory devices as the monitoring software was being developed (prior to July 1988) and therefore, this device is not monitored. Thus, of the 96K bytes of memory available in the RAMUNIT, only 94K bytes are being monitored at this time. The complete DCE SEU monitroing system has been active since July 1988.

IN-ORBIT MONITORING RESULTS

Single-Event Upset Rates

OBC : The observations of SEUs in the OBC NMOS DRAM memory are summarised in the following tables :-

Table 4 (a)
UoSAT-2 OBC MEMORY

Device	*Mostek MKB4116J-83 16K-by-1-bit NMOS DRAM*
Number of Devices	*12*
Total Memory Size	*196,608 bits*
Monitored Memory Size	*196,608 bits*
Monitoring Period	*474 days*
Total Number of SEUs	*491*
SEU Rate (per bit)	5.269×10^{-6} *SEU/bit/day*
SEU Rate (per device)	8.632×10^{-2} *SEU/device/day*

Table 4 (b)
UoSAT-2 OBC MEMORY

Device	*Texas TMS4416-15NL/-20L 16K-by-4-bit NMOS DRAM*
Number of Devices	*6 (3 of each)*
Total Memory Size	*393,216 bits*
Monitored Memory Size	*393,216 bits*
Monitoring Period	*474 days*
Total Number of SEUs	*3937*
SEU Rate (per bit)	2.112×10^{-5} *SEU/bit/day*
SEU Rate (per device)	*1.384 SEU/device/day*

Thus, the Texas TMS4416 devices are found to be 4.008 times more sensitive (per bit), and 16.037 times more sensitive (per device) than the Mostek MKB4116 devices. It would therefore appear that the per-bit error-rate in these devices scales exactly with the device size i.e. 4 : 1. The error-rate for the OBC memory as a whole is 9.342 SEUs per day.

DSR : Monitoring SEUs in the DSR started on 21st July 1988. DSR Bank 'A' was downloaded virtually every week after this, and 70 dumps were received prior to the end of December 1989. To make sure that Bank 'A' and Bank 'B' were not drastically different in their SEU characteristics, Bank 'B' was loaded with the fixed byte pattern (a CCD image) on 14th August 1988 and was surveyed for SEUs in September, October, November and February (1989).

The over-all error-rate for the DSR Bank 'A' memory is 0.340 SEUs per day, whilst the error-rate for DSR Bank 'B' memory is 0.516 SEUs per day. Thus, it would appear that Bank 'B' is approximately 50% more susceptible to SEUs. The cause of this is not yet known. However, it does not seem to be related to the differing numbers of '1' and '0' bits in each bank, as an analysis of the SEU bit-transitions indicates that the probability of bit-upset is the same for a '1' as it is for a '0'.

The observations of SEUs in the DSR CMOS SRAM memory are summarised in the following tables :-

Table 5 (a)
UoSAT-2 DSR MEMORY

Device	*Toshiba TC5516AP-2 2K-by-8-bit CMOS SRAM*
Number of Devices	*48 (Bank A)*
Total Memory Size	*786,432 bits*
Monitored Memory Size	*780,186 bits (averaged over 70 surveys)*
Monitoring Period	*514 days*
Total Number of SEUs	*175*
SEU Rate (per bit)	*4.364×10^{-7} SEU/bit/day*
SEU Rate (per device)	*7.093×10^{-3} SEU/device/day*

Table 5 (b)
UoSAT-2 DSR MEMORY

Device	*Toshiba TC5516AP-2 2K-by-8-bit CMOS SRAM*
Number of Devices	*48 (Bank B)*
Total Memory Size	*786,432 bits*
Monitored Memory Size	*771,328 bits (averaged over 4 surveys)*
Monitoring Period	*184 days*
Total Number of SEUs	*95*
SEU Rate (per bit)	*6.694×10^{-7} SEU/bit/day*
SEU Rate (per device)	*1.076×10^{-2} SEU/device/day*

Apart from bursts of activity which occurred on week-ending: 10/08/88 (10 events), 04/10/89 (11 events) and 25/10/89 (15 events), the 70 surveys of DSR Bank 'A', show a fairly consistent error-rate, for the entire bank, of 2.3 SEUs per week.

The DSR SEU logs include an error pattern output, showing which bit or bits in a byte were upset by a given SEU. One of the important results of the DSR (and DCE) monitoring is that *no* multiple-bit errors in a single byte have been observed.

DCE : There are two main memory systems being monitored in the DCE: 12K (12-bit) bytes of 'PROGRAM' CMOS SRAM, with hardware EDAC protection, and 94K (8-bit) bytes of 'RAMUNIT' CMOS SRAM, with software EDAC protection. As part of the software EDAC protection of the RAMUNIT, 2304-by-8-bit check-bytes are stored in the 'GMEM' CMOS SRAM, giving some monitoring capability in this RAM.

Table 6
UoSAT-2 DCE 'PROGRAM RAM' MEMORY

Device	*Harris 6564 Hybrid CMOS SRAM (16 x HM6504 4K-by-1-bit in each hybrid)*
Number of Devices	*3 Hybrids*
Total Memory Size	*196,608 bits (16K-by-12-bit-bytes)*
Monitored Memory Size	*147,456 bits (12K-by-12-bit bytes)*
Monitoring Period	*823 days (approximately)*
Total Number of SEUs	*54*
SEU Rate (per bit)	*4.450×10^{-7} SEU/bit/day*
SEU Rate (per hybrid)	*2.187×10^{-2} SEU/device/day (HM6564)*
SEU Rate (per device)	*1.823×10^{-3} SEU/device/day (HM6504) (36 of 48 HM6504s are monitored)*

Table 7 (a)
UoSAT-2 DCE 'RAMUNIT' MEMORY

Device	*Hitachi HM6264LP-12 8K-by-8-bit CMOS SRAM*
Number of Devices	*8 (4 in Bank 0 and 4 in Bank 1)*
Total Memory Size	*524,288 bits*
Monitored Memory Size	*524,288 bits*
Monitoring Period	*549 days*
Total Number of SEUs	*159*
SEU Rate (per bit)	*5.524×10^{-7} SEU/bit/day*
SEU Rate (per device)	*3.620×10^{-2} SEU/device/day*

Table 7 (b)
UoSAT-2 DCE 'RAMUNIT' MEMORY

Device	*Hitachi HM6116-3/L-3 2K-by-8-bit CMOS SRAM*
Number of Devices	*16 (8 in Bank 2 and 8 in Bank 3)*
Total Memory Size	*262,144 bits*
Monitored Memory Size	*245,760 bits*
Monitoring Period	*549 days*
Total Number of SEUs	*93*
SEU Rate (per bit)	*6.893×10^{-7} SEU/bit/day*
SEU Rate (per device)	*1.129×10^{-2} SEU/device/day*

Although these error-rates are comparable to those for the other CMOS memories on the spacecraft, it is interesting to note that the less dense 6116 devices appear to have a slightly higher error-rate (per bit) than the more dense 6264 devices.

The DCE general memory (GMEM) RAM consists of seven Harris MI6516-9 2K-by-8-bit CMOS SRAMS. These have no EDAC protection, and therefore cannot be monitored for SEU activity directly. However, check-bytes generated from blocks of RAMUNIT memory are stored in the GMEM RAM as part of the software EDAC system for the DCE RAMUNIT. Each 128- byte block in the RAMUNIT, has associated with it, three check bytes in the GMEM RAM. These bytes are 'self- protecting' and

so if a block has an error, it is possible to tell if the error occurred in the data bytes (stored in the RAMUNIT) or in the check bytes (stored in the GMEM RAM). SEUs in the check bytes occured twice during 1988, giving some indictation of the underlying (albeit low) error-rate for the Harris devices.

Table 8
UoSAT-2 DCE 'GMEM' Memory

Device	*Harris MI6516-2/-9 2K-by-8-bit CMOS SRAM*
Number of Devices	*7 (2 × MI6516-2, 5 × MI6516-9s)*
Total Memory Size	*114,688 bits (112K-by-8-bit bytes)*
Monitored Memory Size	*18,432 bits (768 blocks × 3 bytes)*
Monitoring Period	*549 days*
Total Number of SEUs	*2*
SEU Rate (per bit)	*1.976×10^{-7} SEU/bit/day*
SEU Rate (per device)	*3.238×10^{-3} SEU/device/day*

This is consistent with the other CMOS memories on the spacecraft.

All Systems : In summary, the error rates for the different memory devices within UoSAT-2 can be quantified as follows :-

Table 9
COMPARISON OF DEVICES

Device Type	*Chip Size*	*Number of SEUs*			*SEU Rate (10^{-7} SEU/bit/day)*		
		Meas.	*Max.*	*Min.*	*Meas.*	*Max.*	*Min.*
Harris MI6516	*(2K x 8)*	*2*	*6*	*1*	*1.976*	*5.929*	*0.988*
*Harris H6564**	*(4K x 1)*	*54*	*68*	*44*	*4.450*	*5.603*	*3.626*
Toshiba TC5516AP	*(2K x 8)*	*270*	*299*	*245*	*4.973*	*5.507*	*4.512*
Hitachi HM6264LP	*(8K x 8)*	*159*	*182*	*140*	*5.524*	*6.323*	*4.864*
Hitachi HM6116/L	*(2K x 8)*	*93*	*111*	*79*	*6.893*	*8.227*	*5.855*
Mostek MKB4116J	*(16K x 1)*	*491*	*530*	*457*	*52.687*	*56.872*	*49.038*
Texas TMS4416	*(16K x 4)*	*3937*	- -	- -	*211.230*	- - -	- - -

* - Harris constructed hybrid equivalent to 16 HM6504 4K x 1 bit devices.
Max. and Min. are the 5% Poisson Limits.

The striking characteristic of this table is the similarity between the SEU rates for various CMOS static memories. The CMOS SRAMs range in size from 4 kilobits (in the HM6564 hybrids) to 64 kilobits (in the HM6264 RAMs), yet these devices exhibit virtually the same error rate (per bit, per day) within the defined certainty limits. This rate is of the order of 5×10^{-7} SEU/bit/day. It is also interesting to note that the 6116-type RAMs, not the more dense 6264-type, exhibit the highest SEU rate for the SRAMs.

The DRAMs in the 1802 OBC have SEU rates from one to two orders of magnitude higher than for the SRAMs. In the dynamic RAMs, it is clearly the more dense devices (4416-type) which exhibit higher SEU rates. DRAMs seem to be undesirable for SEU-sensitive applications.

SEU Analysis by Orbital Position

Both the OBC and the DCE systems log the time at which SEUs occur, according to the spacecraft's internal clocks. Because of the finite nature of the wash period for each of these systems, the logged time represents the end of a time 'window', within which the SEU must have occured. For example, the wash period for the OBC is 8.25 minutes, so it is just possible that the time that a SEU is detected is 8.25 minutes later than when it actually occured. The equivalent 'window' for the DCE PROGRAM RAM is approximately 5.25 minutes, with only 19 seconds for the DCE RAMUNIT.

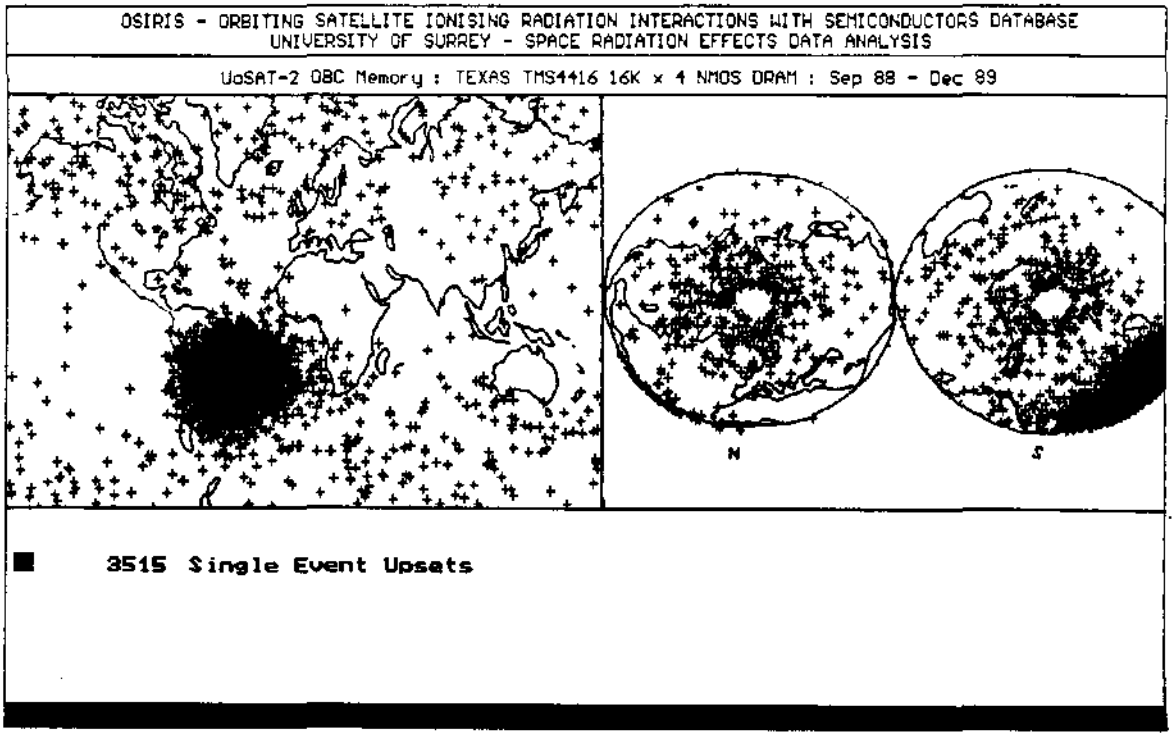

Fig. 2 UoSAT-2 OBC Memory SEU Activity Plotted Against Orbital Position

Once the spacecraft time has been corrected to GMT, it is possible, using a computer model of the orbit., to locate the position of the SEUs with respect to the Earth. These positions can then be plotted on a map, with a worst-case precision of +/- 15 degrees of latitude (corresponding to +/- half the OBC wash window period of 8.25 minutes).

Fig. 2 shows all the collected OBC SEU data plotted on a Mercator's projection map, together with two Polar projection maps. It is clear that the majority of SEUs occur in concentrated region off the coast of South America - a region known as the South Atlantic Anomaly (SAA), where energetic protons (few hundred MeV) are

encountered in the UoSAT-2 orbit. There is also some enhanced activity at high latitudes (greater than 65°), and Fig. 3 shows that this was particularly the case in September and October 1989. At these high latitudes, the opening of the Earth's magnetic field-lines to the interplanetary medium means that the spacecraft is more exposed to cosmic rays. However, the most notable enhancements in these 'auroral' regions, are due to the major solar proton events which occured during 1989.

The graph of raw SEU-rate shows that these solar-flare events had a substantial effect on the error-rate, with the graph going off the scale during the October 19th event.

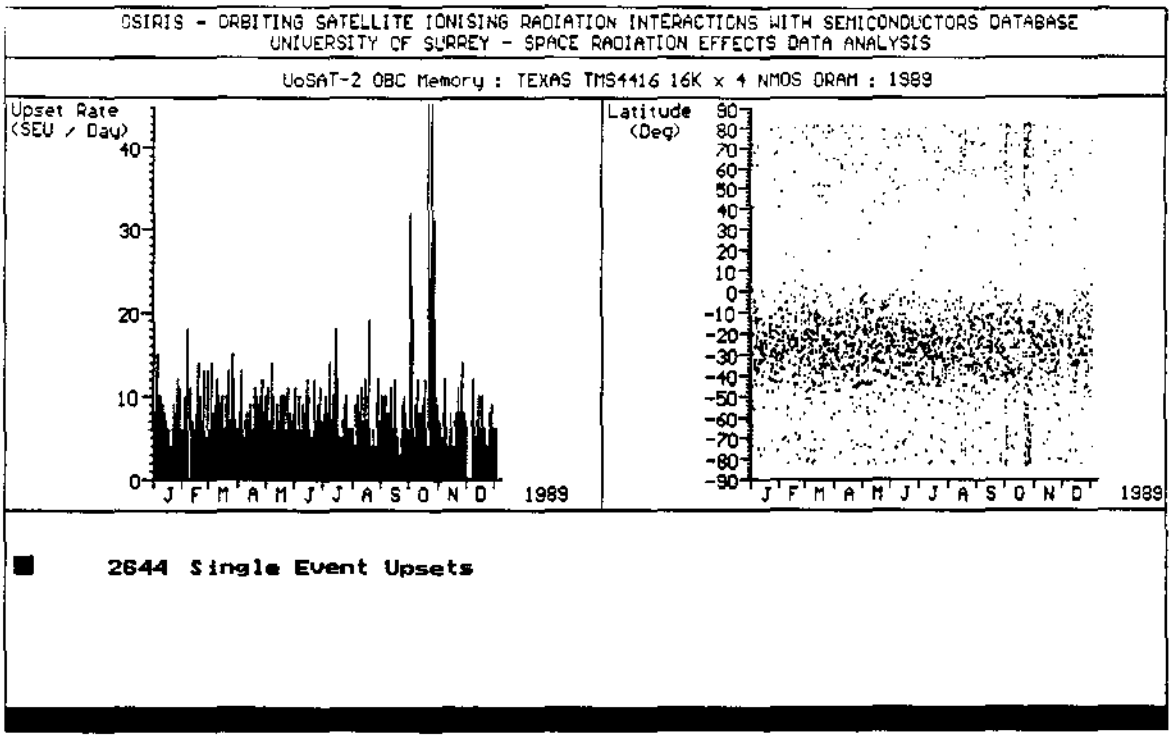

Fig 3. UoSAT-2 OBC Memory SEU Activity : January - December 1989

These patterns of behaviour are also repeated in the other memory systems. However, here the pattern shows up most clearly, due to the relatively high sensitivity of the 4416 devices in the OBC.

By combining these data with a model of the Earth's magnetic field and Solar Geophysical Data Prompt Reports, it has been possible to determine the underlying error-rates due to the quiet galactic cosmic ray (GCR) background, the quiet SAA proton population, and to solar-flare particles. In parallel with these in-orbit studies, a set of memory devices, identical to those flown on UoSAT-2, have been tested at the Harwell Variable Energy Cyclotron (VEC) facility in the UK, and the Paul Scherrer Institute (PSI), in Switzerland [18].

The results of these tests are currently being fed into computer models of radiation-effects, and the space radiation environment, in order to assess the correlation between the predictions of these models and the actual in-orbit performance of the devices.

The Cosmic Particle Experiment / Total Dose Experiment (CPE / TDE)

The University of Surrey's latest 'lightsat', UoSAT-3, which was launched into an 800 km near-polar Sun-synchronous orbit in January 1990, carries with it a space-radiation monitoring experiment (CPE / TDE) built by A.E.A. Technology, Harwell, on behalf of the Royal Aerospace Establishment (Space Department), Farnborough, UK.

This enables the radiation environment in and around the spacecraft to be measured directly, allowing a quantitatve analysis of the effects of that environment upon the spacecraft's systems - which includes the bulk semiconductor memory devices in the PACSAT Communications Experiment (PCE) transponder [19].

The TDE consists of seven specially manufacured p-channel MOSFETs, called RADFETs, which have an unusually thick gate-oxide layer (typically 0.5 micron). As the ionising radiation dose increases, so more positive charges become trapped in the gate-oxide, leading to a reduction in the threshold voltage (V_T) of the device. By arranging a normally-biased and a normally-unbiased RADFET pair on the same chip, it is possible to compensate for temperature effects, and the change in V_T becomes proportional to the total dose received. For a 0.5 micron gate-oxide RADFET, V_T falls about 1V for every kilorad of dose. It is expected that the sensors inside UoSAT-3 (four in the CPE/TDE payload, one in the PCE payload, and one between the battery boxes), will acquire a kilorad of dose after approximately 3 years in orbit. The seventh RADFET is less sensitive (0.1 micron gate-oxide), and is placed on the exterior of the satellite. This should change by 1 volt for every 10 kilorads of dose (approximately one year in orbit).

The CPE gives a measure of the short-term radiation environment inside the spacecraft, integrated over a five minute period. It consists of two detectors, each of which is based upon large (1 cm^2) area PIN diodes, which generate small amounts of charge as particles interact with them (typically around 0.1 pC). The Low-Area Detector (LAD) consists of a single PIN diode, capable of measuring high-fluxes of low-energy particles. The High Area Detector (HAD) consists of ten PIN diodes, arranged in parallel. This is connected to a pulse-height analyser, which sorts out the particles detected into eight energy 'bins'. This is suitable for measuring the relatively infrequent, more-energetic particles. The experiment is primarily controlled by an 80C31 microcontroller, which has 8K bytes of data memory and 16K bytes of program memory.

The CPE/TDE communicates with the PCE every 5 minutes, so that the data from the experiment can be stored in a file. Each day, a file of radiation data is downloaded to the groundstation at Surrey, where it is analysed, before being passed on the RAE Farnborough, and A.E.A Harwell.

Fig 4. shows a graph of the low energy particle count from the CPE's large-area PIN diode array detector.

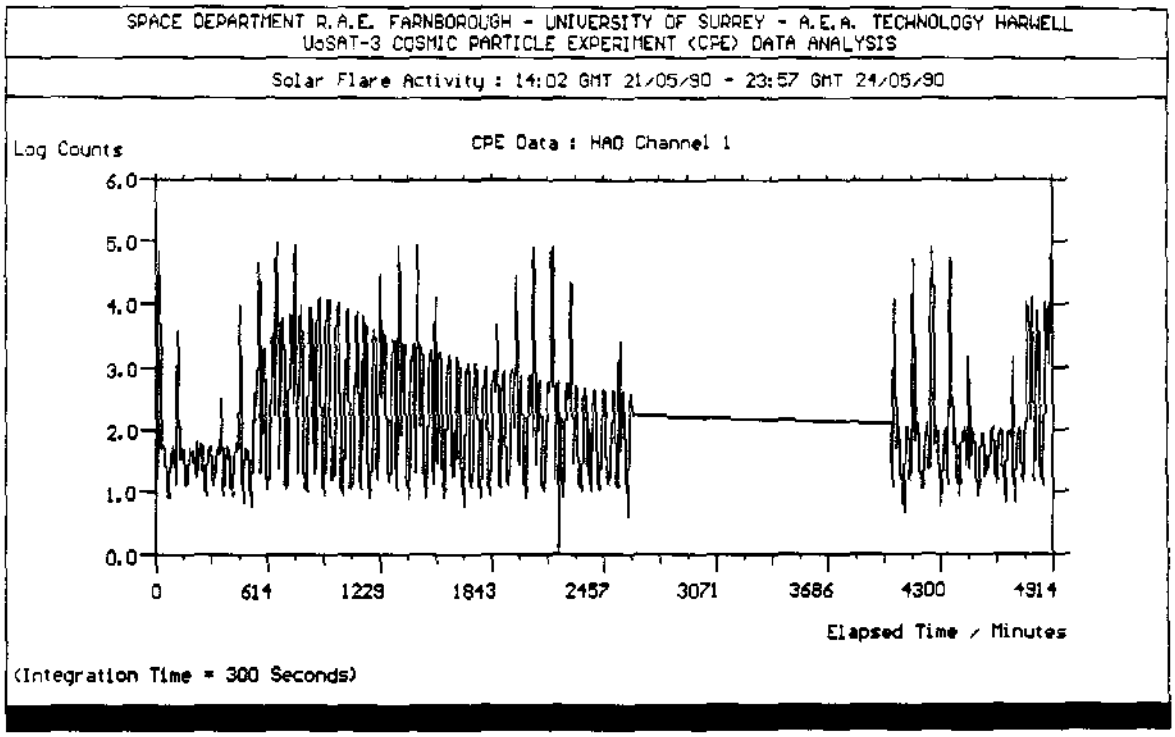

Fig 4. Solar-Flare Enhancements of the Auroral Oval Region Detected by the UoSAT-3 Cosmic Particle Experiment

The regular spikes are traversals of the SAA, whereas the other, lower magnitude spikes, are crossings of the auroral ovals. At the left of the graph, the auroral levels are showing normal activity, but near midnight on 21st May (approximately T+450 minutes), there is a sudden enhancement of auroral-region activity due to a solar-flare event, which slowly decays over the next few hours (the flat line towards the centre-right is due to the instrument being turned-off temporarily). However, during the evening of the 24th, another sudden enhancement takes place, and infact continues over the next few days.

CONCLUSIONS

The monitoring of in-orbit SEUs on UoSAT-2 has provided several interesting statistics, allowing direct comparison of static and dynamic RAMs ranging in capacity from 4 kilobits to 64 kilobits per chip. The SRAMs are significantly less susceptible to SEU than the DRAMS - in some cases by more than an order of magnitude. The static RAMs themselves do not vary conclusively as a function of chip capacity, and comparisons based on feature size will be necessary.

288K bytes of the SRAMs being monitored on UoSAT-2 are 8-bit-wide devices, and it was anticipated that these RAMs would experience frequent multiple bit upsets, with more than one upset bit in a given byte. Contrary to these expectations, no multiple bit errors have been observed in either of the two 96K byte banks of Toshiba TC5516 2K-by-8-bit devices in the DSR. Similarly, no multiple bit events have been observed in the 32K of Hitachi HM6116 2K-by-8-bit devices in the DCE RAMUNIT, although three 'extended' errors have been observed in the 64K of Hitachi HM6264 8K-by-8-bit devices in the RAMUNIT. Of these, one 'extended' event could be analysed in terms of the error pattern, and was found to consist of a single bit error in two neighbouring bytes, and so a multiple bit error in a single byte has yet to be observed.

The orbital analysis of UoSAT-2 SEUs shows an overwhelming concentration of events in the South Atlantic Anomaly for all device types, with a marked enhancement of auroral-region activity during periods of solar-flare activity. This was particularly the case during the major flare event of 19th October 1989. This result suggests that the SEU mechanism of primary concern for the UoSAT-2 orbit is that due to proton induced nuclear reactions within the device.

The UoSAT-2 satellite has been operational in orbit since 1st March 1984. The spacecraft is in good shape and is confidently expected to operate for some years to come. Its predecessor, UoSAT-1, launched in October 1981, was still fully operational when it re-entered the Earth's atmosphere in October 1989 (UoSAT-2 is not expected to re-enter until some time next century). Thus, UoSAT-2 offers perhaps a unique opportunity to examine the long-term effects of the space radiation environment upon a variety of semiconductor RAMs and other microelectronic devices.

Some aspects of the device's behaviour which would be addressed by such a long-term monitoring program include, examining the effect of total-dose on the SEU sensitivity of the devices, looking for changes in activity as the solar cycle reaches its peak and declines, and noting device failure mechanisms as and when they occur. For example, it is interesting to note that single-event latch-up has not been observed in any of the devices on UoSAT-2, despite their being in active use for a substantial part of the spacecraft's lifetime. This result is contrary to that which might be expected from ground-based testing of similar devices.

From January 1990, UoSAT-3 has joined the University of Surrey's fleet of technology demonstrating spacecraft. This satellite has on-board space radiation monitoring payloads and hosts a variety of modern microelectronic devices, further augmenting the space-radiation effects research being carried out at Surrey.

ACKNOWLEDEGEMENTS

I should like to thank Jeff Ward, Principle Investigator of Store-and-Forward Communications Systems at UoSAT, who is presenting this paper on my behalf, and was responsible for much of the original work on SEU analysis for the UoSAT spacecraft. I should also like to acknowledge the funding and support given to this research by the European Space Agency: ESA-ESTEC, and the Royal Aerospace Establishment, Farnborough.

REFERENCES

[1] M.N. Sweeting, "The University of Surrey UoSAT-2 Spacecraft Mission" *J.IERE*, Vol. 57, No. 5 (Supplement), Sep/Oct 1987, pp. S99-S115. [Institution of Electronic and Radio Engineers, London, UK.]

[2] R.M.A. Peel, "The Primary UoSAT-2 Spacecraft Computer", *J.IERE*, Vol. 57, No. 5 (Supplement), Sep/Oct 1987, pp. S132-S142. [Institution of Electronic and Radio Engineers, London, UK.]

[3] J.M. Radbone, "The UoSAT-2 Spacecraft CCD Imaging and Digital Store/Readout Experiments", *J.IERE*, Vol. 57, No. 5 (Supplement), Sep/Oct 1987, pp. S99-S115. [Institution of Electronic and Radio Engineers, London, UK.]

[4] J.W. Ward and H.E. Price, "The UoSAT-2 Digital Communications Experiment", *J.IERE*, Vol. 57, No. 5 (Supplement), Sep/Oct 1987, pp. S99-S115. [Institution of Electronic and Radio Engineers, London, UK.]

[5] J.C. Pickel and J.T. Blandford Jr., "Cosmic Ray Induced Errors in MOS Memory Cells", *IEEE Trans. Nucl. Sci.*, Vol. NS-25, No. 6, Dec 1978, pp. 1166-1171

[6] E. Petersen, "Soft Errors Due to Protons in the Radiation Belt", *IEEE Trans. Nucl. Sci.*, Vol. NS-28, No. 6, Dec 1981, pp. 3981-3986

[7] J.H. Adams Jr., "The Variability of Single Event Upset Rates in the Natural Environment", *IEEE Trans. Nucl. Sci.*, Vol. NS-30, No. 6, Dec 1983, pp. 4475-4480

[8] W.L. Bendel and E.L. Petersen, "Proton Upsets in Orbit", *IEEE Trans. Nucl. Sci.*, Vol. NS-30, No. 6, Dec 1983, pp. 4481-4485

[9] J.H. Adams Jr. and A. Gelman, "The Effects of Solar Flares on Single Event Upset Rates", *IEEE Trans. Nucl. Sci.*, Vol. NS-31, No. 6, pp. 1212-1216

[10] A.J. Sims, P.R. Truscott, G.L. Wrenn and C.S. Dyer, "Environmental Constraints for Polar Platform Design", IAF-87-09, 1987, HMSO London.

[11] M.N. Sweeting, "Final Report on UoSAT-2 Single Event Upset Orbital Data Analysis", ESTEC Purchase Order No. 6041/7, Surrey Satellite Technology Ltd., Guildford, U.K., 1987

[12] C.I. Underwood and J.W. Ward, "The Extraction of Single Event Upset Data from the UoSAT-2 Spacecraft", Final Report for the European Space Agency, Contract No. 7396/87/NL/IW, Surrey Satellite Technology Ltd., Guildford U.K. 1990

[13] L. Johnson, "The OSCAR-11 Packet Experiment", ARRL 3rd Computer Networking Conference Proceedings, Trenton, USA, 1984

[14] J. Ward and H. Price, "The UO-11 DCE Message Store-and-Forward System", ARRL 5th Computer Networking Conference Proceedings, Orlando, USA, 1986

[15] J.W. Ward, "Observations of Single-Event Memory Upsets on the UoSAT-2 Satellite", 2nd Annual USU/AIAA Conference on Small Satellites, Logan, Utah, USA, Sep 18-21, 1988

[16] L. Adams, R. Harboe-Sorensen, E. Daly and J. Ward, "Proton-Induced Upsets in the Low-Altitude Polar Orbit", *IEEE Trans. Nucl. Sci.*, Vol. NS-36, No. 6, 1989

[17] J. Ward, "An Analysis of UoSAT-2 DCE Memory Performance", AMSAT-NA Technical Journal, Vol. 1, No. 1, USA, 1987

[18] R. Harboe-Sorensen, E.J. Daly, C.I. Underwood, J. Ward and L. Adams, "The Behaviour of Measured SEU at Low Altitude During Periods of High Solar Activity", IEEE Nuclear and Space Radiation Effects Conference, 1990, Paper 244, Poster Paper PD-6.

[19] J. Ward, "The UoSAT-D Packet Communications Experiment", 7th ARRL Amateur Radio Computer Networking Conference, Columbia, Maryland, USA, Oct. 1988