A novel, low power optical communication instrument for small satellites

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ABSTRACT

The Miniature Optical Communication Instrument is a NASA-sponsored compact, pulsed optical communication system for distant, power-constrained small satellites. The primary motivation for this system is to reduce the power required for the laser transmitter and to enable variable repetition rates in order to produce a versatile instrument for small satellites down to the CubeSat scale. A differential pulse-based scheme is driven by an FPGA-based Software-Defined Pulse Modulator. This not only improves the reach of the system but also reduces the size and principally the power required, with only a small reduction in data throughput. In addition to optical communication, the MOCI also has potential capabilities in precision clock synchronization and navigation beyond Earth orbit.

INTRODUCTION

Spacecraft communications using optical frequencies is widely recognized as a potentially more power efficient scheme compared to radio frequency communications. This is because the fundamental divergence angle limits of electromagnetic waves are proportional to their wavelength, and therefore, the fraction of transmitted power that is captured by the receiver is inversely proportional to the wavelength squared. Optical frequencies have wavelengths that are many orders of magnitude less than that of radio frequencies used for communications. For example, the wavelength of 1550 nm near-infrared light is 2×10^{-4} times shorter than X-band with a wavelength of ~3 cm, potentially resulting in a 4×10^{8} fold increase in received power for a given amount of transmitted power.

Pulsed optical communications systems utilizing pulsed fiber lasers or Q-swithced lasers allow high optical energies (> 1 mJ) per pulse, while exhibiting only modest average power levels (~ 1 W). This is important for long distance communications, because accurate detection of these pulses depends on the number of photons (or energy) received.

The most recent demonstration of laser communications from space was the Lunar Laser Communications Demonstration (LLCD) on board the LADEE mission[1]. This system demonstrated a record breaking 622 Mbps downlink and 20 Mpbs uplink over lunar distances (~400 Mm). The space segment of the LLCD had a mass of 32 kg and required 137 W electrical power to produce 0.5 W of average optical power. While this is an impressive achievement, the power and mass levels for this instrument are inconsistent with what is commonly available on small satellites and nanosatellites.

At the Precision Space Systems Laboratory (PSSL) at the University of Florida, we are developing the Miniature Optical Communications Instrument (MOCI), a compact pulsed laser transmitter with a target mass and power consumption level of 2 kg and < 10 W while transmitting. A prototype implementation of this technology is currently being developed to TRL 3 by 2017. There are several similarities between LLCD and the proposed MOCI, including a flavor of Pulse Position Modulation and a fiber amplified 1550 nm laser diode system. However, the focus of the LLCD was maximizing data rates using a high reliability instrument, while the MOCI project explores the minimum power regime and CubeSat-compatible components. To achieve such a dramatic drop in SWaP over the LLCD instrument, the MOCI sacrifices bandwidth relative to LLCD and takes advantage of several efficiency maximizing techniques. One such technique is using fewer average laser pulses per second to lower the average power consumed, while maintaining peak laser power levels on the order of that of the LLCD.

The MOCI is composed of two main subsystems: the Software Defined Pulse Modulator (SDPM) and the Master Oscillator Power Fiber Amplifier (MOPFA) laser system. Both subsystems take advantage of precision timing components and electronics developed in the PSSL for the Optical Precision Time-transfer Instrument, which will demonstrate ground-to-space clock synchronization to 100 ps during a planned 2017 CubeSat flight.[2]

The MOPFA system is a 1550 nm fiber laser with target pulse widths of 100 ps and pulse energies of ~1 mJ. To keep the average power low, the minimum period between pulses, or guard time T_g, is chosen to be longer than traditional pulsed laser communications systems. This allows lower power pump lasers to more slowly store the needed energy in the fiber. The MOPFA uses a ~50 mW 1550 nm seed laser diode. The light pulses emitted by this laser are fed into erbium-doped fiber amplifier, with one or more stages, pumped by ~100 mW 980 nm laser diodes.

To take advantage of the longer guard time, the employed modulation scheme is a Differential Pulse Position Modulation (DPPM) with a variable symbol length. DPPM uses the value of the delay between two successive pulses to send data. The number of symbols M that a delay encodes can be chosen to increase the power efficiency or increase the data rate. Shorter symbol lengths allow for higher data rates at the expense of higher power, while longer symbol lengths increase the quantity of information per pulse and reduce the power consumption. While M-DPPM and its application to space optical communication is not new, recent technological advances in FPGA technology and in the miniaturization of precision clocks allow for stable delay generation over relatively long delays, with a system that exhibits extremely low power consumption. This in turn enables a large M and therefore low average optical power with high peak power. High data rates are maintained (10 kpbs to 100 Mpbs) thanks to efficient modulation codes and very short slot times (100 ps).

The SDPM generates rising-edge triggers for the seed laser diode driver with 100 ps precision. The modulator is entirely implemented in a Field Programmable Gate Array (FPGA) to keep power, volume and complexity under control. A compact, low power cesium oscillator, the Chip-scale Atomic Clock (CSAC)[3], is used as reference to generate the delays. The signal of the CSAC is fed to a Delay Locked Loop to account for environmental effects on the FPGA modulator.

The MOCI is designed to be a versatile instrument useful for a fairly wide array of mission concepts. Given its low size, weight and power requirements, and its software-defined modulation rate, it could be incorporated in a CubeSat of at least 3U or on larger deep space spacecraft that are power-constrained. Since its design will be made consistent with existing ground terminals, for example those used for the LADEE mission[4,5], it can be readily incorporated into future missions.

SOFTWARE DEFINED PULSE MODULATOR

Modulation Scheme

The M-slot Differential Pulse-Position Modulation (M-DPPM) scheme is related to M-slot single-pulse Pulse Position Modulation (M-PPM), which uses a fixed symbol interval divided into M time slots (even)[5]. During each symbol interval $\log_2 M$ bits of information are transmitted. If we assume that the length of each of the M time slots is τ seconds, then under ideal circumstances the length of each symbol interval is $M\tau$. However, for practical reasons the laser pulses cannot be generated arbitrarily quickly. We therefore must account for a guard time, T_g, which is the minimum amount of the between pulses. The length of each symbol interval then becomes $M\tau + T_g$, and the resulting data rate for the M-PPM scheme D_{PPM} in units of bits-per-second (p/s) is:

$$D_{PPM} = \frac{\log_2 M}{M\tau + T_g} \tag{1}$$

For T_g on the order of τ seconds, the value of M that optimizes the data rate is $M = 4$. Indeed, the recent LADEE mission utilized a 4-PPM laser communication scheme[1].

A Differential Pulse-Position Modulation (M-DPPM) scheme uses the value of the delay between two successive pulses to send data. The possible lengths of each delay are discretized into M bins, each τ seconds long. Again, the number of bits transmitted with each pulse is $\log_2 M$. The length of each symbol interval is now variable. However, if we assume that the data to be transmitted consists of symbols that are uniformly distributed among all possible symbols, then the average length of each symbol interval is $(M+1)\tau/2 + T_g$. Therefore, the average data rate for the M-DPPM scheme D_{DPPM} is:

$$D_{DPPM} = \frac{\log_2 M}{(M+1)\tau/2 + T_g} \tag{2}$$

For negligible T_g, the M-DPPM scheme increases the data rate by roughly a factor of two. For long T_g, the M-DPPM still has an advantage with respect to data rate relative to M-PPM, since the optimal value of M is such that $(M+1)\tau/2 \sim T_g$.

If we assume the MOPFA system is capable of using a variable guard time, T_g, to increase or decrease optical power P, and if P is proportional to T_g, then the square of the guard time, T_g, is a proxy for distance between transmitter and receiver. The user then has the capability of choosing the guard time to meet received optical

power requirements. The value of M that the FPGA uses to convert data into pulses is taken to be that which maximizes the data rate, D_{DPPM}, given above.

The length of each time slot, τ, also impacts data rate. In general, for high data rates we want small τ and small T_g. Unlike T_g, though, τ is limited by both the modulator and its clock, as well as the laser system. As we will show in the next subsection, modern FPGAs can achieve slot widths on the order of τ = 100 ps when environmental effects are compensated and static errors are calibrated.

To illustrate the versatile nature of the MOCI, we calculate the value of M that maximizes the data rate for a given value for the time slot and required guard time. Figures 1 and 2 show the optimal M for both the M-PPM and M-DPPM schemes and the resulting data rates as a function of T_g and τ. For T_g = 1 ns and τ = 100 ps, a data rate of 3 Gbps is possible using M-DPPM and 2 Gbps for M-PPM. When large guard times are needed to produce sufficient optical power for very long range communications, the optimal M increases and the resulting data rate drops.

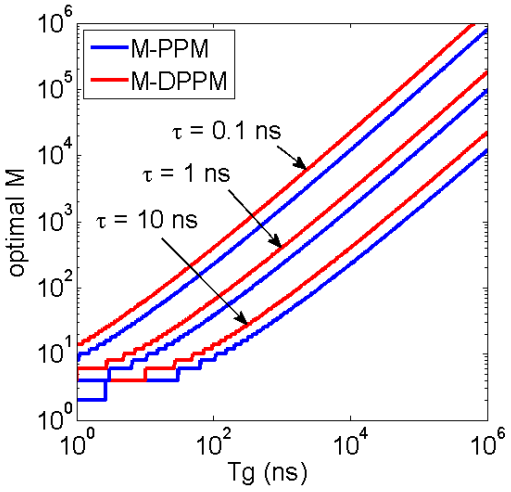

Figure 1: Slot number, M, that maximizes the data rate for M-slot Differential Pulse Position Modulation (M-DPPM) and Pulse Position Modulation (M-PPM) schemes for a given τ and T_g.

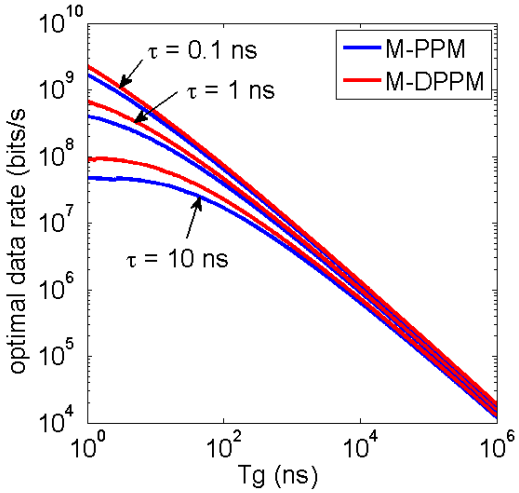

Figure 2: Optimal data rates for the M-DPPM and M-PPM schemes for a given τ and T_g.

As T_g increases so does the requirement for the frequency stability of the on-board clock. Figure 3 shows an estimate of the required short term Allan deviation for the on-board clock. For τ = 100 ps and a guard time of 1 ms, the required Allan deviation is 10^{-8}, which is lower than typical quartz oscillators. The required clock frequency stability shown in Figure 1 simply assumes that the clock's time error after one symbol interval $M\tau$ is less than 0.1τ and that longer term clock drift can be corrected on the ground by tracking the small deviations in the received pulse time with respect to the expected time, which must be some integer n times τ seconds after the previous pulse.

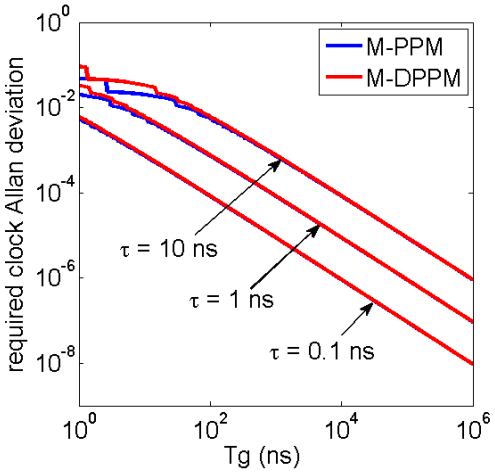

Figure 3: Required clock Allan Deviation for the M-DPPM and M-PPM schemes for a given τ and T_g.

A candidate clock is the Chip Scale Atomic Clock (CSAC) manufactured by Microsemi Frequency and Time Corporation. The CSAC, with a measured short term Allan deviation of 2×10^{-10}, has an extremely low

power consumption of < 120 mW, a volume of < 16 cc, and a mass of < 35 g[3]. Microsemi is currently in the process of space qualifying this clock.

An M-PPM symbol carry $\log_2 M$ bits, so to reduce the impact of an error, it is desirable that an error of one time slot only affect one bit. This can be achieved by Gray codes, in a way similar to Quadrature amplitude modulation schemes.

Architecture

In addition to the M-DPPM scheme, a sequence of other activities is required to generate electrical pulses from the raw input data. The data flow is described in Figure 4. The first step is to apply a forward error correction code, for instance Turbo Codes. Then, the data is packed into elements of the size of one M-DPPM symbol, and a Gray code is applied. After that, the data is encoded with the M-DPPM scheme, resulting in a string of timestamps. These timestamps are then separated in two parts in order to be electrically generated: a counter value, and a delay chain setting. The first value is compared to a running counter and creates a base pulse. The second value is a setting of a variable delay chain, and shifts the base pulse in time to apply finer changes. Before the chain setting is applied to the delay chain, it goes through a calibration, using measurements from a delay locked loop described later in this paper.

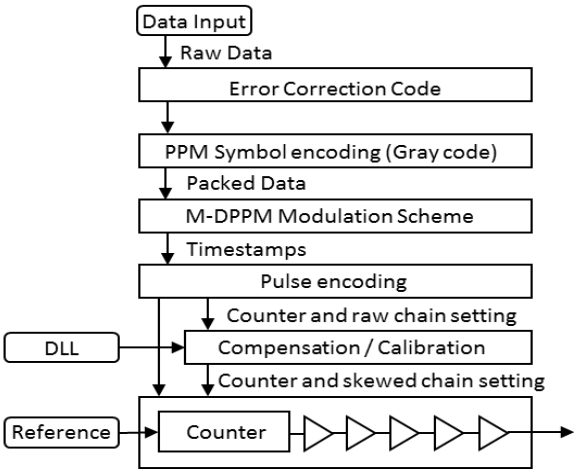

Figure 4: SDPM data flow

The modulator is implemented in 3 parts. The first part is responsible for the encoding of the data, including forward error correction, the M-DPPM scheme, and the application of environmental compensation and calibrations. This part is entirely realized in digital logic. This allows all parameters to be controlled, or complete replacement of the modulation scheme.

The second part includes the counter, the comparison register and the delay chain. All of these components can also be included in the FPGA, but the layout and the timing performance determine the accuracy of the modulator output. Therefore, implementation of this part is specific to the selected FPGA.

The third part is the delay locked loop and its control circuit. This part requires the ability to dynamically reprogram the hardware phased-locked loop of the device.

FPGA Selection

Several specific requirements drive the FPGA selection, including the presence of phased locked loops, the ability to quickly reprogram them and route their output freely. In addition, other criteria like the complete system complexity, the power consumption, the radiation tolerance and the existence of a hardened variant of the device were taken into account. The most important of these requirements are shown in Table 1 for the two most promising FPGAs, the Xilinx Virtex-5 and the Microsemi SmartFusion2.

Table 1: FPGA Selection

Device	Virtex-5	SmartFusion 2
Technology	SRAM	Flash
Power/ Complexity	High	Medium
SEU/SEL	Configuration SEU, no latch-up.	No configuration upset, susceptible to latch up
Rad tolerant version	Virtex 5 QV, limited availability	RTG4 150, Commercially available
Fine timing applications	Highly documented	Lightly documented

These requirements pointed towards Flash-based devices rather than SRAM FPGAs due to their reduced power consumption and system complexity, and their tolerance to radiation. Primarily because of its timing performance, the SmartFusion2 was the preferred device. A Rad-tolerant part with a similar architecture, the RTG4, is commercially available.

Delay chain

Two implementations of the delay chain have been attempted. The first design uses the delay variation within a cell, which depends on the input value. Because the path of the pulses does not change with different delay settings, routing variations have less impact on static errors and nonlinearities. The least significant bit (LSB) in the delay chain setting is typically equal to a 10 ps increase in the delay, and is consistent cell to cell. However, repeated routing of the signal through the local routing matrix results in large overall delays. The fixed

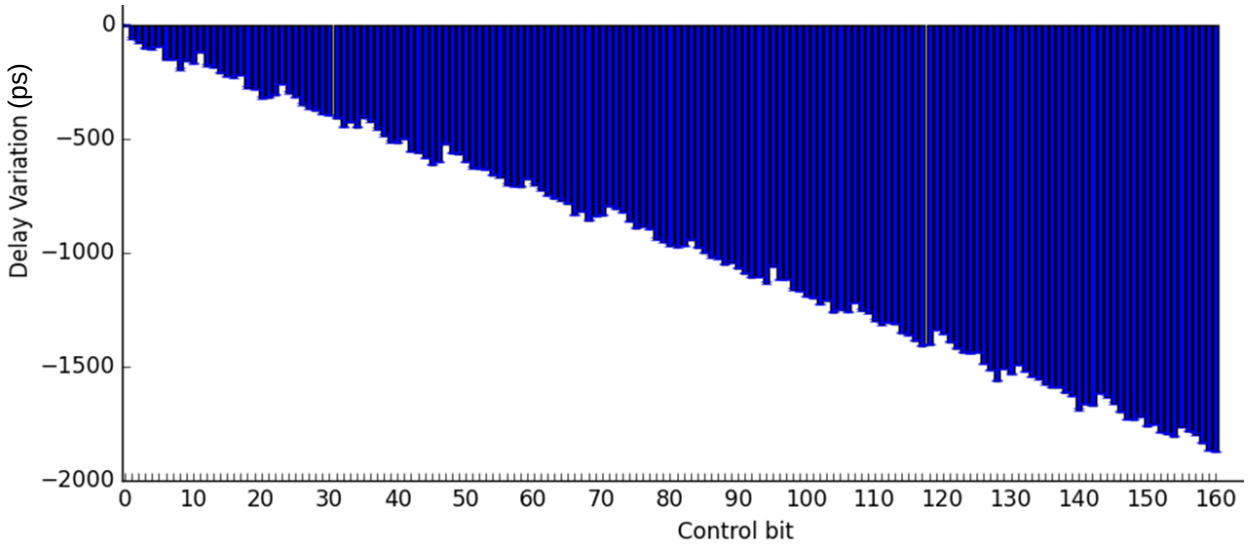

Figure 5: Delay chain propagation delay as a function of control input

delay is more than 60 ns for approximatively 2 ns of variable delay. The jitter also increases from 3.5 ps without the delay chain to 65 ps for a chain of 768 cells, the length required to cover more than one period of the counter.

A second design uses the carry chain and the clock network specific to the SmartFusion2 FPGA. The specific clock network is running along every cell in a row, and is propagating in the same direction as the carry chain. Different delays can be generated by selecting which cell the pulse travels through to jump from the fast row clock lane to the slightly slower carry chain. The delay variation for the first 160 settings is plotted in figure 5. The delay chain is much faster with an overall delay of 12 ns for a variation of 6 ns. The output jitter is the same as the base jitter, which is 3.5 ps. The typical LSB is 12 ps, however the delay increases were not monotonous and the nonlinearities more pronounced as is evident by the repeating deviations from a continuously decreasing slope in Figure 5. Since two delay chains are used, it is possible to balance the nonlinearities of one chain with the other.

Delay Locked Loop (DLL)

The delay in any integrated circuit depends on process, operating voltage, and temperature. This is an issue for space instruments, where temperature and aging are difficult to control. To maintain precision timing over the life of the communication system, delays must be measured accurately while environmental conditions change.

One solution for measuring delays is to use a Delay Locked Loop (DLL). In the DLL shown in Figure 6, a clock signal is generated by a variable frequency source. The signal is fed to a delay chain and then compared to itself. The rising edge of the delayed and non-delayed, direct signal will coincide if the delay is equal one clock period, or a multiple of that period. The loop can be maintained locked using feedback that adjusts the frequency source to keep the rising edges of both signals aligned. To implement a Delay Locked Loop in an FPGA, the variable frequency generator, the rising edge arbiter, and the feedback law must be implemented with FPGA modules.

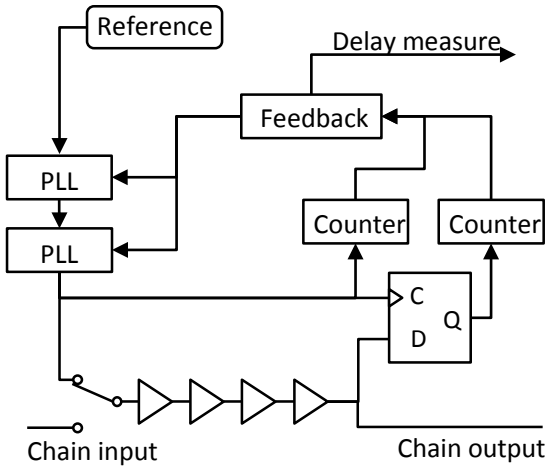

Figure 6: Delay Locked Loop block diagram

In traditional DLLs, the variable frequency generator is implemented with a Voltage Controlled Oscillator. In our implementation, we use one or several Phase Locked Loop (PLLs) to generate a variable frequency. The PLLs use frequency multipliers or dividers, and the frequency can be adjusted by reprogramming the PLL registers. Here, because the variable frequency is a multiple of a

known reference clock, the delay can be measured with an accuracy comparable with the stability of that clock. Using the SmartFusion2, with two Phase Locked Loops, and the 10 MHz CSAC as the reference clock, we achieve a variable frequency generator with a typical period resolution of 1 ps, and a worst-case resolution of 1.4 ps, over a clock period range of $T_{min} = 4$ ns to $T_{max} = 24$ ns.

The rising edge arbiter must determine whether the delayed signal or the direct signal arrives first. A clocked latch, present in all FPGA tiles, can determine if one signal arrives before another, by sampling one while using the other as a clock. In the proposed Delay Locked Loop design, the delayed clock signal is sampled using the direct signal. For a given delay period, we count the number of ones, which occurs when the delayed clock rising edge arrives before the reference rising edge, and divide this number by the total number of rising edges. We then vary the delay period until this fraction equals 50%, which occurs when the delay period is equal to one cycle of the reference frequency. This measurement is plotted in figure 7, over a range of delay periods near the transition region.

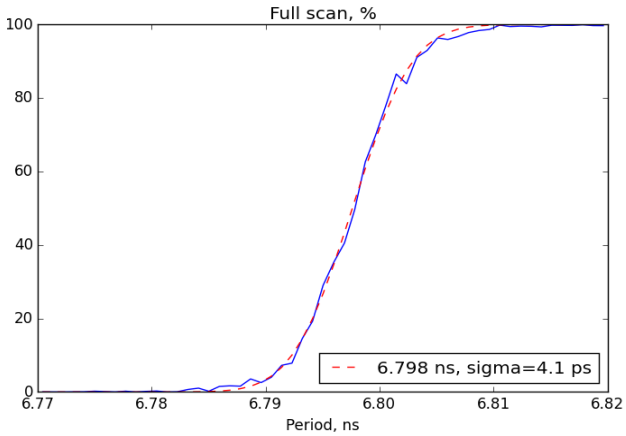

Figure 7: Fraction of ones at the DLL arbiter close to the transition

Figure 7 shows that the transition can be modeled as a cumulative Gaussian distribution. The standard deviation of that distribution can be interpreted as an error, due to the clock cycle-to-cycle jitter and the latch meta-stability. From Figure 4, we see that the clock signals in the FPGA fabric have a precision below 3.5 ps at room temperature. The measurement can be repeated at the same rate as the clock, between 40 MHz and 200 MHz for the proposed design. This allows the DLL to measure delays with a precision well below the jitter level, down to hundreds of femtoseconds.

The DLL arbiter measures the chain output against a clock rising edge. Because clock signals are periodic, if the DLL is locked with a period T, then it will also lock with any period $T_n = T/n$, as the rising edges will still coincide. This allows the DLL delay measurement range to be extended to longer delays. Measurements of delays up to 80 ns, with the mode $n = 5$, have been demonstrated. However, while the range of the DLL is multiplied by n for a given "harmonic", the effective resolution of the frequency generator at that mode is divided by n, reducing the measurement capabilities. The existence of several modes creates the need to distinguish between modes. If two periods, for two successive modes can be sampled, then the mode number can extracted using Eq. (3):

$$n = \frac{T_{n+1}}{T_n - T_{n+1}} \tag{3}$$

In order to sample at least one mode, the maximum period from the variable frequency source must be at least twice the minimum. The source must cover $[T_{min}, T_{max}]$ with $T_{max} > 2T_{min}$. To be able to sample two modes, and always extract the mode number n, T_{max} should be as least $T_{max} > 3T_{min}$.

Delays can both be measured in real time, while the modulator is operating to cancel environmental variation, or be used for static calibration. In the first case, the delay locked-loop sends signals through the chain when the chain is not used for data modulation, or through a parallel chain close to the one used for modulation. By repeatedly sampling the minimum and the maximum of the chain, the effect of both temperature and voltage can be cancelled using an affine function on the delay chain setting. When used to perform static calibration, the DLL measures all delay chain settings, one by one. The result of that operation allows us to generate a table that will reduce integral nonlinarites of the delay chain close to 1 or 2 setting LSB, and ensure that the delay variation is monotonous. This operation can be performed on-orbit, within the FPGA.

LASER SYSTEM

Optical Power Requirements

Four spacecraft-to-ground receiver distances are evaluated in order to demonstrate the range of performance capabilities of the MOCI. They are (a) the maximum and (b) the minimum distances between Mars and the Earth, (c) the distance between the Moon and the Earth, and (d) a 450 km low Earth orbit altitude. Optical pulse energy requirements for each of these four cases is calculated assuming a minimum of 200 photons reach a 1 m diameter detector aperture on Earth, at a 90°

elevation. The 1550 nm laser pulses are transmitted by the spacecraft through an 8 cm diameter telescope, and optical, pointing, and atmospheric losses, taken from Chapter 3 of Hemmati[7], have a combined efficiency of 23%. The resulting energy per pulse for each of these four cases is listed in Table 2.

Table 2: Optical Link Budget

Case	Distance (km)	Energy Required (mJ)
Mars to Earth (Max)	4.0×10^8	10
Mars to Earth (Min)	5.5×10^7	0.2
Moon to Earth	3.8×10^5	10^{-5}
LEO to Earth	450	10^{-14}

Table 3: Estimated Data Rates

Case	T_g (ms)	M	Data Rate (bits/s)
Mars to Earth Far	18	10^7	1,200
Mars to Earth Close	0.3	10^6	50,000
Moon to Earth	2×10^{-5}	10^2	3×10^8
LEO to Earth	2×10^{-5}*	10^2	3×10^8

* Limited by the SDPM

The energy required for all cases is achievable. However the MOPFA design to attain the maximum Mars to Earth case will need to be analyzed and designed carefully, to avoid issues that arise in high power systems like back reflections and nonlinearities.

For each case, 1 W of optical power is pumped into the erbium-doped fiber by the pump laser and its absorption efficiency is assumed to be 60%. The time needed for the pump laser to charge the fiber is one constraint for the guard time, T_g. A slot width of τ = 100 ps is used, and the optimal number of slots, M, is taken from the results shown in Figure 1. We take the minimum value for the guard time to be 20 ns, which is the current limitation of the modulator. At lunar distances, the guard time required for the MOPFA is roughly 20 ns, but for the 450 km LEO case, the MOPFA limited guard time under ideal conditions is several orders of magnitude below this value. These data rates are competitive with existing radio communications systems, even though the MOCI requires only a fraction of the size weight and power of such systems.

Master Oscillator Power Fiber Amplifier

The output of the SDPM is fed to a pulsed laser diode driver. This driver generates very short pulses of current through a 1550 nm laser diode with an output power on the order of 50 mW. Every rising edge produced by the modulator results in a pulse of 1550 nm wavelength light. A candidate pulsed laser diode driver architecture is similar to that of the Highland Technologies T165 picosecond laser diode driver, capable of producing 200 psec pulses with repetition rates up to 250 MHz. This driver has been tested in the laboratory at the University of Florida (UF) using a 1550 nm fiber-coupled seed laser diode. This setup was capable of producing 50 mW, sub-nanosecond optical pulses with a repetition rate of 10 MHz using a laser diode current of 400 mA. The configuration under test at the UF is shown in Figure 8.

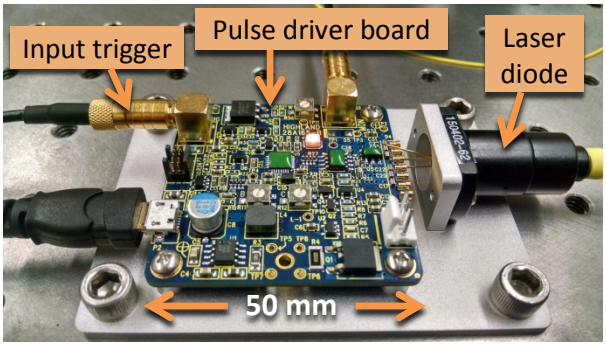

Figure 8: Picosecond laser driver and 1550 nm fiber seed laser

The pulsed output of the 1550 nm laser diode is fed into an erbium-doped fiber amplifier in a Master Oscillator Power Fiber Amplifier configuration. The pump laser diode with a wavelength near 980 nm is used to store energy in the amplifier, which is then released when the 1550 nm laser diode is pulsed. Fiber amplifiers offer more versatility than their Q-switched counterparts, allowing for arbitrary modulation of the pulses as well as changes in the transmitted pulse energy. The pump diode is driven separately from the seed diode and the time required to saturate the fiber amplifier increases with decreasing laser pump power. Therefore, decreasing the pump power increases the saturation time and thus the guard time. Consequently, a tradeoff exists between pump laser power and guard time. This tradeoff will be studied in order to maximize the data rate given the overall <10 W power consumption goal for the MOCI.

Downstream of the fiber amplifier will be a fiber coupled Faraday isolator and finally a small telescope to expand and collimate the beam. Since the target volume of the proposed instrument is 2 liters, the telescope aperture will be constrained to ~8 cm in diameter.

LABORATORY RESULTS

Initial Modulator Performance

A prototype of the Software-Defined Pulse Modulator, constructed in the Precision Space Systems Lab, is

shown in Figure 9. This setup is used to verify the SDPM's functionality and timing performance. The SmartFusion2 FPGA and a Microsemi development board is integrated with a Chip Scale Atomic Clock and a custom laser driver interface board.

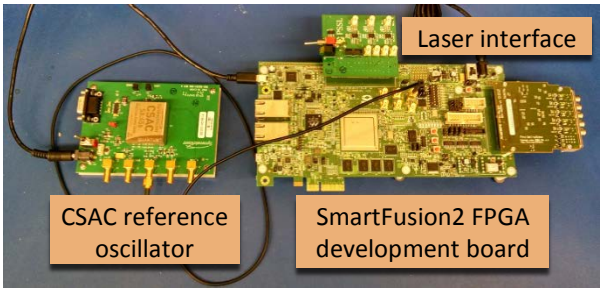

Figure 9: Software-Defined Pulse Modulator consisting of the SmartFusion2 FPGA, CSAC and laser driver interface board

The DLL environmental compensation software is incorporated, but the modulator is currently operating without data encoding and calibration. We achieved a maximum repetition rate of 50 Mhz (20 ns between pulses) using the second version of the delay chain design described above.

The SDPM prototype is capable of producing sequences of electrical pulses with prescribed delays. Figure 10 shows one such sequence with six pulses separated by 20 ns, 22 ns, 18 ns, 20 ns, and 18 ns respectively. Each electrical pulse is roughly 10 ns in width, but the rising edge is steep (~1 ns) and exhibits a measured jitter of just 27 ps. Prescribed delays can be generated by the delay chain with a resolution of 12 ps (uncalibrated), which is below the measured jitter.

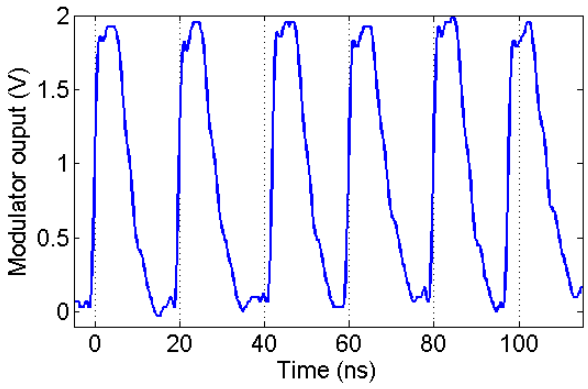

Figure 10: Variable delay pulse string

Initial Seed Laser and Driver Performance

In order to test the interface between the SDPM and the laser driver and to facilitate development of the MOFPA system, a custom interface board, shown in Figure 9, is integrated with the prototype SDPM. This interface board is connected to the Highland Technologies T165 laser diode driver via coaxial cable, and the driver is connected to a 50 mW, fiber-coupled 1550 nm seed laser diode. The pulse driver sends current through the laser diode based on rising-edge triggers generated by the SDPM. The laser's fiber optic cable is connected to a collimator, which allows the optical pulses to travel in free space for a short distance before being detected by an avalanche photodetector (APD). The laser, pulse driver, fiber collimator and APD are shown in Figure 11.

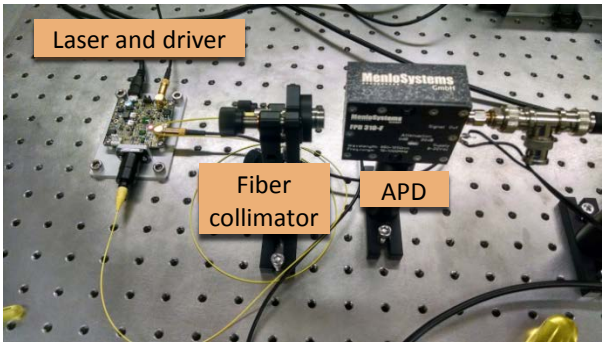

Figure 11: 1550 nm diode laser driver, fiber collimator and avalanche photodetector (APD)

A 5 GHz Tektronix oscilloscope is used to simultaneously record the output voltage of the SDPM, an echoed signal produced by the Highland pulse laser driver that is proportional to the current through the seed laser diode, and the output of the APD. A sequence of 500 pulses, evenly spaced by 200 μs, is recorded by the oscilloscope and shown in Figure 12.

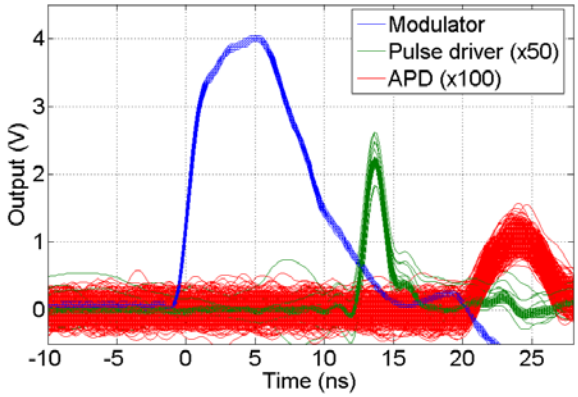

Figure 12: A sequence of 500 overlaid pulses produced by the modulator (blue), pulse laser driver (green), and recorded by the APD (red).

As is seen in Figure 12, these pulses are very consistently produced and detected. Small delays (10-15 ns) exist between the modulator, laser driver, and detector, which do not affect the overall performance of the system. The timing associated with each pulse is estimated using

simple rising edge detection. The timing jitter at the modulator, pulse driver, and APD, listed in Table 4, is taken to be the standard deviation of the 499 measured differences between successive pulse times. More elaborate detection schemes, such as combined rising and falling edge detection or curve fitting may produce more consistent results than those shown in Table 4.

Table 4: Measured Timing Jitter

Component	Jitter (ps)
Modulator	27
Pulse Driver	52
APD	244

The target slot width for the MOCI is 100 ps. From Table 4, we see that initial testing of the SDPM and pulse driver indicate that both sub-systems are consistent with this goal. The estimated timing jitter of the pulse driver may be conservative since the echoed signal produced by this device is known to be noisier than the current it drives through the laser diode. The APD timing jitter is greater than 100 ps, because of the bandwidth limitations of the commercial APD used. We are currently developing a custom APD circuit board, similar to an APD system used for OPTI[2], which has a measured timing performance of < 100 ps.

FUTURE WORK

The overall goal of this research is to elevate the technology readiness level of the MOCI to TRL 3 by the end of 2017. Over the next two years we plan to integrate the delay locked loop and the current modulator into a single system, and add the error correction code. The current delay chain routing can also be improved to further reduce nonlinearities, and will explore the timing characteristics of the hardened FPGA, the RTG4.

Also during this time, a one or two stage fiber amplifier system meeting the requirements listed in Tables 2 and 3 will be designed, tested, and integrated with the modulator. The new APD system, described above will also be integrated with the experimental setup. Finally, we plan to design and fabricate a prototype packaging for the MOCI that includes all of the components described in this paper plus an ~8 cm diameter beam expander. This packaging will be made consistent with a 2U CubeSat form factor so that it may be incorporated into a 3U or larger spacecraft platform.

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