Affordable Rad-Hard – Impossible Dream?

Presented to 2008 Small Satellite Conference

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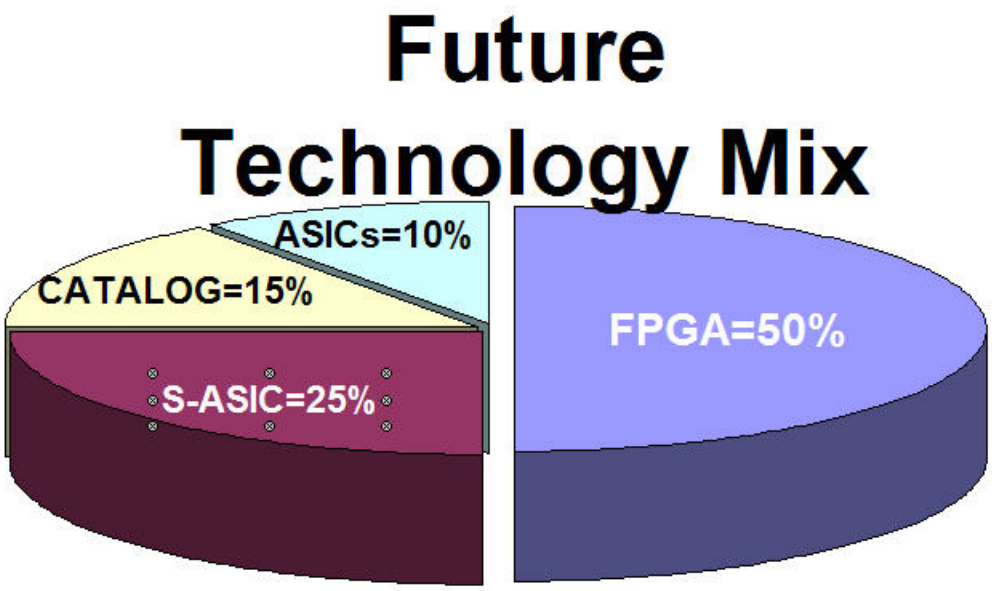
Outline

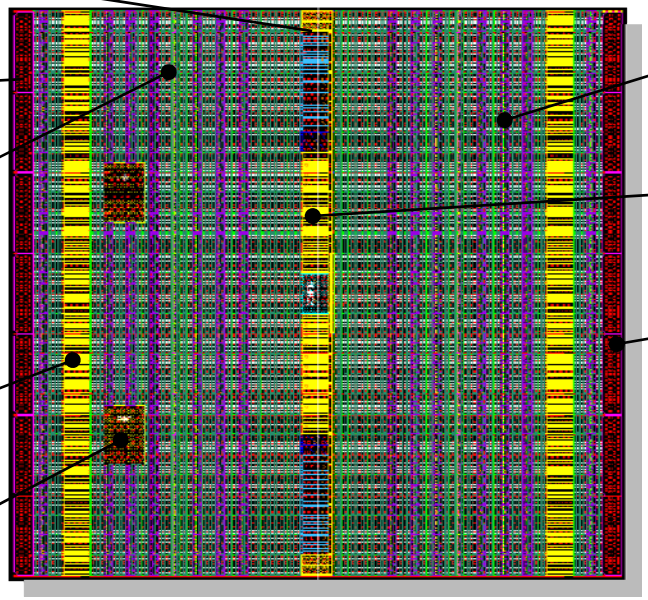
- Vision of parts mix for future satellites
- FPGA – commodity parts for space
- Structured ASICs – nano-scale performance at low cost
- Catalog parts – minimally invasive process for enhanced hardness
- ASICs – library for hardened by design

Parts Mix for Future Satellites

- **Tightly constrained piecepart budgets**
- **Reduced development time**
- **Decreased power allocations**
- **Increased on-board processing**
- **Standardized interfaces**



SIRF VIRTEX 5 Program



Phase-1: Design Feasibility, Test Chip

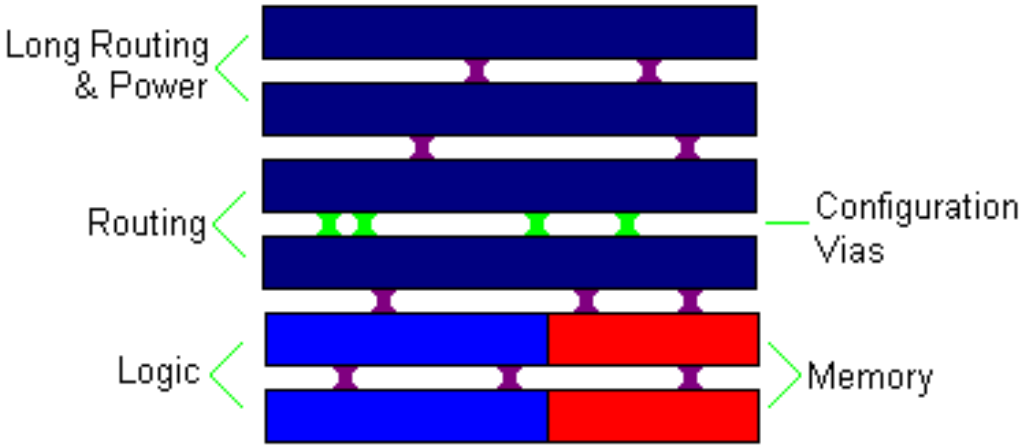
Phase-2: Chip Development

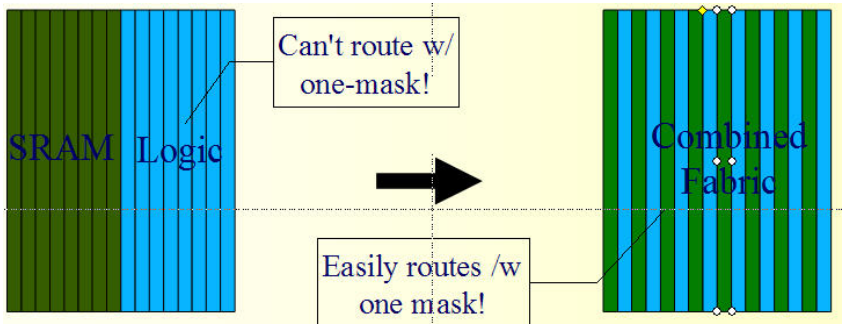
Phase-2A: Advanced Features

- **Total Dose 300 krad(Si)**
- **Single Event Latchup – None**
- **Single Event Upset**
  - **1E-2 data err/chip-day**
  - **1E-4 config err/chip-day**

Assumptions: AFRL rough estimates for comparable million gate applications. Typical ASIC budget is $10M, 2 yrs; typical FPGA budget is $2M, 6 months.

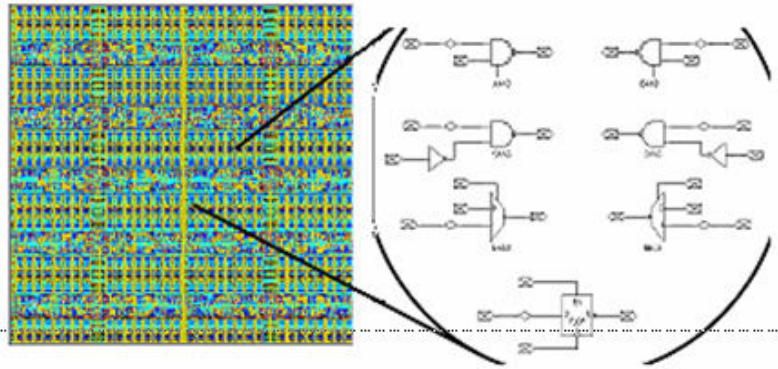
Structured ASIC Concept





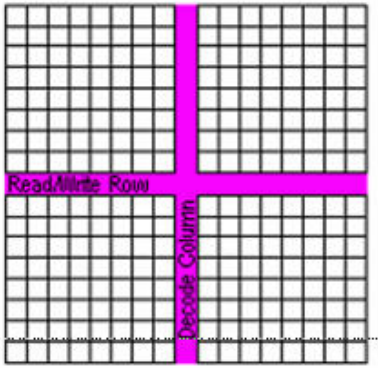
Patent 6,693,454

Logic Cell



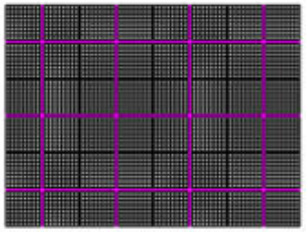
Logic Cells are composed of optimized simple gates and SRAM bit cells

Logic Tile



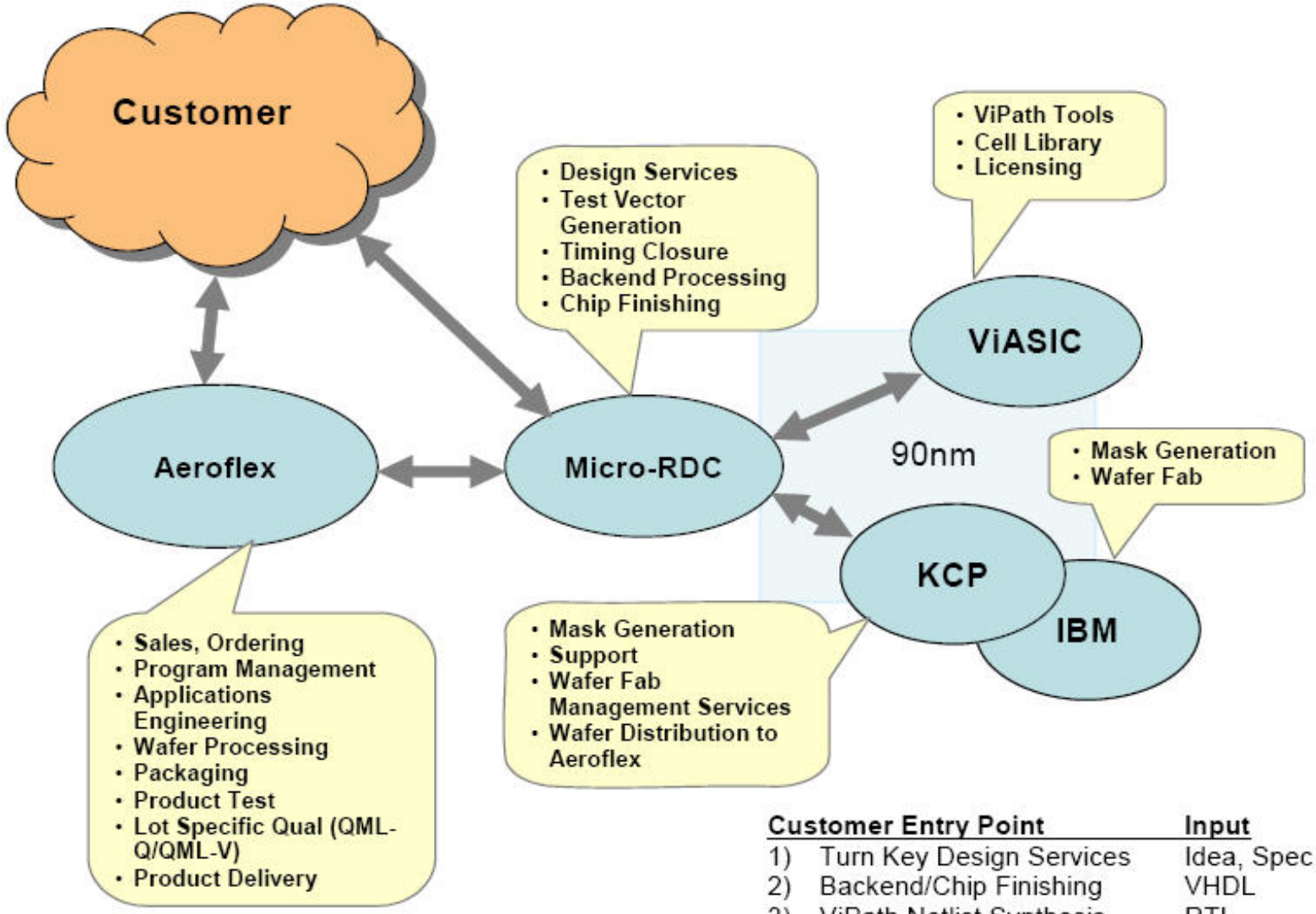
Logic Tile made from 16x16 array of Logic Cells and a 128x[1…32]b distributed SRAM

Footprints



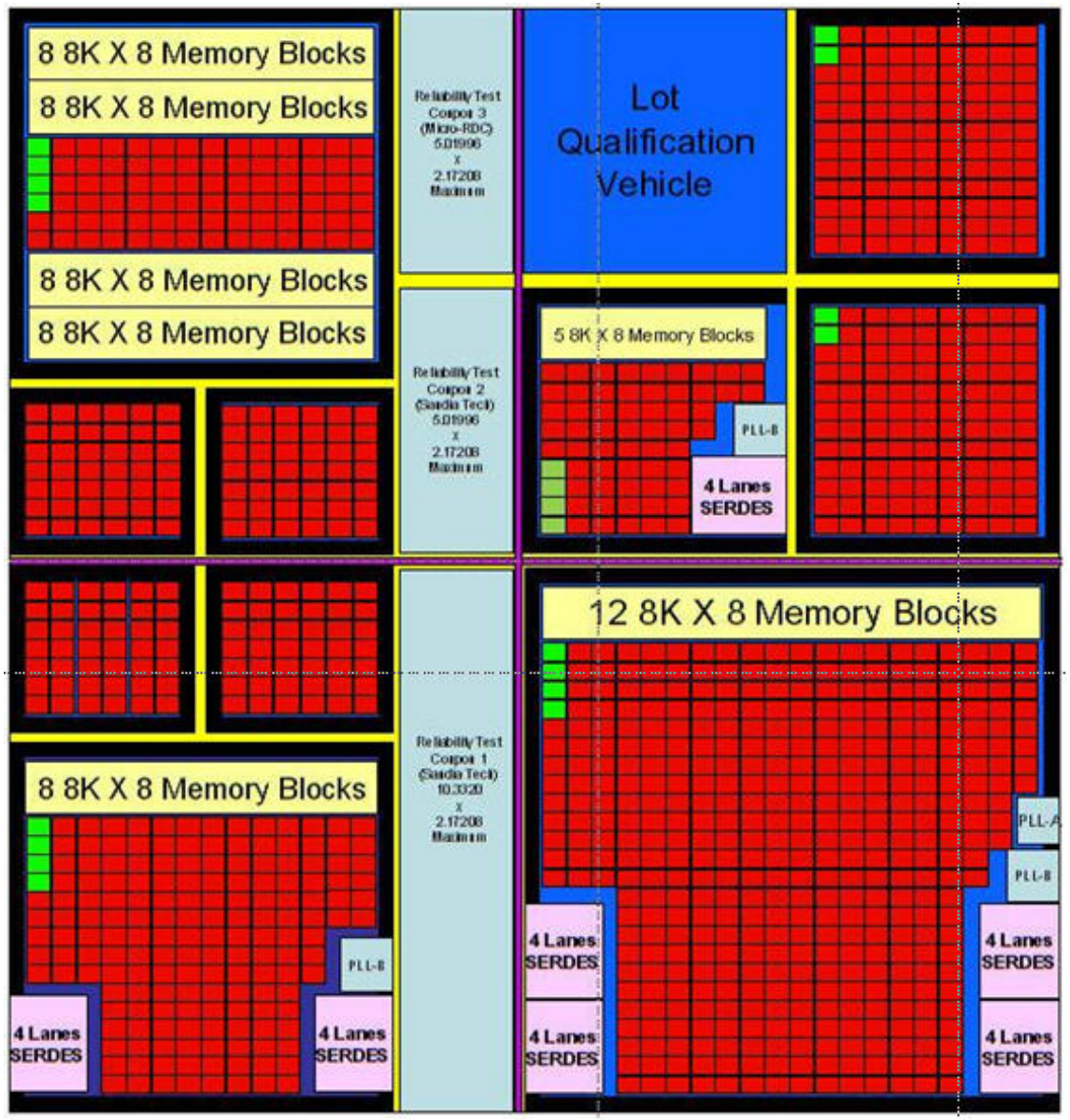
Footprints are any size array of Logic Tiles. Can be rectilinear to optimize space

S-ASIC TEAM



Customer Entry Point	Input
1) Turn Key Design Services	Idea, Spec
2) Backend/Chip Finishing	VHDL
3) ViPath Netlist Synthesis	RTL

Reticle Floorplan



- One 10 x 10 die
  - Full feature die
- Two 7 X 7 die
  - One full feature
  - One memory heavy
- Four 5 X 5 die
  - Two full feature
  - Two logic only
  - One full feature reserved for Lot Qualification
- Four 3 X 3 die
  - Three logic only
  - One location reserved for Reliability Test Coupon

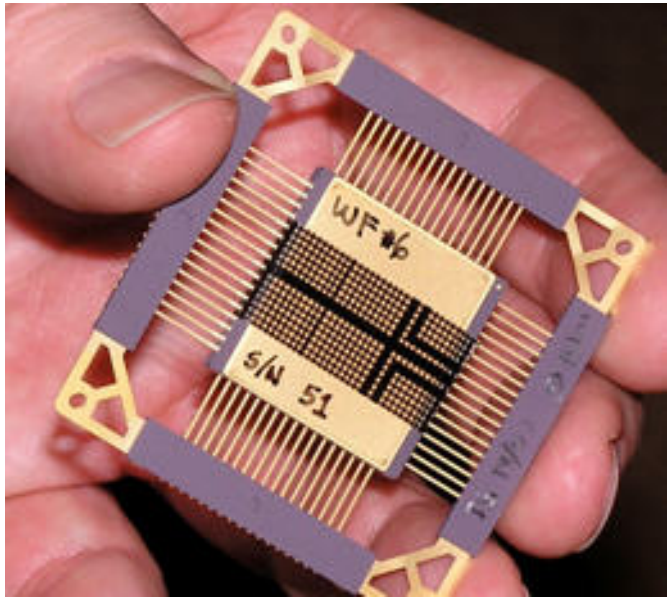
S-ASIC Features

Die Size	Total Pads	Pwr/GND	CMOS User IO	SERDES	PLL	Block SRAM	Distributed DP SRAM	Equivalent Logic Gates	SERDES LVDS*	PLL	VROM
3 x 3	172	60	96	0	0	None	~86K Bits	~126k	No	No	None
5 x 5 A	276	112	158	0	0	None	~217K Bits	~318K	No	No	256K Bits
5 x 5 B	276	92	128	28	18	5 Blocks 8K X 8	~125K Bits	~183K	Yes (4 Lanes)	Yes	512K Bits
7 x 7 A	410	114	192	56	18	7 Blocks 8K X 8	~356K Bits	~522K	Yes (8 Lanes)	Yes	512K Bits
7 x 7 B	410	154	248	0	0	28 Blocks 8K X 8	~164K Bits	~240K	No	No	512K Bits
10 x 10	604	152	328	112	31	8 Blocks 8K X 8	~850K Bits	~1.2M	Yes (16 Lanes)	Yes	512K Bits

* LVDS IO is only available if not using the SERDES lane(s).

16 Mbit SRAM Team

- **Silicon Space Technology**
  - **Minimally Invasive Implant Technology**
  - **16 Mbit Architecture**
    - **Silicon Design Solutions – Designers**
    - **DPACI – Prototype packaging**
- **Texas Instruments**
  - **180 nm process**
  - **12 wafers processed**
  - **3 splits**
    - **Baseline**
    - **Implant A**
    - **Implant B**
  - **First pass yield 40% to 50% (573 devices)**
  - **Process compatible with hardening catalog parts**

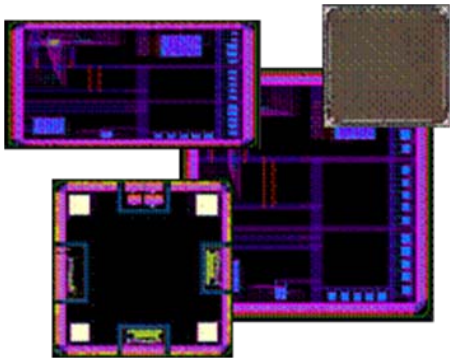


16 Mbit SRAM Characteristics

- **C05HA512K32 is a high performance CMOS SRAM organized as 524,288 words with 32-bit word.**
- **Configurable as Master or Slave device during package. Master device (C05HA512K32M) can initiate autonomous scrub and demand scrub cycles on Slave device (C05HA512K32S).**
- **20ns read, 10ns write maximum access time**
- **Functionally compatible with commercial 512Kx32 SRAM devices**
- **Built-in EDAC (Error Detection and Correction) to mitigate soft errors**
- **Built-in Scrub Engine for autonomous correction**
- **CMOS compatible input and output level, three state bidirectional data bus**
- **3.3 +/- 0.3V I/O, 1.8 +/- 0.15V CORE**
- **Radiation performance**
  - **Use both substrate engineering and radiation hardened by design (HBD)**
- **Packaging -- 68-lead ceramic quad flatpack (CQFP68)**

Library for Affordable ASICs*

- 1014 Cells - equivalent to commercial library with parameterized options for speed, power, radiation hardness. Designed and verified for IBM 9SF process.
  - Status V1 Library Status
    - Electrical, Functional, Radiation characterization complete
    - EDA views, models validated
    - Used in multiple circuit designs
    - SET generation and sensitivity characterization in work
  - DICE Status
    - V2 – Passed Go-NoGos, mitigated angular effects
    - V3 - Jan '08 Test – Used on OPERA/PDV1
    - V4 – May '08 Test



Development Step	Data included
Synthesis	• Liberty Format Files (.lib) • Synopsys Data Base Files (.db)
Simulation	• Verilog simulation models • VHDL VITAL simulation models • Cadence schematics
Placement & Routing	• Cell physical geometry • Cell frame views • Cell timing views • Cell power views • Technology file
Verification	• Cell SPICE netlist • Verification decks version
Support data	• Cell datasheets • Models & Design rules version

Bottom Line: The government owns this technology and will ensure that it is made available to any and all government contractors and both Boeing and DARPA concur with this position.

*Cohn, L.M., 2008 Fault Tolerant Space-borne Computing Workshop

Summary

- Affordability must be judged in terms of total system cost
  - Acquisition
  - Test
  - Application engineering
- Programs are underway to ensure the availability of reasonably priced, high performance pieceparts for space systems