AN FPGA-BASED JPEG 2000 DEMONSTRATION BOARD

SPACE DYNAMICS LABORATORY

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PROJECT GOALS

- DEMONSTRATE THE JPEG 2000 STANDARD IN FPGAs
- PLACE AS MUCH TIER1 AND TIER2 FUNCTIONALITY INTO TWO XILINX VIRTEX II FPGAs

BOARD FEATURES

IMAGE SIZE 256 x 256 PIXELS MIN

1024 x 2048 PIXELS MAX

BIT DEPTH 8 or 12 BIT GRAYSCALE

THROUGHPUT BENCH MARK 10 MPS

8 BIT 1024 x 2048 PIXELS

TILE SIZE 128 x 128 PIXELS

CODE BLOCK SIZE 32 x 32 PIXELS

WAVELET TYPES 5/3 and 9/7

OUTPUT QUALITY 1

LAYERS

OUTPUT FILE SIZE 512 KBYTES

BOARD FEATURES

FILE TYPE SEQUENTIAL TILE AND

TILE PART

HEADER TYPE UNWRAPPED J2K AND

JP2 USING THE PART 1

REQUIRED BOXES

COMPRESSION MODE LOSSLESS AND LOSSY

BASED ON BIT RATE CONTROL OR IMAGE

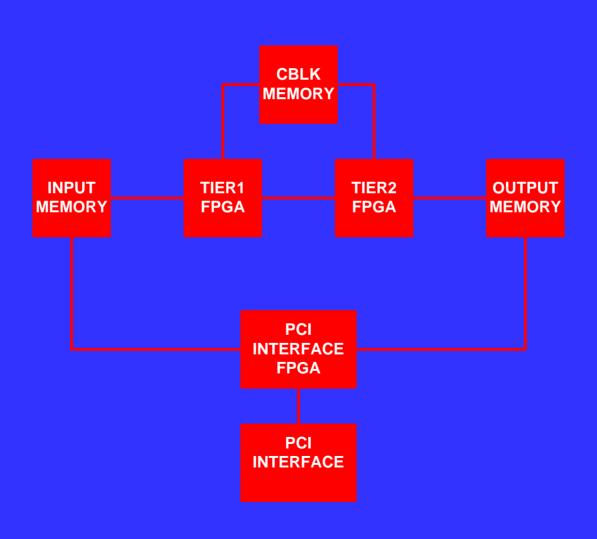
QUALITY

PCI INTERFACE

BOARD PICTURE



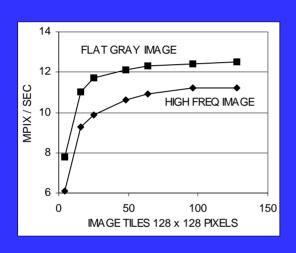
FUNCTION BLOCK DIAGRAM

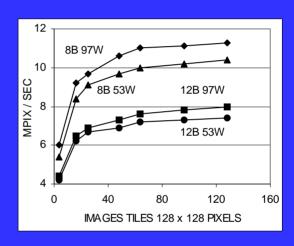


DATA FLOW



THROUGHPUT





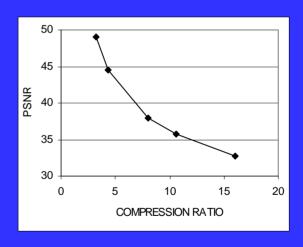
THROUGHPUT = IMAGE PIXELS / COMPRESSION TIME

COMPRESSION TIME STARTS AFTER THE IMAGE IS LOADED INTO THE INPUT MEMORY

COMPRESSION TIME ENDS WHEN THE EOC MARKER IS PLACED IN OUTPUT MEMORY

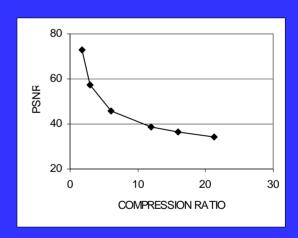
8 BIT PSNR vs COMPRESSION RATIO





12 BIT PSNR vs COMPRESSION RATIO





TILE OF INTEREST



CR = 4.4



CR = 18.5

FILE TRANSMISSION ERROR RECOVERY

DATA DROPOUT DURING TRANSMISSION WILL CAUSE FILE CORRUPTION

TWO TYPES OF ERROR RECOVERY ARE POSSIBLE WITH THE COMPRESSED FILES GENERATED WITH THIS DEMONSTRATION BOARD.

FILES GENERATED USING THE SEQUENTIAL TILE FORMAT WILL LOOSE THE PART OF THE IMAGE CONTAINED IN THE MISSING BYTES, HOWEVER THE OTHER TILES WILL NOT BE AFFECTED BY THE MISSING BYTES

FILES GENERATED USING THE TILE PART FORMAT CAN GENERALLY DISPLAY THE ENTIRE IMAGE, AFTER SOME DATA DROPOUT, BUT THERE WILL BE SOME LOSS OF IMAGE QUALITY OVER THE ENTIRE IMAGE.

ERROR RECOVERY SEQUENTIAL TILE FORMAT



ORIGINAL IMAGE



RECOVERED IMAGE

ERROR RECOVERY TILE PART FORMAT

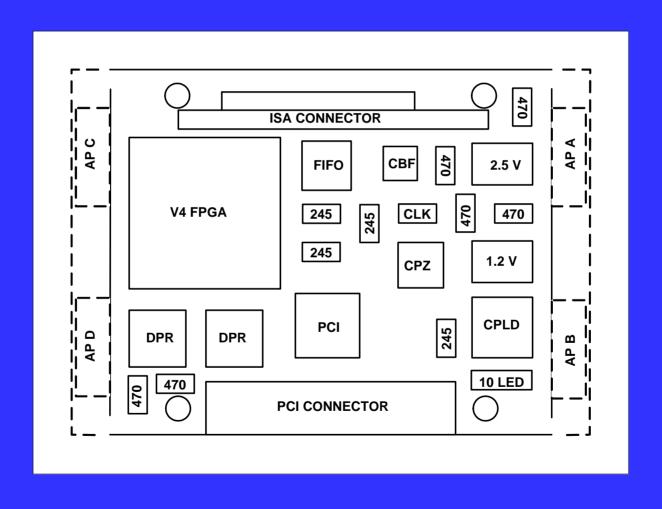


ORIGINAL IMAGE



RECOVERED IMAGE

SECOND GENERATION DESIGN



CONCLUSION

EXPERIENCE WITH JPEG 2000 IN A HARDWARE ENVIRONMENT

LESSONS LEARNED WILL AID IN THE DESIGN OF FUTURE SYSTEMS THAT WILL HAVE MORE FUNCTIONALITY AND SMALLER BOARD DESIGNS

THANK YOU