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Electronics Design of the AGLITE-LIDAR Instrument

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ELECTRONICS DESIGN OF THE AGLITE-LIDAR INSTRUMENT

by

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ABSTRACT

Electronics Design of the AGLITE-LIDAR Instrument

by

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The AGLITE-LIDAR instrument is a three-wavelength lidar system being designed and constructed at the Space Dynamics Laboratory under contract from the Agricultural Research Service. Its purpose is to implement a novel new approach to making measurements of gas and particulate pollutants released into the atmosphere by agricultural operations. Once operational, it will provide a means whereby the total flux of pollutants being emitted by agricultural facilities might be measured. This approach is valid even for facilities that may cover several acres.

The design of the AGLITE instrument consists of a myriad of different components that are brought together in a strictly coordinated system. The overall design is broken into three main categories: the mechanical, optical, and electrical designs. The electrical design is equally essential in the operation of the final instrument as the mechanical and optical aspects and is closely intertwined with their workings. The electronics include all of the sensors and detectors, the data acquisition systems, the

component control and synchronization circuitry, and the computers and data links. Combined with software, these allow the overall control of the system.

This report documents the complete design of the electronics system for the AGLITE instrument from the conceptual layout of the instrument to the final fabrication. It is divided into two main portions. First, the high-level system design covers the scoping of the electronics system and the layout of the system architecture. It explains the major design decisions that were made before arriving at the implementation plan. The second portion of the report covers the detailed design of the electronics proceeding even to the circuit level where appropriate. It fully documents the critical details of the final system.

(122 pages)

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CHAPTER 1

INTRODUCTION

A. *Project Background and Relevance*

In recent years there has been growing public concern regarding the release of pollutants into the atmosphere from agricultural operations. Much of this concern is centered on organic gases such as ammonia and methane as well as microscopic particles in the range of 2.5 – 10 microns in diameter. These particles are also commonly referred to as PM2.5 and PM10 (PM for 'particulate matter'). According to the Environmental Protection Agency, PM2.5 and PM10 contribute to a number of respiratory illnesses and are the major cause of reduced visibility conditions (haze) seen in many parts of the country. The organic gases are responsible for contributing to the greenhouse effect, acidification, ozone production, and other general environmental concerns. Many types of agricultural facilities generate large amounts of these emissions. These include poultry houses, cattle feed lots, plowing operations, etc. Given the environmental and health concerns, the government has a growing interest in monitoring and regulating emissions as well as developing methods to mitigate their release.

The measurement of the total emissions of gases and particles from an agricultural operation is a technically difficult task. This is because there is no practical way to collect a representative sample of the emissions at a single measurement point. The gases and particulates escape in all directions over an area that may cover many acres. Existing methods of measuring these emissions have relied heavily on the use of samplers located at a few locations around the emission source whose readings are then extrapolated to

estimate the total flux of emissions. Unfortunately, these techniques are fraught with inaccuracies and difficulty of operation along with the inability to make real-time measurements while on-site. Without a good method for measuring emissions it is extremely difficult to implement regulatory measures on the operations. Also, it is difficult to determine if experimental mitigation efforts are having the desired effect. For this reason, the Agricultural Research Service (ARS) has sponsored a project to develop instrumentation with the ability to measure the total flux of various gases and particulates accurately and in real-time. The Space Dynamics Laboratory (SDL), part of the Utah State University Research Foundation, won the contract to design this experimental system and it became known as the AGLITE-LIDAR. The name AGLITE is an acronym for AGriculture LIght TEchnology and represents a series of instruments that will be built as part of this project, of which this lidar is the first. Through the remainder of this report, however, the lidar instrument will simply be referred to as AGLITE.

B. *Scientific Basis of the Instrument*

The approach taken by SDL to perform total emission measurements relies on a technology known as lidar (LIght Detection And Ranging). Basically, a lidar system consists of two main optical components, a laser and a telescope. The laser is fired intermittently to send out short bursts of light at a particular wavelength. The telescope is coaligned with the laser to collect the laser light that is scattered back from objects in the laser path. With each pulse, precise electronics measure the time from when the light left the laser until it returns to the telescope. The length of time indicates the range to the object. For atmospheric lidar, the objects in the laser path are generally things such as

dust, water vapor, aerosols, etc. that are mostly transparent. This means that only a small portion of the laser beam will be scattered at any given point along its path allowing the rest to continue forward to be scattered by other objects. In this manner, a profile can be formed showing the lidar return over a range of distances along the laser path. Also, by analyzing the returned light and making certain assumptions about the measurement environment, information can be inferred about the objects in the laser path such as their composition and size.

The amount of light that is scattered back and received in the telescope depends on the particle concentration and the backscatter coefficient. The particle concentration is a simple idea; however, the backscatter coefficient is comprised of many different things. This coefficient depends on the wavelength of the laser light, the properties of the particles such as their composition and size distribution, and also the environmental conditions such as the ambient humidity. The theoretical basis that drives the science of this instrument is that by analyzing the scattered light received at the detector, the equations can be worked backwards to arrive at the initial information such as the particle size or the composition. To make this backwards extrapolation possible, some reasonable assumptions must be made about the environment and the particles. Ultimately, it is also necessary to take measurements with several different wavelengths of light so that the information can be compared to arrive at a solution for the desired unknown.

Given the broad descriptions of the purpose of the instrument, several essential components of the lidar become immediately clear. First, there must be a laser that produces several different wavelengths of light. There must also be a telescope and detectors to receive the scattered light. The signals on the detectors must be processed

and then the data must be logged for further analysis. A directional mirror must also be included to scan the beam of the lidar in the desired directions. Finally, all of this must be coordinated with some sort of control system. These basic components are shown pictorially in fig. 1.1. This conceptual diagram was the beginning point for the design of the AGLITE instrument.

C. *Role of the Electronics System*

The AGLITE electronics system has the task of coordinating all the functions of the lidar. It controls the firing of the laser and synchronizes this with the data collection

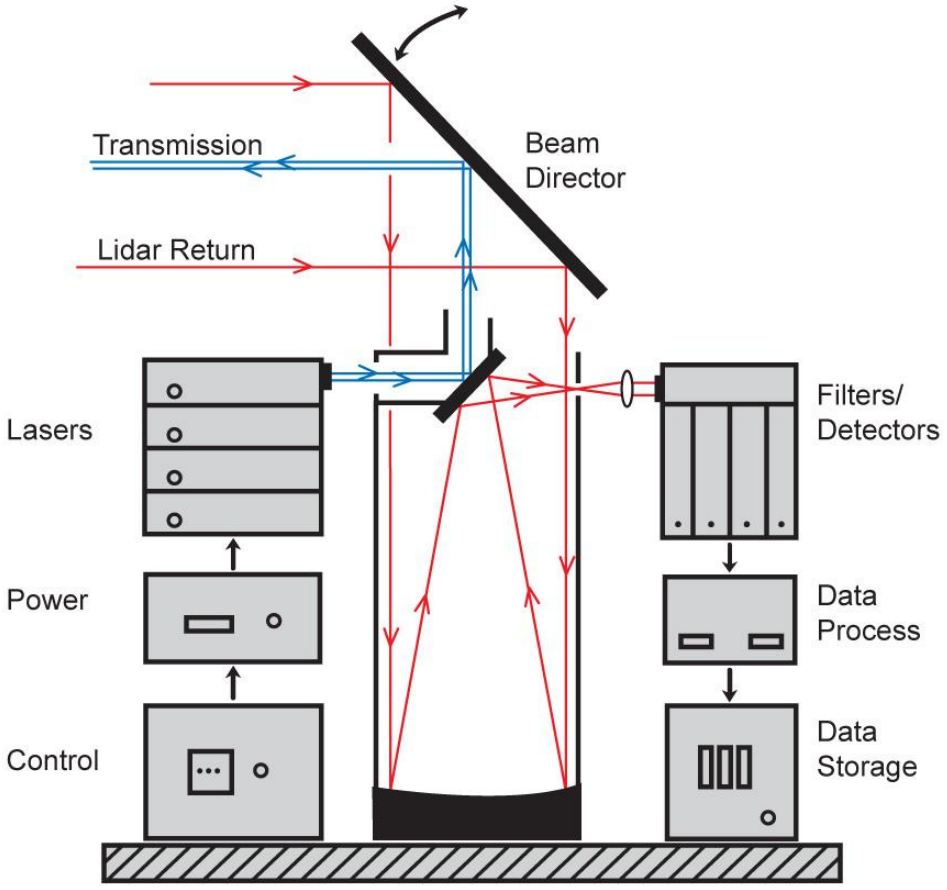

Fig. 1.1: Lidar conceptual drawing.

systems. Once collected, the data is averaged and reduced before it is stored and made available to the operator for further analysis. The electronics system also controls the beam director to perform the scanning operation. There are many smaller components in the system as well such as the light detectors, a digital camera, and sensors to internally monitor the instrument. The total electronics package integrates all of these components and establishes semi-automated computer control over them. The operator interface occurs at the computer terminal and once the system is configured it runs without the need for further user intervention.

D. *Chapter Overview*

The remainder of this report is broken into three main chapters covering the design of the electronics system for the AGLITE instrument. In addition, there are references and appendices listed at then end of the report.

Chapter 2 deals with the system level electronics design. First, this describes the general requirements that were the impetus for many of the system design decisions. Secondly, this chapter covers the overall operational scheme that was developed and establishes the organizational hierarchy of the various electronic components. Finally, a description of the instrument itself is given. This includes an overview of the functionality of each of the components that comprise the instrument as well as their interactions and interconnections with one another.

Chapter 3 covers the work that was done in the detailed design of the electronics hardware. For components that were requisitioned from outside sources, a description of their relevant specifications is given as well as the reasoning that governed any

significant selection decisions. For components that were custom designed for this project, a detailed description is given that explains their operation to a circuit level. The final portion of this chapter covers the layout and fabrication of the custom electronics as well as the physical arrangement of the entire electronics system.

Chapter 4 presents the conclusions of this project. This explains the future development possibilities for this project. It also describes the successes and the items that could be improved for future work.

CHAPTER 2

SYSTEM LEVEL DESIGN

The first major task in designing this lidar system was to complete a thorough system level design which would account for all of the major components that were to be included in the system. At the outset of this project, the only things that had been determined were the overall goals and a very conceptual picture of how the instrument might function. This concept is depicted in fig. 1.1. Very little consideration had yet been given to the electronics system of the instrument. This, therefore, became the first task to be undertaken.

The system level electronics design required a good deal of collaboration with others on the team who were responsible for the scientific goals of the project as well as those engineers working on the mechanical and optical design. Also, lengthy research was required into commercially available components that could be integrated directly into the design. The system level design involved the scoping of system requirements, laying out the operational scheme and information flow in the system, and establishing the components and subsystems that were to be included. The system components were also subdivided into primary components that would be included in the initial prototype fabrication and secondary components that would be future add-ons to the prototype. Finally, while this design project focused on the electronics, it was also necessary to consider the mechanical implications as well. This was particularly true in planning the layout of the enclosures and the PCB for the custom electronics so that mechanical limitations were accounted for.

One overriding theme that was considered continuously during the system design was the scalability of the instrument. The initial goals of the project focused on the development of an instrument that provided proof-of-concept and usable data with as few components as necessary. However, in the long-term plans for the project, it was projected that additional laser colors might be added with corresponding detectors. Also, different methods of collecting and analyzing data were proposed that would require additional sensors and hardware. For these reasons, it was desired that the system be designed to handle these additions without the need for any major redesign of the existing hardware.

A. *General System Requirements*

The initial statement of the goals of the AGLITE project made clear some of the major components that were to be included in its design. These were the first items considered in developing a system design. These items included a three-color laser, detectors for these wavelengths, a data collection system, and actuators to steer the lidar scan direction. As these components were explored and understood, and as the scientists continued their simulations, more precise specifications were determined. Also, it became clear that there were additional components that were either required or desirable in the system. The result of this early analysis was the list of components shown in table 2.1 that were to be included in the lidar system.

As the development of the project continued, some of these components were determined to be niceties that were not absolutely required in the initial prototype instrument. It was decided that these would be included in a second phase of possible

TABLE 2.1

INITIAL REQUIRED SYSTEM COMPONENTS

Component	Description
3-color Laser	NdYAG laser operating at the wavelengths 1064, 532, and 355 nm
Detectors	Photon detectors that could operate at the given wavelengths
Beam Steering	Actuators that could manipulate a mirror to scan the laser beam and receiving telescope beam in azimuth and elevation
Photon Counting Data Acquisition	A data system that could implement a photon counting approach to detect extremely low return signals
Analog Digitizer Data Acquisition	A parallel data system that could perform traditional digitizing of analog signals for moderate to high return signals
Digital Camera	A camera to follow the field of view of the lidar and capture digital imagery of the downrange scene
Thermal Control	Sensors as well as fans and heaters to control system temperature
Laser Energy Sensors	Sensors to monitor the outgoing laser energy continually during normal system operation
Remote Alignment	Motorized actuators used to align the laser and telescope without manual adjustment
Synchronizer	Electronics to synchronize the laser firing with the data acquisition systems and the detector gates.

additions to the system. However, to avoid the necessity of a total redesign of the electronics to accommodate the additional components, these phase-two additions were thoroughly investigated in the system design. In this way, when the components are added, they can simply ‘plug in’ to a place already prepared for that purpose. That is the ideal picture. In reality, some minor hardware modifications or additions may be necessary but these are fairly simple to implement. They might be things like adding signal conditioning for an additional analog input or adjusting the programming in the synchronizer’s FPGA (field-programmable gate array). By including this future planning in the system design, major modifications can be avoided.

B *Operational Description*

Once the general list of desired components was compiled, the next step was to proceed with the arrangement and layout of the overall system. Based on experience with previous lidar projects, two major considerations drove the system operational layout. First, it was desired that the lidar instrument could be operated remotely by computer after it was initially set up. This was so that while the lidar was running outdoors in a field campaign out of the back of a trailer, the operators could be located separately but nearby in more comfortable accommodations. Secondly, it was very attractive that the computer used to remotely operate the system be hardware independent of the lidar. This meant that any desktop PC or laptop computer installed with the proper software could control the lidar system over a standard communication interface. This was to avoid an overabundance of dedicated hardware and also, since the remote computer would likely be running the data processing algorithms as well as other software, it would allow the unlimited upgrade of the remote computer without interfering with the lidar electronics.

Given the two driving design considerations, the operational layout shown in fig.

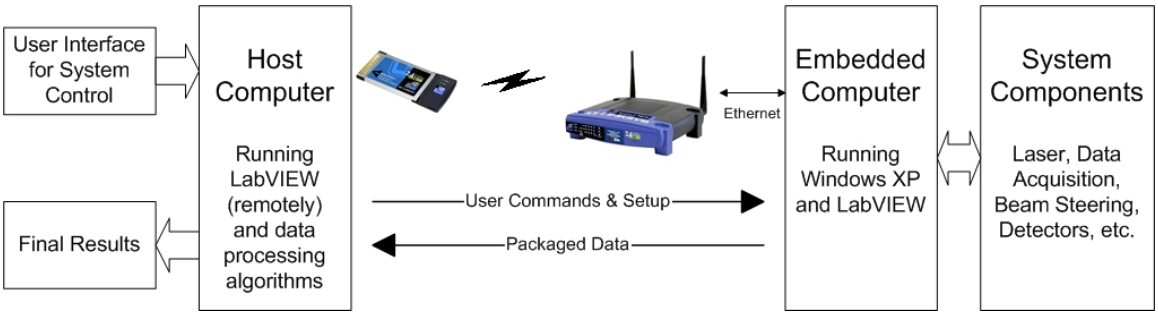

Fig. 2.1: Operations layout.

2.1 was developed. As seen in the figure, the system is comprised of two computers known as the host computer (left) and the embedded computer (right) which communicate with one another over a standard wireless LAN. The embedded computer controls all the lidar instrument components, and the host computer is both the interface for user control and the location where data processing occurs. A more detailed description of the components follows.

1) *Host Computer Role*: The host computer is the PC or laptop from which the operator controls the system and processes incoming data. During normal field operations this computer may be located in an RV or a building near to where the instrument is set up. This computer does not have any specialized hardware requirements other than a wireless networking card installed in the machine and sufficient storage space to accommodate the incoming data. Due to the network-based communications architecture, it has also been considered that in future developments of the project, additional computers dedicated to processing incoming data may be added on the user side. The need for this will be determined by the scientists developing the data reduction algorithms.

Concerning software, the host computer will simply be running Microsoft Windows XP as an operating system. To control the lidar, LabVIEW has been chosen for quick development time and easy creation of a user interface. The core LabVIEW routine runs on the embedded machine but a very convenient feature in LabVIEW allows the host computer to remotely interface to this core routine over the LAN. The only other required software for the host computer is the chosen software package for doing data analysis. It is most likely that the data processing algorithms will run in MATLAB

initially. In the future, a stand-alone application implemented in C++ may be developed that will integrate system control and data analysis in a single software package. Overall, this end of the total AGLITE electronics system is intentionally made very simple to allow an easy and standardized method of interacting with the rest of the instrument.

2) *Communication Link*: The communication between the host computer and the embedded computer takes place over a wireless LAN using commercially available hardware (i.e. wireless routers and wireless network cards) for creating this link. The embedded computer is hardwired to the wireless router which is located in the trailer with the rest of the instrumentation. The host computer communicates with the router wirelessly using the standard 802.11g protocol. As mentioned above, LabVIEW contains an operation mode that allows a remotely located computer to interface to another machine that is directly connected to the instrument. The host computer emulates local control, meaning that the actual LabVIEW program is running on the embedded computer but the GUI appears instead at the host computer terminal. All user input such as keystrokes and mouse clicks that take place on the host computer are treated as if they occurred directly on the embedded computer. This same LabVIEW function also accommodates data transfer between the two machines so that the data being generated by the instrument can be delivered to the host computer in near real-time.

3) *Embedded Computer Role*: The embedded computer carries the load for the low-level operation of the AGLITE instrument. This computer is tasked with providing direct control to the numerous components in the instrument. It configures all of the hardware components based on user input prior to beginning the lidar scans. Once the scan begins, it then collects and condenses data from the data acquisition systems, the

digital camera, and a small amount of housekeeping data. This is packaged and transmitted to the host computer over the LAN. The potential need was foreseen for a large amount of pre-processing to be performed on the raw data before being transmitted over the LAN to the host computer. This dictated that the embedded computer should have a great deal of processing power, something on the order of a fast Intel Pentium IV processor with at least 1GB of RAM.

In the process of the system design, a number of vastly different choices were considered for the embedded computer. Early on, when the list of components that were to be included was small and the need for processing power was minimal, the PC/104 and PC/104-plus form factors were considered the best option. These were attractive due to their very small size and the possibility of writing very basic software to run them. As the design progressed, however, it was found that the number and variety of interfaces to the components exceeded what was readily available in a PC/104 architecture. The shift was then made to single-board computers (SBC's) that provided much more advanced I/O options while maintaining a fairly small form-factor. The complexity of these computers, however, suggested the need for a more advanced operating system that could easily support the I/O interfaces that were to be used. Finally, the need for expandability and raw processing power led to the decision to use a full blown Pentium IV PC. This was attractive also because it allowed more standardized and readily available components that were familiar to the software engineers. A very significant price was paid, however, in the total system size and mass. This was very undesirable to the project managers but was determined to be unavoidable given other constraints on the project.

The embedded computer that was selected is an industrial grade computer very

similar in form and function to a powerful desktop computer. It has all of the standard interfaces one would expect on a PC including USB ports, serial ports, Ethernet, PS/2, etc. PCI cards are utilized to expand its capability to the non-standard functions it must perform. These additional functions are digital I/O, analog-to-digital conversion, and the addition of many more serial ports for component control. Its enclosure is industrialized with powerful cooling, air filtering, and vibration protection. The software for the embedded computer is explained later in this report.

4) *Instrument Description*: The AGLITE instrument consists of the components listed in table 2.1. These include the lasers, detectors, data acquisition systems, etc. that lie at the heart of the instrument. The research conducted in the early stages of this design showed that many of these components could be purchased as commercially available modules designed to interface directly to a computer over various standard interfaces such as RS-232 and USB. The other components, particularly those that had to be custom designed, could be communicated with using more basic interfaces, i.e. digital I/O and analog-to-digital channels. The total instrument, then, is a marriage of a myriad of different components that must be made to work together. This marriage occurs in the software as well as the custom designed hardware that links many of the components. A thorough description of the system level design and selection of these components is given later in this chapter.

5) *Operating System and Software Planning*: Determining the operating system that would be used in this project was a very significant decision that was considered in great detail. The initial investigation into the proposed components showed that most were designed to interface directly to a desktop style computer over standard interfaces.

Also, they were supplied with drivers for the most common operating systems such as Windows NT/2000/XP, Linux, and VxWorks. There were several things considered in making this selection. These considerations were the need for a real-time operating system (RTOS), the development time, and the implementation cost.

The first factor to consider in choosing an operating system was whether the need existed for real-time capability to provide service to the components. The systems that had the most time critical operation were the synchronization of the laser firing with the triggering of the data acquisition and the retrieval of the data from the data acquisition systems. The timing involved in the synchronization of the laser and data acquisition is necessarily very precise. It was desired to keep the timing ambiguity to the order of tens of nanoseconds so that the unknown time bias would be shorter than the best resolution of the lidar. If the synchronization was left to the computer to execute, this level of timing reliability could not be assured, possibly even with an RTOS. Therefore, the synchronizer was implemented in independent hardware so as to eliminate the need for fast servicing from the computer. The other possible time critical operation was the retrieval of data from the data acquisition hardware. However, after analyzing the hardware capability as well as the operational scheme, it was determined that the internal memory buffers on the hardware were sufficient to eliminate the need for real-time software support to retrieve and store the data. This is discussed in greater detail in the data rate analysis portion of the report.

Based on this analysis, it was determined that a real-time operating system was not needed. For this reason, VxWorks as well as other RTOS's were eliminated as possible choices for the OS since these were both expensive and required a great deal of

extra development time and cost. The remaining choices were Windows and Linux. While Linux was very inexpensive, and arguably a more efficient OS, the hardware components that were planned for use were much better supported for a Windows environment making the software development prospect much more attractive for a Windows based system.

The decision to use Windows XP was marred by only one major blemish – it is well known that this operating system has an exceptionally large footprint, meaning that it consumes a great deal of hard drive space and system memory to run. A solution was sought to decrease this footprint as much as possible, mainly due to concern over latency caused by unnecessary processes. The solution that was found was a product produced by Microsoft called Windows XP Embedded. This operating system is identical to Windows XP Professional except that every service routine, driver, application, etc. that is included in the Professional package is hand selectable and configurable in the Embedded version. This allows the developer to trim all the 'fat' out of the operating system and streamline its performance. A license and developer tools were purchased for Windows XP Embedded but due to development time considerations this was shelved until the initial phase of instrument construction and integration is complete. In the meantime, Windows XP Professional is being used with all of the non-essential background service routines disabled.

The final element in the software system design is the application software. This consists of the user interface, the data transfer protocol, and the local control software for the instrument components. As mentioned previously, this is being accomplished using LabVIEW which has built-in capability for all of these aspects of the software. In the

interest of a short development time, this is was the application of choice; however, in future development of the project, it is likely that a stand-alone application will be developed. This will likely coincide with the implementation of the Windows XP Embedded operating system. The combination of these future software improvements will have tremendous effects in improving the software responsiveness and lowering the system resource overhead. These performance improvements are not presently critical in the first phase of prototype construction but will become so with the addition of an analog data acquisition system in the second phase.

C. *Instrument Electronics Overview*

Beyond the computers and software, the AGLITE instrument is comprised of a myriad of components that are orchestrated to perform the scientific mission of the project. Electronically, these are all organized under the embedded computer which dictates the system functions. These components interface to the computer through a variety of standard means such as RS-232, USB 2.0, PCI, digital I/O, and analog-to-digital conversion. Figure 2.2 shows the top-level interaction of all of these components both to the computer and to one another. The diagram shows the host computer and the embedded computer as well as the connection between them on the left with the remainder of the components on the right. The components that are outlined with a dashed line are planned as possible future add-ons to the system and are not included in the initial prototype. They are included here, however, since they played a role in specifying the scalability needed in the overall system. Each of the components will be described here generally along with their relevance to the total system functionality.

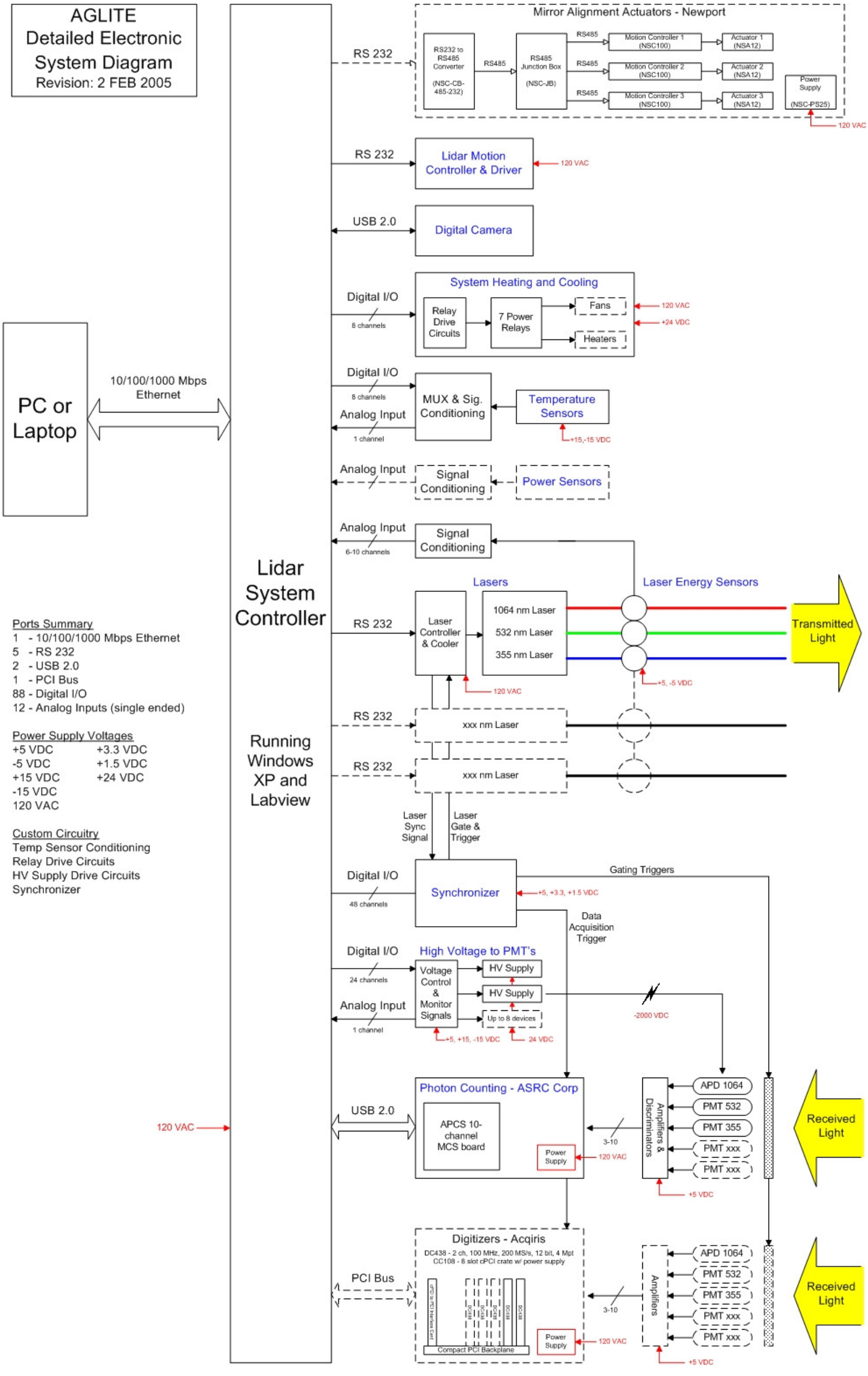

Fig. 2.2: Electronics system functional diagram.

1) *Initial Phase Components:*

a) *Motion controller and driver*: The motion controller and driver is a self-contained module that is responsible for directing the beam of the lidar in its scan pattern. The ability to scan the lidar is essential to performing the science mission. The lidar is designed optically as a coaxial system. This means that the laser exits the system exactly in the center of the telescope so that the field of view (FOV) of the telescope is directly overlapped with the laser beam. One of the major reasons for choosing this optical configuration was to allow easy steering of the beam in azimuth as well as elevation. Selection of the motors and the drivers was the responsibility of the mechanical designers. Since the controller was sold along with the actuators, it was not necessary to interface directly to the stepper motors. Instead, an RS-232 serial port provides the communication link between the embedded computer and the motion controller. Manipulating the device is as simple is giving a software command to move to a specific angle at a certain speed.

b) *Digital camera*: The purpose of the digital camera is both scientific and logistical. The scientific purpose is to capture high resolution images of the downrange view where the laser is firing so that visual data can be used to if necessary verify and correlate the lidar return data. Logistically, it is used as a safety precaution so that the operator can be aware of potential risks related to people or animals entering the beam path. The camera is mounted parallel to the telescope and its view is reflected off of the same steering mirror used for the main beam so that its view will follow that of the lidar. The applications intended for this camera required that it have very good resolution, but a high frame rate was not necessary. This would suggest something very similar to a

handheld digital camera in performance that could be easily automated over a standard interface and was built for OEM (original equipment manufacturer) applications. To fill this need, USB-based cameras were found to be the best fit. These are controlled via a USB 2.0 interface and the captured image is transferred over the same interface back to the computer. After retrieving the image, the computer performs a standard JPEG image compression before sending it on to the host computer.

c) *System heating and cooling*: The operation of the AGLITE instrument is anticipated to take place in a variety of environments ranging from cold Cache Valley winters to hot Texas summers. For this reason, the ability to provide a certain level of thermal control was desired. This control is provided electronically using relays to power fans and heaters in the system. The relays are controlled using digital I/O that is connected to a drive circuit that powers the relay coils. The device side of the relays is capable of switching both AC and DC voltages at up to 15 amps. The wiring of this side of the relays is left open so that appropriate power for the individual devices can be applied. Currently, there are no heaters or fans included in the mechanical layout of system. This feature is included as a precautionary option that will be utilized as the need arises. Also, it may be used for other unforeseen devices that require basic power control.

d) *Temperature sensors*: The temperature sensors included in the instrument provide basic housekeeping data and are not directly involved in the science data collection. These sensors are positioned on the various temperature critical devices in the instrument to allow the operator to monitor for any adverse conditions. There are several components included in the lidar system that are highly temperature sensitive. Most of

the electronics are designed to be environmentally robust, but the more delicate components, such as the laser and the detectors, must be maintained within a much smaller temperature range. Also, the optical bench must be monitored to assure an approximately uniform temperature so that metal expansion does not bend any of the optical paths. Since the function of the sensors is diagnostic, it is not necessary to have an extremely high level of accuracy in the measurement. Errors within 1-2 degrees Celsius are acceptable. Also, since temperature variations are expected to occur very slowly, the measurements need not have a high time resolution. Sampling each sensor several times per minute is adequate. Based on these requirements, it was chosen to multiplex the temperature sensors through an analog multiplexer to minimize the number of channels needed on the ADC card. The circuit therefore is controlled using digital I/O to select the active sensor, and the signal is then routed through a single channel on the ADC card.

e) *Laser*: The laser was selected and ordered in the very earliest stages of the project while the rest of the design was still being conceptualized. This was due to the very long lead time required for its construction. For this reason, it was treated as a pre-determined item as far as the electronic system was concerned. The laser emits three wavelengths, 1064, 532, and 355 nm, simultaneously from a single aperture and can operate at pulse frequencies between 5-15 kHz. The laser consists of three components – the laser head that is placed in the instrument, the laser controller that is mounted in the electronics rack, and the cooler which is positioned (when needed) next to the instrument. The controller is the only component that interfaces directly to the other electronics and it is communicated with via an RS-232 serial port. This controller then assumes all control

of both the laser head and the cooler. All setup and configuration commands are transmitted over the serial port but separate synchronization signals are also provided. These signals enter the controller through three BNC connections for an external frequency trigger, an external gate, and for the sync output pulse. These are all connected to the synchronizer module and are explained in greater detail in that section.

f) *Laser energy sensors*: In order to accomplish the scientific goals of the project, it was necessary to know precisely the power being output by the laser at all times during operation. One of the main concerns was that the laser output power would slowly drift over the course of hours of operation. Also, the measurable quantities could not be exactly specified without knowing precisely the baseline energy transmitted into the environment by the laser. To achieve this measurement, a portion of the outgoing laser beam is diverted using a 3% fused silica reflector. This diverted beam is then passed through a system of dichroic reflectors that separate the three wavelengths from one another with a minimal energy loss. Each of the beams then strikes a laser energy sensor designed for the specific wavelength. These sensors are thermal devices that respond to the incident energy on the detector surface by a corresponding change in temperature. Internally, the sensors perform corrections for the ambient temperature and then condition their output signal as an analog voltage that is passed to ADC card in the embedded computer. Essentially, the only additional circuitry needed is the proper power and ground connections. Also, once full scale integration is underway, these sensors will have to be carefully calibrated so that the actual laser output can be determined from the measured diverted beam.

g) *Photon counting data acquisition*: The initial fabrication of the instrument

includes only a single data acquisition approach that is based on the concept of photon counting. This method is used for very low-level light where the individual photons striking the detector surface can be distinguished from one another and counted. According to the time that they strike, the range from which they are returning can be determined. Since this is probabilistic process, the laser is pulsed many times and the returned counts are summed together to provide a time-integrated total return. The nature of this counting process requires very fast specialized hardware to perform it accurately and efficiently. Also, the hardware was required to be able to accomplish this for many detector channels simultaneously. This type of hardware is commonly referred to as a multi-channel scalar (MCS) device. For this application, a product was chosen from an external contractor that specializes in MCS hardware. The photon-counting board can simultaneously count signals from ten separate detectors, perform internal pulse integration, and transfer the final data to the computer over a USB 2.0 connection. The configuration of the MCS parameters such as range bin size, number of range bins, number of integration cycles, etc. is performed prior to operation over the same USB connection. The data acquisition is triggered by a signal from the synchronizer that is transmitted over a coaxial cable.

h) *Synchronizer*: The synchronizer is a custom built circuit that having the task of timing the laser pulses with the data acquisition and the gating of the detectors. The synchronizer itself consists of a fast FPGA that works with an accurate crystal to measure time by counting clock ticks.

One aspect of making lidar measurements is that after collecting the light return from a number of laser pulses, a background measurement must be taken by running the

data acquisition system as normal but without the laser firing. This provides a measurement of the portion of the total return signal that is comprised of the ambient light and is not from the laser. With this in mind, the laser is set simply to run a predetermined frequency unless it is inhibited by the gate signal. The first task, then, of the synchronizer is to control when the laser fires using the external gate on the laser controller.

When the laser fires it first sends out a 'sync' signal which indicates that laser will fire in approximately 1-2 μs. The exact delay time is not specified until the laser is delivered and this value has been found experimentally. This delay must be taken into account for the purpose of triggering the data acquisition system so that it begins taking data precisely when the laser fires. Based on this, the second task of the synchronizer is to provide this delay by counting the appropriate time from receiving the sync signal before it provides a trigger signal to the data acquisition.

As mentioned previously, the laser is inhibited at regular intervals during data acquisition to allow for the collection of background measurements. Since the laser is inhibited, it does not produce the regular sync signal that is delayed and then used to trigger the data acquisition. Therefore, this trigger signal must be artificially generated by the synchronizer during background collection without the sync signal input. This is the third task of the synchronizer.

Finally, as the laser pulse exits the instrument, the near-field return can be orders of magnitude larger than the return at the range of interest. Since the detectors are tuned to detect signals at this far-field range, the initial signal is sometimes sufficiently large to either saturate or possibly damage the detector. In these cases, an electronic gate is often

used to inhibit the input signal during the near-field range but will allow it to turn back on quickly enough that it can begin collecting the return signal once the laser pulse is sufficiently downrange. The fourth task of the synchronizer is provide these gate signals after some specified delay from the time of the laser firing.

The synchronizer interfaces to the embedded computer through 48 channels of digital I/O. Prior to beginning operation, the user-specified delays as well as the desired background time and other parameters are loaded into the FPGA and stored. From this point on the FPGA operates asynchronously from the computer based on the signals received from the other components.

i) *Detectors*: To collect the light return from the scattering of the laser requires the use of extremely sensitive detectors optimized for detecting photons at the wavelengths being used in the system. The wavelengths are 1064 nm in the IR spectral range, 532 nm which appears green in the visible spectrum, and 355 nm in the UV range. There are two types of detectors used for this type of application – photo-multiplier tubes (PMT's) and avalanche photodiodes (APD's). PMT's are vacuum tubes consisting of a cathode and anode with usually about ten dynode stages in between. A photosensitive material on the cathode emits electrons when struck by a photon. A potential difference between the dynode stages causes those released electrons to accelerate into the next dynode causing a cascade of more electrons until the electrons finally reach the anode and have gained enough electrons to form an appreciable current. PMT's generally require an applied voltage in the range 1-3 kV to operate. APD's are special photodiodes that when struck by individual photons cause a massive release of electrons proportional to the number of incident photons. Another more specialized type of APD is a Geiger

mode APD that is optimized for the detection of single photons incident on the detector.

For this system, PMT's were chosen as the detectors for the UV and visible beams based on their intrinsically high efficiencies at those wavelengths. Unfortunately, PMT's are a very poor choice for the IR and with a few exceptions they have no detection ability at those wavelengths. APD's on the other hand, while not optimal in the IR range, are at least capable of detection at those wavelengths. For this reason an APD was chosen for the IR detector.

All of these detectors are designed to detect single-photon events and produce a single output pulse corresponding to this photon. Since this is an isolated pulse, it can be discriminated into a digital pulse for easy transmission to the photon counting hardware. The discriminated pulses are TTL compatible signals. Cleary, since the pulses are not infinitesimal in duration, there is a physical limitation to the maximum attainable count rate. For PMT's that are optimized for photon counting, each single-photon event must be separated by a time on the order of 20ns. For APD's this time increases to at least 70ns. If this rate is exceeded, then the detector becomes saturated, meaning that all of the photon events bleed together and appear as a single output pulse.

j) *High voltage supplies and control*: As mentioned in the description of PMT's in the detector section, they require a very large voltage to be applied to achieve their desired gain. The voltage required for most PMT's is between 1-3 kV and by varying the voltage, the gain of the PMT can be controlled. There are several manufacturers of controllable high voltage power supplies that work well with PMT's. The power supplies accept a control voltage to electronically control the output voltage applied to the tube. To facilitate this control, custom circuitry had to be included. This circuitry consists of

digital-to-analog converters with buffered outputs that are controlled by digital I/O from the embedded computer. Also, monitor signals are provided from the high voltage supplies that indicate the output voltage and the output current from the supply. The monitor signals are multiplexed and fed back into the ADC card in the computer on a single analog channel.

2) *Future Add-on Components:*

a) *Computer controlled alignment*: One important operational aspect of any lidar system is the alignment of the laser and the telescope. This alignment usually has to be conducted at the beginning of every data collection campaign since it can shift during transport or after servicing internal components. Alignment is performed by adjusting finely threaded thumb screws on the optical mounts of the final mirrors that direct the outgoing laser beam. In order to allow remote alignment and also make reproducible adjustments easier, a motorized set of adjustment screws was considered for the alignment system that would replace the thumb screws. These are made by several different companies but the most attractive ones were made by Newport. Each actuator has a small controller module that is connected via RS-485 to a junction box. The RS-485 box is then converted to RS-232 to interface to a standard serial port. These were selected as the best option because they were compact in size, were very simple to communicate with, and were less expensive that some of the alternatives found. Sufficient RS-232 ports were included in the embedded computer in so that motorized controls could be added to the design in the future.

b) *Additional laser wavelengths*: One of the possibilities for the long-term development of this instrument is the addition of other lasers to provide a wider variety of

wavelengths. Two additional laser wavelengths have been suggested as possible add-ons. Based on the existing laser, it was assumed that any other lasers would require essentially the same interconnects to be able to interface to the rest of the system. For this reason, extra RS-232 ports were included for this possibility. Also, there are extra analog inputs available on the ADC card to process the signal from additional laser energy sensors. Finally, the synchronizer was also provided with expandability to allow the control of additional lasers, data acquisition systems, and detector gates. The FPGA programming would have to be altered but no hardware changes would have to be made since there are extra available connectors to the FPGA already built-in.

c) *Analog data system*: The analog data system is another traditional method used in lidar for detecting larger light returns than those dealt with in the photon counting method. It was described previously that when individual photons strike a detector, they cause a single distinguishable pulse that can be counted using an MCS unit. However, when many photons are striking a detector faster than they can be resolved individually in the output, the result is a continuous output current from the detector. The magnitude of this current relates to the number of photons striking the detector. By digitizing this output signal using high speed analog-to-digital conversion, similar data can be collected from this system as is collected from a photon counting system. The long-term intent is that such a system will be included in this instrument as a parallel data system to the photon counting system.

In order to perform a system level design as well as a data rate analysis, it was necessary to select a commercially available system that would be a good fit to the project so that it could be planned for. The system chosen is produced by Acqiris and is

an expandable system of digitizer cards. These cards interface to a Compact PCI backplane and are synchronized using inter-board connectors. The trigger originates from the synchronizer. The cards move their data to the cPCI backplane where is taken by an interface card and transferred over a cable to a PCI card placed in the embedded computer. In this fashion, the data from all the digitizer channels is transferred to a single PCI card in the computer. The digitizer model that best fit the requirements was the DC438. It is a 12-bit, 2-channel card with a 100 MHz input bandwidth, sample rates of 200 MS/s and 4 Mpoints of memory. This card would be able to provide the sampling resolution needed for the lidar system and was less expensive than other options.

d) *Additional detectors*: There exists a good possibility for the future addition of more detectors to this instrument. Currently, there are three detectors that are intended for the original three wavelengths. If an analog data system is later added to the system, it would require three new detectors for the same wavelengths that were better suited for analog signals. Also, if two additional wavelengths are added with new lasers, this would introduce four more detectors (two for the photon counting system and two for analog system). This totals ten detectors. The final possible addition could occur if it was desired to observe the different light polarizations. If this were implemented, then each of the ten existing detectors would have a twin that could detect the oppositely polarized light that was separated out by receiver optics.

Based on the possible detectors mentioned, it was assumed as a worst case scenario that there may be as many as ten detectors attached to each data acquisition system running simultaneously. This became a factor in choosing data systems that could handle such a load as well in the data rate analysis. Ultimately, the electronics were

designed such that handling a load such as this would be possible. It is important to note that allowing this extra capability in the electronics system did not add any significant costs or complexity to the project. The photon counting data system was already designed to handle ten channels and would have been the system of choice regardless of the number of channels that were intended for actual use. The analog data system is expandable by two channels at a time to fill the present need so this avoids purchasing superfluous hardware. Finally, to add the extra capability in the custom electronics required only a few minor additions with minimal cost and was primarily an issue of allowing room in the layout rather than adding expensive hardware.

3) *Data Rate Analysis*: There are three sources of data that were considered in the data rate analysis – the photon counting data system, the analog data system, and the digital camera. Data from the temperature sensors, energy sensors, high voltage monitors, etc. was considered negligible in comparison to the major sources and was thus excluded from the analysis. The purpose of the analysis was to assure that the volume of data being produced from a worst case scenario was within the limitations of the computer hardware and software to handle.

In calculating the data volume that would be produced, worst case assumptions about the operation parameters were made as shown in table 2.2. These assumptions were based on estimates given in discussions with the scientists on the project.

The photon counting data acquisition system provides functionality for integrating multiple pulses internally until the integration time is reached at which point it transfers the data through the USB port to the computer. This relieves a large portion of the load that would otherwise be placed on the computer and results in a fairly small data package

TABLE 2.2
OPERATION ASSUMPTIONS FOR DATA RATE ANALYSIS

Assumption	Value	Units
Repetition rate of the laser	10	kHz
Range bin size	15	meters
Number of range bins	1000	-
Integration time	0.5	seconds
Number of channels per data system	10	-

that must be transferred. The data rate for this system can be very simply found by the following formula:

```
rate = (# of range bins) * (2 bytes/bin) * (# of channels) / (integration time)
```

This results in approximately 40 Kbytes of data per second. Since the allowable data rate across a USB 2.0 connection is theoretically specified at 480 Mbps, there is absolutely no conceivable problem with accomplishing this data transfer.

The analog data system is not as nicely adapted to lidar applications as are MCS units because it lacks the ability to integrate successive pulses internally and the data from each pulse must be transferred over the PCI bus to the computer where it performs the integration. These calculations were made based on the Acqiris DC438 digitizers with 12-bit resolution. In this case the formula for calculating the rate becomes the following:

```
rate = (# of range bins) * (1.5 bytes/bin) * (repetition rate) * (# of channels)
```

Completing this calculation yields a data rate of about 150 Mbytes per second. Given

that the maximum data rate across the PCI bus is 100 MB/s, even if it were totally devoted to this data transfer it is clear that this rate is not supportable. This can be remedied imposing a few realistic limitations on the worst-case operation scheme. First, the number of channels is very unlikely to reach ten. For the current system comprised of three detectors, if all the other parameters were left unchanged then the volume of data would be only 45 MB/s. Also, the number of range bins is more likely to be 200-300 for the workable signal range of an analog system so this reduces the data rate by another factor of 3-5. Accounting for this range limitation yields data rates between 9 MB/s for three channels with 200 bins and 50 MB/s for ten channels with 300 bins. These data rates are much more manageable and a realistic estimate would say that the worst case that would actually ever be implemented in the system would be about 25 MB/s.

Once arriving at the embedded computer, the analog data would be summed up over the same time periods as was performed for the photon counting data which would reduce the data package to tens of Kbytes. More specifically, five channels operating with 300 bins would produce 25 MB/s of raw data that would reduce to about 6 KB/s of averaged data. The ability of the embedded computer to handle this data reduction in real-time was also considered. A sample program was contrived to simulate this data rate pouring into system memory as well as a routine to sum the data as it came in. It was performed on a machine far inferior to the embedded computer running Windows XP and it was able to keep up using only about 20% of the CPU power to accomplish it. Based on this it was projected that embedded computer would have no problem reducing the incoming data.

The final major data source is the digital camera capturing images at a rate of

about one per second. The camera is a 3.1 mega-pixel camera which means that a raw image would be about 10 MB assuming 24-bit color resolution. Using a compression ratio of 10:1 would yield a data rate of about 1 MB/s. Ironically, this becomes the largest data rate consumer by far compared to all of the other data sources.

The wireless link between the embedded computer and the host computer is another possible location of a data bottleneck. Based the analysis just described, the expected data rate across this connection could be about 1 MB/s. The theoretical data rate for an 802.11g wireless connection is 54 Mbps or 6.75 MB/s. This means that even if the wireless link were operating at only 15% of its rated capacity, it could still maintain the needed data rate. In conclusion, it was found that given the current design and operational scheme, there should be no bottlenecks in the data reduction and transfer to the host computer. A summary of the expected worst-case data rates is presented in table 2.3.

TABLE 2.3
DATA RATE SUMMARY

Data Source	Data Rate – Instrument to Embedded Computer	Data Rate – Embedded Computer to Host Computer
Photon Counting (10 channels, 1000 bins/channel, 0.5 second integration)	40 KB/s	40 KB/s
Digitizers (5 channels, 300 bins/channel, 0.5 second integration)	25 MB/s	6 KB/s
Digital Camera (3.1 Mpixel, 24-bit color, 1 image/second, 10:1 compression)	10 MB/s	1 MB/s
Instrument Monitors (Laser Energy Sensors, Temperature Sensors, etc.)	<1 KB/s	<1 KB/s

D. *Implementation Plan*

The system level design can be broken into two main categories for the continued design work, i.e. hardware and software. With the system architecture in place along with an overall plan for the software implementation, the detailed software design work was handed off to software designers to complete. What remained was the detailed design of the hardware. This included the final selection of components, the design of the necessary custom circuitry, and the physical configuration of the electronics. I assumed responsibility for the detailed hardware design and also continued to work with the software designers as needed to clarify the design plan and communicate relevant interactions between the hardware and the software. The remainder of this report covers the detailed design of the AGLITE instrument hardware.

CHAPTER 3

DETAILED ELECTRONICS DESIGN

A. *Requisitioned Hardware*

The design of the AGLITE system involved the use of many highly specialized components that require a great deal of expertise to design and manufacture. For this reason, as well as to expedite the overall project, most of these components were requisitioned from companies that specialize in those areas. There was, however, a great deal of work done to specify and select those components as well as to design and fabricate the custom electronics that would serve as the glue to bind all of these pieces together. The components that were requisitioned from outside sources were the laser, the beam steering hardware, the laser energy sensors, the computer electronics, the camera, the photon detectors, and the photon counting data system. A few of these, i.e. the laser, energy sensors, and beam steering, were selected by other engineers on the project so it was only left to design the interface to these components. The other requisitioned components are described here including significant design decisions that were made in the process of their selection.

1) *Embedded Computer*: Once the decision had been made in the system design to use a PC style computer as the embedded controller for the instrument, it was determined also that this should be a powerful machine that was physically robust. To fill these requirements, an industrial grade rackmount computer was selected from Advantech that was custom assembled to the specifications required by the project. While there is a wide variety of manufacturers of industrial PC's, Advantech was chosen

based on the capability and diversity of their product line as well as their reputation in the industry for producing reliable equipment that is well supported. Also, several PCI cards were needed to provide extra RS-232 serial ports, digital I/O, and digital-to-analog conversion. These were also purchased from Advantech.

The computer was selected for its processing power as well as for the availability of the necessary ports as described in the system design. The motherboard that was selected was the model AIMB-742. This is an Intel Pentium IV based board and it was selected to have a 3.2 GHz processor with an 800 MHz front-side bus. Combined with this was 2GB of DDR333 RAM. This combination of processor power and memory assured that the embedded computer would have ample capacity to reduce the incoming data streams. The other requirement was on the available ports. This board was equipped with gigabit Ethernet, five PCI slots, and eight USB 2.0 ports meeting all requirements except serial ports. The number of RS-232 serial ports was insufficient but this was supplemented with an RS-232 PCI card. This motherboard setup was placed in a model IPC-610MB industrial rackmount chassis. The chassis is designed with extra reinforcement and restraining clamps to protect the components from vibration. This chassis also features a powerful forced-air cooler with and a 300W power supply. The final component in the computer was a 120GB Western Digital hard drive. The specifications for the computer are summarized in table 3.1.

The embedded computer also includes three PCI cards to add special functionality for controlling the instrument. Additional RS-232 ports were added with an Advantech PCI-1620B-A card. This card contains eight independent serial ports (DB-9 style) that are treated just like the COM1 and COM2 ports on a standard PC. In fact these map as

TABLE 3.1
EMBEDDED COMPUTER SPECIFICATIONS

Specification	Value
Processor	Intel Pentium 4 (3.2 GHz)
Front Side Bus	800 MHz
PCI Bus	5 slots – 32-bit/33 MHz
ISA Bus	2 slots – 16-bit/8 MHz
RAM	2GB (4 dimms) DDR333 SDRAM
Ethernet	1 port – 10/100/1000Base-T (gigabit)
USB	8 ports – 2.0 compliant
Serial	2 ports – RS-232
Hard Drive	120GB

COM3-10 for communication purposes. These ports come off of the card in a single 62-pin connector and are split up into eight DB-9 connectors using an octopus-style cable.

The next PCI card in the embedded computer is for basic digital I/O ports. The card is from Advantech, model PCI-1753-A. This has 96 bits of digital I/O arranged in 12 8-bit ports. Each of these ports emulates the 8255 PPI chip operating in mode 0. Simply stated, this means that it is the most basic (and widely used) version of digital I/O that is ideal for controlling simple devices. The 96 channels come off of the card in a 100-pin SCSI connector.

The final card in the embedded computer provides analog-to-digital conversion (ADC) channels for reading the analog signals such as the laser energy sensors and the temperature sensors. The card for this is an Advantech PCI-1713-A. This contains 32 single-ended or 16 differential inputs which can be configured in combination. These can be sampled at up to 100 KS/s with 12-bit resolution. It also has a 4K sample FIFO buffer onboard. The connector for this card is a 37-pin D-connector.

2) *Laser*: The laser is one of the absolutely fundamental components in the

AGLITE instrument. The properties of the laser have been driving factors in many design decisions throughout the system. The laser that was purchased for this project is a customized version of the model DSC10-SLM multi-wavelength laser produced by Photonics Industries. This is an NdYAG laser that simultaneously emits the first, second, and third harmonics of a normal NdYAG based system. This equates to beams at the wavelengths 1064 nm (IR), 532 nm (green), and 355 nm (UV). All three of these beams are emitted simultaneously from a single aperture in the laser head and the laser is designed to operate at a repetition rate between 5 kHz and 15 kHz. The high repetition rate was selected to offer a significant reduction in the eye-safety range so that during measurement campaigns the standoff distance from the target could be minimized. A summary of the performance characteristics of the laser is given in table 3.2.

While all of the laser characteristics were significant in the optical design of the AGLITE instrument, the two characteristics that played the largest role in the electronics

TABLE 3.2
GENERAL LASER PROPERTIES

Property	Value
Wavelength	1064.2 nm (IR), 532.1 nm (Green), and 354.73 nm (UV)
Average Power	500 mW at 5-10 kHz (per wavelength)
Pulse Energy	50 μJ at 5-10 kHz (per wavelength)
Pulse Width	35 ns
Pulse Repetition Rate	5-15 kHz
Transverse Beam Mode	TEM_{00}
Spectral Bandwidth	SLM, 100 MHz (with seeder)
Beam Diameter	IR-1.0mm, Green-1.0mm, UV-0.9mm
Beam Divergence	IR-2.5mrad, Green-1.6mrad, UV-1.3mrad
Cooling Method	Air-cooled with optional water-cooler

design were the operating wavelengths and the repetition rate. The wavelengths played a major role in the selection of detectors and energy sensors as is discussed in later sections. The repetition rate affected these choices as well but also played a major role in the selection of the data acquisition hardware and was one factor in choosing the design scheme for the synchronizer. The role of these parameters is explained in greater detail in the corresponding sections of this report.

The other important features of the laser are its physical interconnections with the other electronics. The laser controller communicates with the embedded computer over an RS-232 connection. Through this port, the operating parameters of the laser are configured. This provides the same control as if the configuration were being performed directly using the front panel controls on the laser controller. The other interconnections are three BNC connections also located on the controller. The first two provide external control over the laser operation. The laser normally generates its own timing for pulsing the laser; however, the 'external frequency' input accepts a TTL trigger signal to fire the laser at an externally determined frequency. The other input is the 'external gate'. This is also TTL and is normally internally controlled. This allows the laser output to be electronically inhibited by disabling the Q-switch in the laser to prevent it from firing. The third connection is the 'sync' signal. This is produced by the laser controller to indicate the eminent firing of the laser pulse. The time delay (1-2 μs) between the rising edge of the sync signal and the actual emission of light is a known length of time and allows the simultaneous triggering of the other hardware such as the data acquisition and the detector gates.

3) *Laser Energy Sensors*: The laser energy sensors are intended to monitor the

energy or the average power of the outgoing laser beams. To accomplish this, a small portion of the beam (3%) is diverted just before it exits the instrument using a fused silica reflector. The diverted beam still contains all three wavelengths in a single beam so these are separated using a series of dichroic reflectors that are designed to reflect a small band of wavelengths while allowing the others to pass through. Once separated, the beams strike the three sensors that measure their power.

The sensors that were chosen for this instrument are produced by Molectron Detector, Inc. and sold through Coherent Inc. While I performed the initial investigation into the sensor selection, the final selection was made by the optical engineer. The sensors are model PS19Q and are a thermal style detector. Thermal sensors work by very accurately measuring the change in temperature caused by the incident laser light on the detector surface and comparing that with the temperature of an unexposed surface. After some internal signal processing, a measurement of the laser power is extracted. These detectors are unique due to their advanced thermal stabilization making them nearly impervious to both external and internal factors that could disrupt the thermal measurement. These sensors operate over a very wide spectral range; therefore, the same sensor type is used for all three wavelengths. The time response of these sensors is rather slow, on the order of one second, which means that only an average power can be determined over many laser pulses. However, given the projected integration times that will be required to collect a sufficient signal, this should not be a problem.

The detectors are designed to normally interface with an electronic meter that not only reads the analog data but also communicates with a small PROM (programmable read-only memory) in the sensor to extract basic information about the sensor head. The

sensor is therefore equipped with a 25-pin D-connector to plug into the meter. For our application, the use of a specialized meter for each sensor was impractical as well as expensive. The only required connections on the D-connector are the power and signal pins. The sensors requires a +5V, -5V, and GND power connection and produces an analog voltage signal that has a range between 0V and 10V. The ramifications of the power requirements can be seen in greater detail in the power design of the custom electronics. In short, these sensors require a +5V connection that is referenced to analog ground and not digital ground for the sake of the return signal integrity. For this reason, a separate voltage regulator is included to create a +5V line from the +15V supply that is referenced to AGND instead of using the main +5V generated directly from the power supply which is referenced to DGND. While this distinction seems small, the accuracy of the measurement is critical so the additional hardware was justified. Also, this eliminates a potential for a ground loop that could interfere with a number of components.

4) *Beam Steering*: The beam steering mechanism is another critical component in the AGLITE instrument given the operation scenario in which the instrument will be employed. The purpose of the instrument is to scan in vertical planes surrounding an agricultural operation. This requires both azimuth and elevation control that is highly accurate and repeatable as well as being mechanically robust to move the mass of the pointing mirror. The selection of this hardware was conducted entirely by the engineers responsible for the mechanical and optical design of the instrument. The hardware selected is produced by Newport and includes two different motorized platforms and a single driver that controls and powers both simultaneously. The rotational stage is model RV350PP and has a 350mm center opening through which the main beam of the

telescope and laser passes. The elevation stage is model BGM120PE. Both of these actuators are manipulated by a model ESP300 universal controller/driver. This driver is the only interface to the rest of the electronics system and communicates over a standard RS-232 serial port. A fairly simple instruction set allows full control over the position, velocity, and acceleration of the actuators and allows the user easy control over the scanning parameters of the lidar.

5) *Digital Camera*: The digital camera is included in the design of the AGLITE instrument as a safety measure, a diagnostics tool, and potentially a data acquisition tool. The primary purpose is to provide the operator of the lidar system with a close-up view of the downrange scene. This allows the visual detection of potential hazards, such as a person or animal passing in front of the laser beam, and also ensures that the beam is not striking any stationary object. Another purpose for the camera is to provide a basic diagnostics tool for the alignment of the laser since at least one of the beams is in the visual spectrum. The third potential purpose of the camera is to collect imagery of cloud motion that can be processed to extract the 2-D velocity vectors of the clouds and contribute to the science data collection. The camera mounts on top of the instrument and is positioned parallel to the outgoing laser so that its FOV is also directed by the beam steering mirror and it can thus follow the laser beam.

Given the applications that are planned for the camera, high quality color resolution was very important but achieving high frame rates was not critical. Also, a camera was wanted that could interface easily to a computer without cumbersome PCI cards or hardware dependant connections. For these reasons, a scientific grade USB camera was chosen. The selection of companies that manufacture this type of camera is

TABLE 3.3
USB CAMERA SPECIFICATIONS

Specification	Value
Resolution	2048x1536 pixels (can be sub-sampled)
Sensor size	6.5mm x 4.9mm, 3.2µm square pixels
Frame rate	6 fps at 2048x1536 or 20 fps at 1024x768 (sub-sampled)
Internal memory buffer	1 frame
Power Requirement	USB power or external 6V, 500mA
Power Consumption	~ 2.5 W
Exposure	Automatic/Manual
White Balance	Automatic/Manual
Dimensions (W x H x D)	2.25 x 3.85 x 1.56 inches

surprisingly sparse. Several were investigated but one was clearly superior in the quality, performance, and selection of its product line. The camera purchased for this project was a model Lu375 made by Lumenera Corporation. This is a CMOS 3.1 megapixel color USB 2.0 camera that can run at six frames per second at full resolution. It is equipped with a standard C-mount lens connection point so it can accept a wide variety of lenses. A summary of the camera's specifications is given in table 3.3.

The camera functions entirely over the USB connection. The connection is sufficient for the operating power needed to run the camera. This connection also provides the communication path for all commands and image data. Software is included that provides Windows drivers for direct integration of the camera into OEM applications. Through this software, the embedded computer has complete control over the camera operation including frame rate, resolution, white balance, etc. One additional feature included in the camera is an I/O port that allows synchronization with external devices such as strobe lights, etc. This is not intended to be used in the current design but may find future application.

6) *Detectors*: The detectors are another core component in the AGLITE instrument as this is where the received photons are collected and turned into a measurable electrical signal. After the light is collected in the telescope it is passed into a series of optics that condition and filter the light before it is incident on the detectors. A set of dichroic mirrors, exactly like those used in the measurement of the outgoing laser, is used to separate the incoming light into the three laser bands of interest. Once separated, the light passes through a set of extremely narrow band-pass filters to eliminate as much of the skylight contamination as possible and allow only the laser wavelengths through. This filtered light is then incident on the detector surfaces for each wavelength. In response to each incident photon, a small charge or current is produced by the detectors. For an analog data acquisition scheme, this signal is a continuous current that is then digitized using analog-to-digital converters. However, for a photon-counting data acquisition scheme, this signal comes as a series of pulses and a complementary set of circuitry is used to discriminate this signal and create a corresponding digital signal. The digital signal is TTL compatible and can be transmitted over longer cables to the counters. The proper selection of the detectors was a critical aspect in achieving the operational expectations of the project. For this initial design phase, only detectors optimal for photon counting were considered. Detectors used for an analog data acquisition approach have slightly different qualities that make them more suitable for that application.

The primary properties of the detectors that were considered in the selection process were quantum efficiency, maximum count rate, and gatability. Based on these factors, a photomultiplier tube (PMT) was chosen for the UV and visible beams and an

avalanche photodiode (APD) is used for the IR beam. The most significant factor in determining this first level of selection was the quantum efficiency spectrum. The photosensitive materials used on the surfaces of these devices are subject to a widely varying response based on the wavelength of the incident light. Except for a few very new and expensive PMT designs, PMT's in general have a very good response in the UV and visible regions but have very weak detection ability in the IR. Due to the silicon in APD's, they have a spectral range that just reaches to the 1064 nm wavelength used in this instrument but their other performance characteristics cannot fully match those of the PMT's. For this reason, PMT's are used wherever possible to take advantage of their performance, but for the wavelength that cannot be reached by these, an APD is used instead.

a) *PMT's*: For the two shorter wavelengths (UV and visible), the detector selected is a photomultiplier tube (PMT). The operation of these devices was explained previously; however, in short, they are a vacuum tube with a photosensitive material on the cathode end that triggers a cascade of electrons when excited by a photon. The cascade of electrons is amplified in several stages until reaching the anode end of the tube as an appreciable charge. For simplicity, the same tube is used for both the UV and visible wavelengths. A wide range of tubes was considered from different manufacturers such as Hamamatsu Photonics Corp., Electron Tubes Ltd., and Burle Industries, Inc.

There were several specific things looked for in the selection of the best product for the project. The first required feature for the detectors was that they be fabricated with a protective housing that provides a light-sealed enclosure along with structural mounting points, cable connections, etc. It was also preferable that the housing have

electromagnetic shielding properties as well. Secondly, a discriminator was required that was matched to the output of the PMT to provide the TTL compatible signals that are sent to the photon counter. For PMT's that have been designed for photon counting, this module is generally available as an accessory or may be built directly into the housing. Initially, there was a third requirement placed on this selection, namely that the tube be gatable with a manufacturer supplied gating circuit. This feature was to protect the tube during the initial release of light from the laser while the pulse was still at close range. After lengthy research into the available products, no product could be found that was capable of gating at the desired rates (10+ kHz) and was also suitable in its other performance characteristics. Furthermore, detailed simulations of our operating conditions had shown that there was no apparent risk of overexposure of the PMT's even at close range. For these reasons, the gatability requirement was dropped but remained a preference if it were found plausible.

Given the requirements that were placed on the PMT selection, what remained was to select a PMT that had the best performance within those requirements. Performance was judged first on quantum efficiency. Quantum efficiency is a percentage rating that indicates how many of the total incident photons will register an output pulse from the detector. For instance, a detector with a quantum efficiency of 20% will only produce an output pulse for an average of 1 in 5 photons that strike the surface. The next performance criterion was the pulse-pair resolution. This is the minimum time from one registered photon to the next that will still result in two distinct output pulses. This time is the sum of the rise time, fall time, and width of the PMT output pulse. Additionally, it also takes into account the discriminator circuit which often creates a slightly longer TTL

output pulse than the analog input pulse. If photons are registered by the detector faster than the pulse-pair resolution, an event known as saturation occurs in which it is impossible to distinguish one pulse from the next and the photons cannot be counted. The counting hardware also has a pulse-pair resolution limit which in this case was 22 ns. The performance goal for the PMT selection was to match this number. The final performance characteristic that played a role in the PMT selection is the dark count rate. One characteristic of PMT's is that even in an environment completely devoid of light, due to random processes within the tube there will still be an occasional signal produced. This is known as dark current, or for photon counting PMT's, dark count. Most PMT's will have a count rate that ranges between 10 and 1000 counts per second. While the low end of this scale is preferable, for this application, even the high end of this scale does not add a significant error to the measurement so this factor was considered lightly during selection.

Ultimately, after weighing all of the requirements and performance of the PMT's under consideration, the tubes selected were from Electron Tubes, Ltd. The tube is a 9954A series that was selected for low dark counts and afterpulsing. This is a 2-inch end window tube with a bialkali photocathode. The values chosen for the resistor network placed on the dynode stages are constant across stages 2-8 and then ramp up to 3 times their constant value on stages 9-12 before reaching the anode end of the tube. This is commonly done for pulsed light applications. The enclosure is a B2F/RFI housing. In addition to the required features mentioned previously, this housing contains a Mu-metal ferromagnetic shield to protect against magnetic interference. The PMT is potted securely into the housing along with a small circuit board containing the resistor network.

TABLE 3.4
SPECIFICATION SUMMARY FOR THE PMT DETECTORS

Description	Value
PMT – 9954A	
Photocathode material	Bialkali
Active photocathode diameter	46 mm
Quantum efficiency – 355 nm 532 nm	~ 27% ~ 13%
Dark count rate	< 800 per second
Maximum gain	18×10^6
Nominal input voltage range	1.8-2.3 kV
Voltage damage threshold	2.8 kV
Single electron rise time	2 ns
Single electron FWHM	3 ns
Transit time	41 ns
Amplifier/Discriminator – AD6	
Discrimination threshold	-2 mV
Output pulse rise/fall time	2 ns/2 ns
Pulse-pair resolution	20 ns
Power requirement	+5V, 10mA
Housing – B2F/RFI	
Dimensions (diameter x length)	75 mm x 225 mm

The power and signal connections are brought out to BNC connectors at the rear of the tube. The discriminator is model AD6 and requires a +5V supply voltage for the internal circuitry. This module is housed externally to the PMT housing in a small enclosure and is connected by short coaxial cable to the PMT. A summary of the detailed specifications for the PMT modules are given in table 3.4.

b) *High voltage power supplies*: Photomultiplier tubes operate at very high voltages to produce the electron multiplication effect between the dynode plates. The PMT's used in the AGLITE instrument have a nominal operation range between -1.8 kV and -2.3 kV at the photocathode. The precise voltage level applied affects the overall

gain of the tube so this is often adjusted depending on atmospheric conditions to produce the desired output signal. Applying this voltage requires special high voltage (HV) power supplies. The supplies chosen for this application and are designed for use as PMT power supplies and are made by Spellman High Voltage Electronics Company. In the design there is a power supply provided for each PMT to avoid any possibility of cross-talk between the tubes if they were run on the same power supply.

The model chosen is the MP2.5N24/F from the MP series of power supplies. These are high stability 10W power supplies whose output voltage is electronically controllable. The particular model chosen has a full scale output of -2.5 kV. The PMT's actually run in a reverse polarity where the cathode voltage is driven extremely negative and the anode is at ground. Usually, however, this distinction is not made in a general discussion about the operating voltages; it is simply assumed. This voltage was chosen because it covers the full operational range of the PMT's but does not have the capability of exceeding the PMT damage threshold of 2.8 kV. In this way, even if the operator set the supply at full output, there would be no way to inadvertently cause damage to the detectors. The output is adjusted by an analog 0-10V signal that is produced by the custom electronics board and is computer controlled. The details of this control are given in Chapter 3, Section B.3 of this report. The HV supply draws DC power from the +24V power supply and can draw up to 1 Amp if running a full output. The actual output of the HV power supply is monitored for both voltage and current. This information is output on two 0-10V analog signal lines that are fed back into the embedded computer through the custom board and the ADC card. Finally, the flange mount chassis option was selected for easy mounting to the custom enclosure.

c) *APD's*: The final detector included in the current AGLITE design is for detecting the IR wavelength of the laser at 1064 nm. This wavelength is problematic to detect because it falls well out of the usable spectrum for PMT's. For this reason, an avalanche photodiode (APD) is used instead. Even using an APD, this wavelength is barely detectable but it does still fall within the performance specifications and it has been shown in other instruments to work sufficiently well. An APD is basically the same idea as a normal photodiode but it is designed to create a large amount of current with very little stimulus. The Geiger mode APD's, such as are used for photon counting, can produce a measurable output signal from a single photon as stimulus. The quantum efficiency is generally very high for an APD (approaching 60-70% in the visible spectrum) which allows it to just barely reach to the 1064 nm wavelength where it has an efficiency of only about 1-2%.

Given the efficiency advantages of using APD's, it begs the question as to why not use APD's for all of the wavelengths in the AGLITE system. There are several reasons for this. First of all, while the spectral range can reach into the IR for an APD, it has virtually no UV detection ability making it useless for the 355 nm wavelength. The second major disadvantage is found in the time response performance. The physics that drive an APD's functionality require that the device be 'quenched' after the diode dumps a large amount of current. Effectively, this stops the avalanche effect and returns the device to its ready state to receive the next incident photon. While advances are being made in the design of APD's, this quenching process is still relatively slow which gives them a poor pulse-pair resolution. The APD chosen for this application has a pulse-pair resolution of only 100 ns which is outstripped by the PMT's by a factor of five. The third

disadvantage to APD's is in the difficulty of physical interface to the device. The active area of the chosen APD is only 175 μm in diameter which is miniscule in comparison to the 46 mm diameter of the PMT. Due to the small size, the incoming light must be focused using very carefully aligned optics. Any error in the alignment can have severe ramifications for the received signal. The precision required in alignment also dictates that a sturdy module be built around the APD that can be easily mounted and provides a good thermal path to remove heat from the device. While there are clearly some disadvantages to using APD's as detectors, they nevertheless have capabilities not found in PMT's and therefore were still the best option for the IR detector channel.

In the selection of the APD it was determined that the complexity in designing and building the mechanical and electronic infrastructure required for an APD was beyond the practical scope of this project. Therefore a module was sought that contained a fully functional APD system designed for use as a photon counter. The product chosen is made by PerkinElmer, Inc and is the called the Single Photon Counting Module (SPCM). This is a self-contained device that requires only a +5V power supply and a gate signal as input. Its output is a TTL signal that interfaces directly to the counting hardware. It contains a high voltage power supply, thermal control, a thermoelectric cooler, an active quench circuit, and a discriminator to produce the output signal. The model that was chosen was the SPCM-AQR-14. In form and function, all of the SPCM models are the same but they are differentiated post-production based only on the dark count of the detector. Most of the important performance characteristics for the APD module are the same as for the PMT's so a lengthy description is not repeated here. A summary of these characteristics for the SPCM module is given in table 3.5. One major

TABLE 3.5
SPECIFICATION SUMMARY FOR THE SPCM MODULE

Description	Value
Detector Properties	
Active detection diameter	175 µm
Quantum efficiency – 1064 nm	~ 2% typical
Dark count rate	< 100 per second
Signal Properties	
Gate delay time (enable/disable)	55 ns/4 ns
Output pulse width	35 ns
Pulse-pair resolution	70-100 ns
Housing Properties	
Power requirement	+5V, 1.9A max
Dimensions (L x W x H)	127 x 76 x 34 mm

feature that the SPCM possesses that was not available for the PMT's is a gating circuit. This is controlled with a TTL signal to either enable or disable the input signal.

7) *Photon Counting Data System*: The final major piece of requisitioned hardware is the photon counting data system. This device is responsible for timing the incoming pulses from the detectors and counting them in their corresponding range bins. It also performs internal integration of successive pulses over the same set of range bins before passing this data on to the computer. This is known as an MCS (multi-channel scalar) device. A wide variety of them are available from various manufacturers. Most of these, however, are somewhat slow in their resolution and do not handle more than a few signal channels simultaneously. For the purposes of this project, an MCS with moderate to high speed capability was needed that could also handle a large number of channels simultaneously. In addition, it needed to be compact and easily interfaced to the embedded computer. To find a suitable product, we relied on past experience with other

lidar systems, in particular, several systems owned and operated by the Goddard Space Flight Center. These lidar systems use photon counting data acquisition boards that are made by ASRC Aerospace Corporation. Our colleagues' experience with these products had shown them to be powerful and versatile as well as robust for field use. These products were investigated for use in the AGLITE instrument as well and were found to be the most suitable option.

The model of MCS board that was chosen is the very latest in ASRC's product line. It is the Advanced Photon Counting System (APCS). It has ten simultaneous signal channels which is enough to accommodate the most ambitious expansion plans for the AGLITE system. For synchronization it uses a TTL 'sync' pulse to initiate data collection on all the channels. The interface to the embedded computer takes place over a USB 2.0 interface. On this interface the computer initially sets all of the data collection parameters. Once data collection has begun, the packaged data is sent back to the computer over this same connection. The APCS card also has several features that are not used in this application such as serial UARTs, analog input channels, digital output channels, and an IDE hard drive interface. These functions are provided for systems in which the command and control of the entire system can be performed by the APCS card itself without the use of another computer. For the AGLITE instrument, however, this was not feasible so the functions are left unused. Another important feature of the APCS board is its memory architecture. It has what is known as a ping-pong memory structure to facilitate uninterrupted data collection. The ping-pong structure is two memory banks organized in parallel that can be accessed either by the electronics that store new counts to the memory or by the electronics that handle the data transfer over the USB port. In

TABLE 3.6
MCS PARAMETERS FOR THE PHOTON COUNTING SYSTEM

Parameter	Value
Number of channels	1 to 10
Input signal sample period	8 ns
Pulse-pair resolution	22 ns
Bin width #1	40 ns to 8184 ns
Bin width #2	40 ns to 8184 ns
Bin width transition location	2 to 4094
Number of bins	2 to 4095
Number of accumulation cycles	1 to 32767
Accumulation delay	8 ns to 1016 ns

operation, one side of memory is used to accumulate the incoming counts while the other memory is emptied through data port. When the collection cycle ends, the memories toggle to allow the data to be dumped while new data is being collected.

The parameters that establish the receiving, partitioning, and integration of count pulses are known as the MCS parameters. The MCS parameters for the APCS card are given in table 3.6. Each of these must be set up before data acquisition begins. The first parameter is simply the number of signal channels that will be used during data collection. The sample period is the clock speed of the input samplers. These samplers look for high-low or low-high level transitions to detect the TTL input pulses from the detectors. The pulse pair resolution is the minimum time between rising edges of the input pulses in order for them to be detectable. The bin widths are the length of time over which received pulses will be clustered into the same range bin. The minimum width is 40 ns which corresponds to a range distance of 6 meters. This is the best spatial resolution that can be achieved by the AGLITE instrument using the photon counting data system. The APCS card has the option of setting two different bin widths, one for

close range and a different one for long range. The bin number at which these widths switch is the bin width transition location. The number of bins is the number of memory locations that exist for collecting data in. If the minimum bin size were used, the lidar would have a maximum range of about 24.5 km before it ran out of bin locations to store data in. This is well beyond the expected operation of the AGLITE and if a greater range was needed, the bin width could be expanded from its minimum size. The number of accumulation cycles is the number of pulses over which the card will integrate the incoming signals. At the end of the accumulation cycles, the data is dumped to the USB port. Finally, the accumulation delay is a timer that can be set to create an offset between the reception of the sync signal and the beginning of data collection. For the AGLITE, this operation is absorbed into the synchronizer.

The APCS is a very efficient and elegant device for collecting all of the photon counting data and is ideally suited in performance and scope to the AGLITE instrument. The software for the card is a simple set of drivers for the Windows operating system that are easily integrated into the main software package for the instrument. All of the data rate considerations are covered in the data rate section of the high-level system design chapter (2.C.3).

B. *Custom Designed Hardware*

In addition to the requisitioned components, the AGLITE electronics system contains a certain amount of hardware that was custom designed to fulfill the specific needs of the project. This hardware forms many of the subtle connections between components and allows them to interface to one another. The custom electronics can be

divided up into four primary sets of circuitry – the temperature sensors, the computer controlled relays, the high voltage power supply controllers, and the synchronizer. There is also some secondary circuitry such as the on-board power conditioning and the connector routing. All of the primary circuits except the synchronizer were prototyped by hand before proceeding to a formal PCB layout to verify the expected operation of the components. The formal schematics were created using Mentor Graphics software which was also used for creating the physical layout of the PCB.

1) *Temperature Sensors*: The purpose of the temperature sensors is to provide information to the operator on the approximate thermal status of the instrument. The sensors are located in the electronics enclosure and in various locations in the lidar instrument itself. The circuit design allows 16 sensors to be multiplexed through a single channel of the ADC card in the embedded computer. These 16 sensors are allotted as follows. Sensor number 16 is integrated as part of the custom PCB to monitor the on-card temperature. Sensor numbers 13-15 leave the card in a DB-9 connector. These are intended for placement inside the custom electronics enclosure. One will monitor the ambient internal temperature. The other two will likely monitor the DC power supplies and the high voltage power supplies. The final 12 sensors leave the card on a DB-25 connector which is routed directly to the back panel of the chassis for connection to the instrument through the main umbilical cable. The exact placement of these sensors is not fully determined; but it is known that sensors will be placed on each detector since these are susceptible to overheating. Also, several sensors will monitor the temperature of the optics plate at different locations to provide an indication of uneven heating which may cause flexing of the plate and misalignment of the optical paths.

The design of this circuit was driven by several main ideas. As was explained, the temperature sensors are entirely housekeeping devices and are not involved in the scientific purposes of the project. For this reason, some leeway was allowed in the accuracy of the sensors in favor of producing a very simple set of circuitry. The sampling rate for the sensors is expected to be below 1 Hz so there was no need to use components capable of high frequency operation. Also, because of the low sample rate, the signals could be multiplexed into a single channel of the ADC card to avoid unnecessary taxation of the limited ADC channels.

The actual temperature sensor circuit consists of only four components – a digital buffer, multiplexer, the sensor themselves, and a shunt resistor to convert the current signal to a voltage. The basic circuit is shown in fig. 3.1. All of the custom circuits require control that is provided by the embedded computer through the digital I/O card. The temperature sensors are allotted one 8-bit port of digital I/O. The standard approach for all of the circuits was to buffer this digital connection. The digital I/O card was capable of providing plenty of drive current but an extra layer of protection against possible damage to the card was included as a precaution. For this circuit, the digital connection was for command only so bidirectional data transfer was not needed. The buffer selected was a SN54ACT244 octal buffer made by Texas Instruments. The '244' chip is very commonly used for buffering digital signals and is a reliable and easy to use part.

The second part in the temperature sensor circuit is the analog multiplexer. The part used for this is the ADG526A made by Analog Devices. This 16-channel multiplexer has the capability of latching the inputs for interface to a microcontroller;

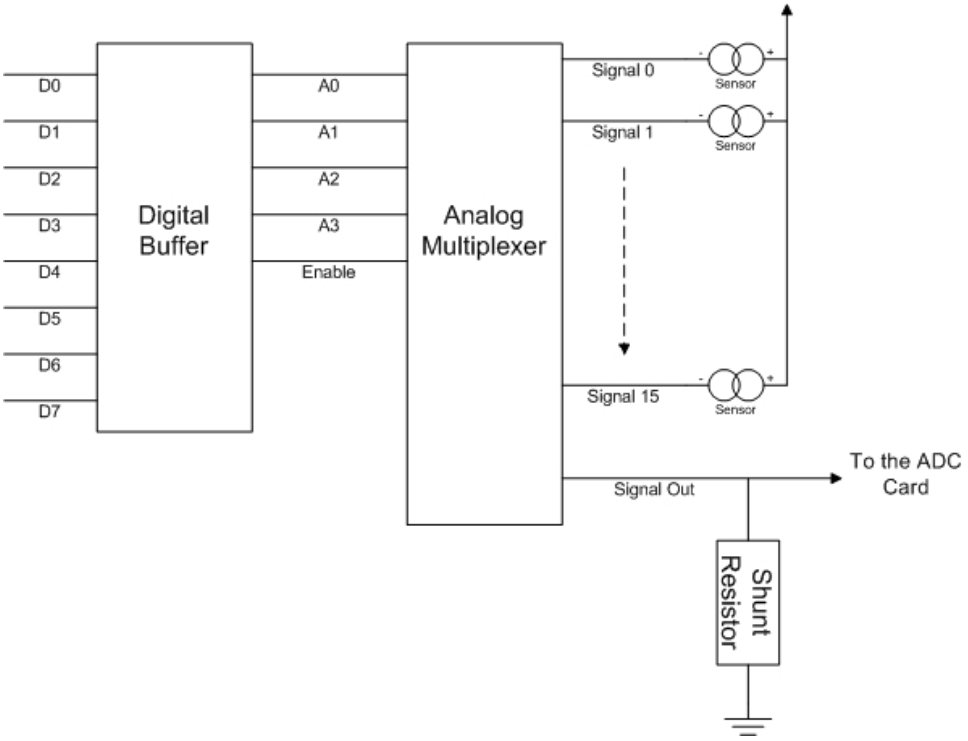

Fig.3.1: Temperature sensor functional diagram.

however by disabling this feature, the device becomes very simple to use by simply encoding the desired signal on the address pins. The multiplexer has a typical 'on' resistance of about 300 Ω which is small in comparison to the shunt resistor so it has little effect on the voltage registered on the output terminal that is passed to the ADC card.

The most obvious component of this circuit is the temperature sensors themselves. The sensor chosen was the AD590 made by Analog Devices. This device is a temperature transducer meaning that it accepts a very wide range of input voltages and generates an output current that is regulated to 1μA per degree Kelvin. This two-pin interface makes it very easy to integrate in a design and the device is entirely self-contained, meaning that is requires no external circuitry for signal linearization, temperature reference, etc. Also, the sensor accepts any input voltage from 4 to 30 volts,

making it ideal for physical locations that are far from the ADC and must be reached over long cables. The AD590 comes in three forms: a surface mount chip, a metal canister, and a flatpack device. For this application, the metal canister will be used for the on-board sensor and all the rest will be flatpacks that can be adhered directly to the components. The sensors come in several models with different levels of accuracy. For the sake of cost, the K model was selected for this application which is accurate to ±2°C with proper calibration.

As mentioned, the signal output from temperature sensors is a current regulated at 1 µA/K. For a typical temperature of 25°C, this equates to 298.2 µA. By dropping this current across a 10 kΩ resistor to ground, a voltage of 2.982 V is produced which is easily read by the ADC card. For the maximum temperature range of the sensor, -55°C to 150°C, the voltage output would range between about 2.4V and 4.25V, which is well within the allowable input range of the ADC card. Clearly, however, the instrument could never operate in an environment anywhere near these maximum ratings because most of the other components in the system would fail long before reaching these extreme temperatures.

2) *Computer Controlled Relays*: The computer controllable relays are a part of the future planning included throughout the electronics design. It was anticipated that in certain operating environments active thermal regulation of the AGLITE instrument would be necessary. This could potentially be in the form of both cooling and heating. In the current mechanical design, there are no fans or heaters included, but these could be added without great difficulty as the need arose. The purpose of the relays is to provide electronic control over these devices or any other unforeseen components that might

require basic power control.

Since the devices that may be controlled by the relays are unknown, it was important to choose a relay that supported both AC and DC voltages at potentially high currents. For AC power, most devices are designed to run off a standard wall socket which operates at 110-120 VAC with at least 10 Amps of output current capability. This was set as the minimum requirement for the AC power. For DC power, a minimum voltage rating was chosen to be 24VDC which is the maximum DC voltage currently in the entire system. Also, since there was already other circuitry in the system that required a +24V power supply, it was prudent to select a relay whose coil also operated at 24V to avoid the need for additional power supplies. To meet these requirements, a product was selected from Omron Electronics called the LY1 general purpose relay. This is a single-pole/double-throw (SPDT) relay that fits into a rail-mount socket with screw-post terminals for external connections. The LY1 relay is rated for 15 Amps at either 110VAC or 24VDC. Also, it is available with a 24VDC coil that has a coil resistance of 650 Ω meaning that the current draw is only 36.9 mA when it is turned on.

The relays are controlled by digital signals from the embedded computer. These signals must be buffered electronically to provide sufficient power to operate the relay coils. For this purpose, the relay drive circuit shown in fig. 3.2 was designed. The heart of this driver is an array of Darlington transistors that provide an electronic low-side switch for the relay coils.

The drivers are controlled by the embedded computer through the digital I/O card and the entire circuit is allotted one 8-bit port from the card. The digital signals are buffered initially using the same 74ACT244 chip as was used in the temperature sensor

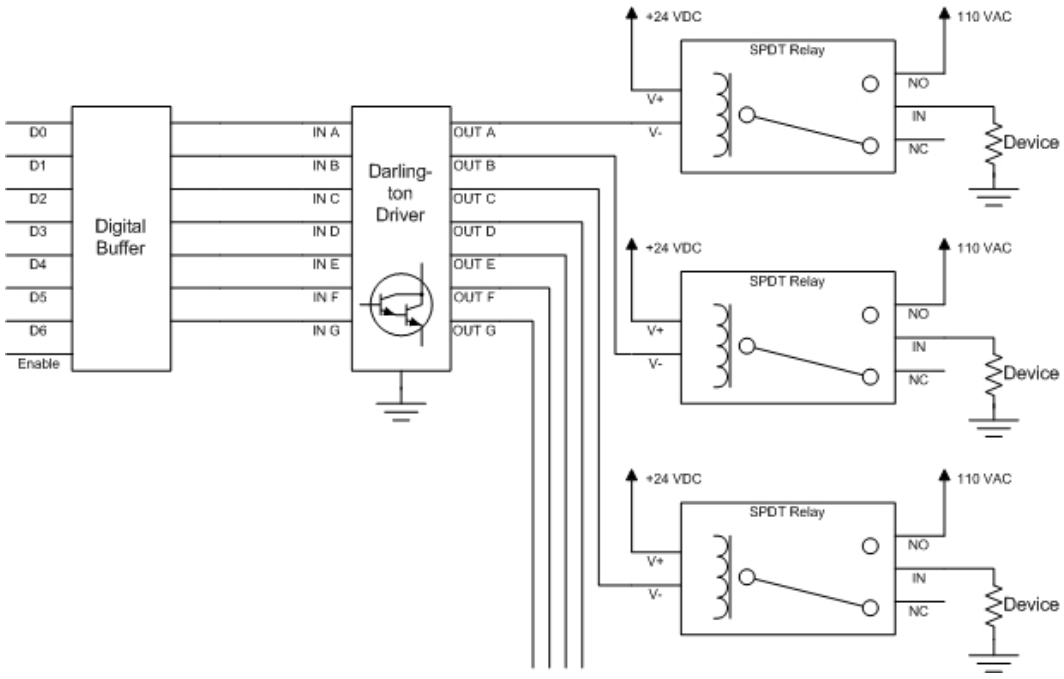

Fig. 3.2: Relay driver block diagram.

circuit. The outputs of the digital buffer are pulled low through 10 kΩ resistors (not shown in the diagram) to ensure that a low signal assertion is always present at the inputs to the Darlington array unless they are intentionally driven high. The output of the digital buffers have a tri-state setting so the pull-down resistors are included to ensure that a floating output from the buffers does not inadvertently allow the Darlington transistors to turn on.

The Darlington driver used in this design is part number ULN2003A made by Texas Instruments. This same chip is also made by several other manufacturers. It contains seven Darlington transistor pairs that share a common source which in this case is connected to ground. The inputs to the Darlington pairs are CMOS compatible so they can be easily driven by the digital buffer. The current-sinking capacity of each pair (in

the surface mount package) is 500 mA when operating individually. However, in a worst case situation where all of the transistors are on at the same time with a 100% duty cycle, the current capacity drops to about 60 mA per channel in a 70°C environment. Even under these conditions, the drivers can still operate the relay coils which draw only 37 mA when turned on.

The relays are connected to the Darlington drivers through the ground path from the coil as shown in the figure. One side of the coil is tied high at +24V and the transistor then serves as an electronic switch to complete the circuit to ground. The wiring configuration for the device side of the relay has the normally open (NO) pin connected to the supply voltage. The normally closed (NC) pin is left with no connection and this is the rest state of the device. The input (IN) pin of the relay is connected to the device which is then connected to ground.

3) *High Voltage Power Supply Controllers*: Photomultiplier tubes are used as detectors for the UV and visible wavelength laser beams. These tubes are operated at voltages that range between about 1700 and 2200 volts. These very high voltages are provided by high-voltage (HV) power supplies. Having the ability to adjust the voltage applied to the PMT's is very important so that the overall gain of the detector can be adjusted for different operating conditions. The HV supplies themselves are electronically adjustable so they can provide a range of voltages to the PMT's. The control to these power supplies is provided by a DC analog input voltage that ranges between 0-10V which scales the HV supply output between zero and its full-scale rating. Also, each of the power supplies has two analog output signals that give a scaled reading of the actual output voltage and the output current. These are both 0-10V signals that

must be read back into the controller for output monitoring.

A representation of the high voltage power supply control circuit is shown in fig. 3.3. The analog control voltage is created individually for each of eight possible HV power supplies using a set of eight digital-to-analog converters (DAC's). The output of these converters is buffered using op amps in a voltage follower configuration. The

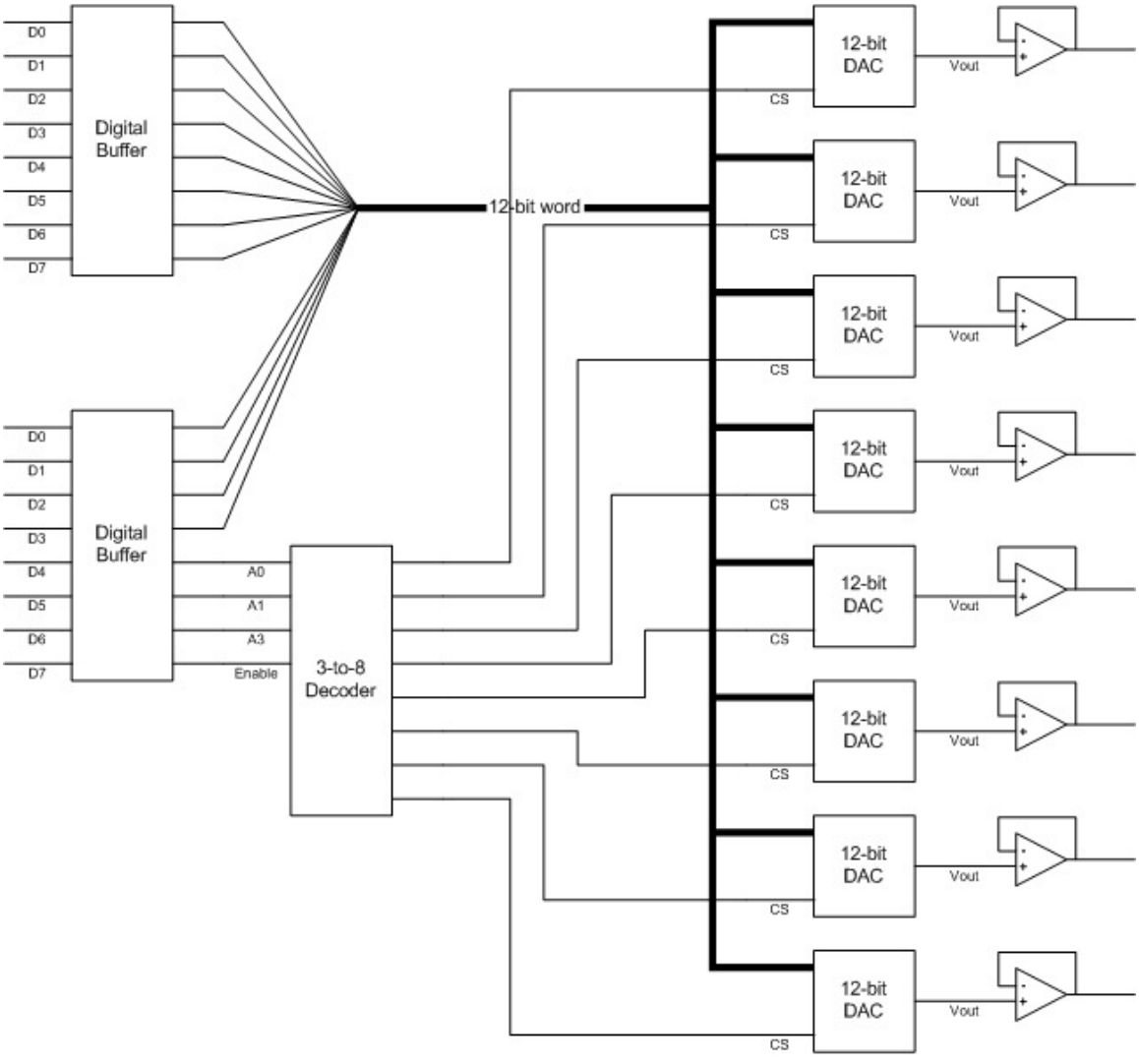

Fig. 3.3: High voltage controller block diagram.

DAC's are arranged in a microcontroller data bus configuration. A 12-bit data bus is connected in parallel to all of the DAC's. A 3-to-8 decoder is then used to generate a chip select signal which stores the value on the data bus into the corresponding DAC in internal registers. In this way, eight 12-bit DAC's can be controlled using only 16 digital I/O lines from the digital I/O card in the embedded computer. A secondary function that is included in the HV supply control circuit is a 16-channel multiplexer for reading back monitor signals from the HV power supplies. This is not shown in the figure because this circuit is identical to the one used for the temperature sensors shown in fig. 3.1 minus the shunt resistor. Control of this circuit requires another port from the digital I/O card making the total three 8-bit ports for the HV power supply control circuit.

All of the digital I/O connections to the HV control circuit are for command only, just like those in the temperature sensor circuit and the relay control circuit, meaning that 1-way digital buffers work fine for this application. There are three 74ACT244 chips in this circuit to provide this buffering. Twelve of these lines form the data bus for the DAC's. Four lines control the 3-to-8 decoder and five are used to control the analog multiplexer. The remaining three are unused. The 3-to-8 decoder is a SN74HC138 made by Texas Instruments. The '138' chip, along with the '244', is another device with a long legacy of use as a common part in bus architectures. It has three input address pins which are decoded to assert negative one of eight outputs. These outputs interface directly with the negatively asserted chip select pins of the DAC's. The decoder also has an enable input allowing none of the eight outputs to be asserted when no changes are being made.

The digital-to-analog converter selected for this controller was the AD767 made by Analog Devices. This device was selected for several reasons. First and foremost was

the resolution. As specified by the program leaders, 12 bits was the minimum resolution for the output voltage. Further investigation showed that any more resolution than this fell below the output accuracy of the HV power supply and would be useless anyway, so 12-bit resolution was set as the specification. The input format was the next major deciding factor in selecting a DAC. Several serial input devices were considered because of their low pin count but they were found to be rather complex to program and expensive. Therefore, a parallel input configuration was chosen which simplified programming a great deal and also allowed the convenient data bus architecture used in this design. There were very few performance constraints because these devices operate essentially at DC frequencies where their outputs are only likely to change every few minutes or hours. Since performance was not an issue, this allowed the selection of a cost-effective component which finally led to the AD767 which is relatively simple to use and ideal in performance for this application. The AD767 has several selectable output voltage ranges, one of which is 0-10V. This meant that no additional gain had to be applied to the output. It could simply be buffered and sent to the HV supply. The chip select pin serves as the read signal to latch whatever is on the data bus into the internal registers which becomes the new output voltage. Besides the twelve data pins, all the remaining connections to the chip are for setting the output range and precisely tuning the output for an accurate reading.

Each output of the DAC's is passed through an op amp to provide a buffer to the external device. The op amps are wired in a standard voltage follower configuration. The op amp chosen for this was the AD824 made by Analog Devices. This was chosen for several reasons. First, since the purpose of the amp was to serve as a voltage

follower, no special controls such as bias pins were needed, and a quad package was the best option. The AD824 was readily available as a quad package op amp, and one of its stated application purposes is a buffer for DAC outputs. Since it fell within the required voltage ranges and there were no other performance requirements to consider, this was selected as the output buffer.

The final component in the HV control circuitry is a multiplexer for reading back the data from the monitors on the HV supplies. Each supply has two monitor signals for total of 16 potential signals that must be read using the DAC card in the embedded computer. Like the temperature sensors, the time resolution needed for sampling these signals was less than 1 Hz. Since the components and the design used for the temperature sensors were completely compatible with the signals from power supplies, the same circuit was copied over for this application as well. The 16 channels are all fed through a single port on the ADC card and this is controlled using digital I/O that is passed through a buffer.

4) *Synchronizer*: The synchronizer has the most complex functionality of the custom circuitry. The purpose of the synchronizer is to handle the timing of all the time-critical components in the lidar system. This includes pulsing the laser, triggering the data acquisition systems, and controlling the detector gating. Early on, an analog solution was considered for this problem using one-shot timers to program the appropriate delays. However, this idea was abandoned due to the difficulty of reconfiguring the delays with the inclusion of additional components such as new lasers, detectors, or data acquisition systems. Also, assuring the accuracy of such circuit was problematic since it would be very sensitive to environmental changes. The chosen solution was to create a highly

programmable timer using a very fast PLD (programmable logic device). Such a device is perfectly suited to interface with the TTL signals that must be sent and received. By using an accurate crystal as the timing basis, very accurate and repeatable delays can be produced. An added feature is the ability to adjust the delays in the field. The delay, in this case, is simply a programmed number stored in the device that sets a terminal count. Once that count is reached then a signal is triggered. By making the count a piece of information that is passed in by the embedded computer instead of being 'hard coded' into the device, changing the delay time is as simple as a few key strokes in the field and does not require any physical access to the hardware. That feature is potentially very valuable, particularly during the calibration stages of the instrument development.

The selection of a PLD was the first critical task in the synchronizer design. The most critical constraint was speed. Since this was to be used as a very accurate clock, then the faster the device ran, the better the time resolution could be in setting the delays. To select the target speed, the speeds of other devices in the system were considered as well as the time scale of the measurements. The smallest time/range bin that could be resolved by the photon counting hardware was 40 ns which equates to a 6-meter range bin. To achieve this bin size the counting hardware actually samples the input every 8 ns. The time delay between resolvable single photon events for the PMT's (the faster of the two detector types) is about 22 ns. This means that even operating at the shortest bin size, the counting hardware can nearly resolve two photon events in a single bin. Therefore, since the synchronizer is the trigger for when the time bins start, its accuracy should ideally be something close to the timing accuracy of the counter which is 8 ns. Subsequently, this was set as the performance goal with the realization that half, or

perhaps even a third, of this speed was still acceptable. Beyond the speed requirement there was also the requirement that the device be large enough to contain the required programming and have adequate I/O for interfacing.

An initial investigation into the various types of PLD's showed that the only type of device that could meet the timing and size requirements was an FPGA (field programmable gate array). After this, the search for suitable devices focused on those families of devices that were already familiar and had a history of use at SDL. In the course of this search, an optimal device was found. It is from the Cyclone family of FPGA's made by Altera. Specifically, it is the EP1C3T144C6. This is one of the smaller members of this family but was much more than adequate for the programming and I/O needs of the synchronizer. Also, this device is rated for clock speeds as fast as 6 ns which easily met our best speed requirement. In practice the device will likely be run with a 10 ns clock for the ease of time/count conversions and to ensure that the FPGA is easily able to meet timing requirements regardless of the complexity of the programming. Since every logic gate has an intrinsic delay associated with it, complex programming will slow down the logic circuit because there are more sequential gates for the signal to pass through. If sufficient time is not provided for the logic output to settle before the inputs change, then logic errors will occur.

From a circuit standpoint, the synchronizer is not complicated. A diagram of the circuit components is shown in fig. 3.4. It consists of the FPGA with its accompanying components (i.e. the clock and the programmer) and the I/O transceivers. The clock is simply a crystal oscillator combined with its related circuitry that interfaces to the FPGA on a single pin. For programming, the FPGA has two different modes, AS and JTAG.

This circuit was designed to implement only the AS mode which loads the configuration into the FPGA serially through a 10-pin header on the board and a small configuration chip that talks directly to the FPGA. The header is connected over a special cable with a small embedded circuit to a normal PC with a parallel port. In this way, the program developed on the PC using any HDL such as Verilog can be loaded directly into the FPGA.

The only other parts that comprise the synchronizer circuitry are the transceivers. The FPGA operates with a 1.5V core and all of its I/O is 3.3V. Since the rest of the design is based on 5V, level shifting transceivers were included on all of the I/O channels

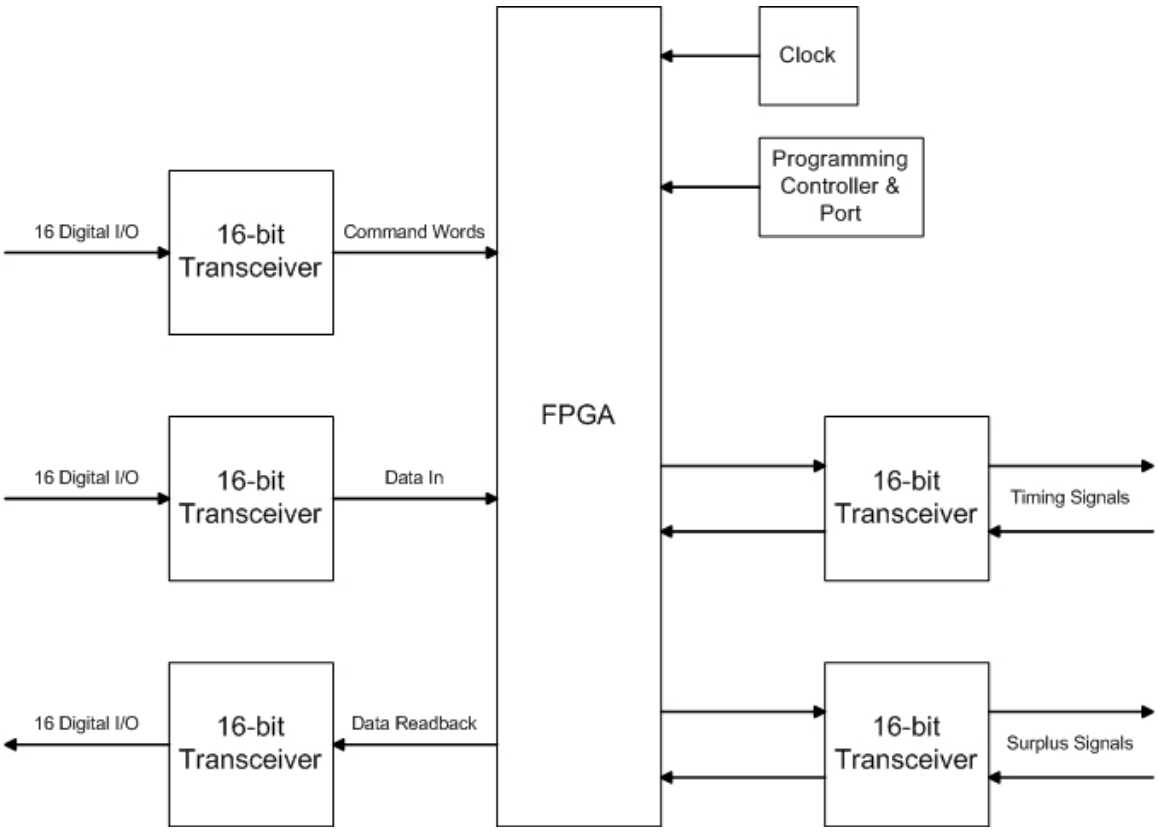

Fig. 3.4: Synchronizer circuit block diagram.

of the FPGA. The chip is called an SN74ALVC164245 and is made by Texas Instruments. These also function conveniently as bidirectional buffers/line drivers. Each transceiver handles 16 bits split into two 8-bit groups. The direction of each group is controlled by a direction pin. All of the direction pins on the transceivers are tied to the FPGA so that this can be programmable. The FPGA has a total of 100 possible I/O pins. Of these, 48 (six 8-bit ports) are used to interface directly to the digital I/O in the embedded computer so that all of the user defined delays and commands can be communicated to the synchronizer. Another 32 I/O pins are allotted to an external board connector for the passing of all signals to and from the synchronized devices. Ten more pins are used to control the directions on the five transceivers. The remaining ten pins are either used for a special programming function or are left unused. For a complete description of the pin assignments on the FPGA see appendix C.

A basic information flow diagram for the programming of the FPGA is shown in fig. 3.5. Internally, the FPGA will contain several 16-bit registers that will store information provided by the user. This information includes the desired frequency of the laser pulses, the number of regular pulses and background pulses to generate, and the time delays to introduce for the data acquisition trigger and the gate triggers. The number input for the delay and the frequency registers will not represent a certain time measured in seconds; rather, it will indicate the number of clock cycles required to accumulate until the desired time has elapsed. This number depends on the exact period of the oscillator and will be calculated in the user software, not in the FPGA. This information is loaded into the FPGA using the digital I/O connections shown in fig. 3.4. The ‘data in’ bus contains the actual value for each register. The ‘command’ bus has several purposes.

First, it addresses the register corresponding to the data word currently on the data bus as well as providing a write signal for the register. This bus also contains the mode bits for the detector gating, computer override signals, and an enable bit that starts the FPGA into

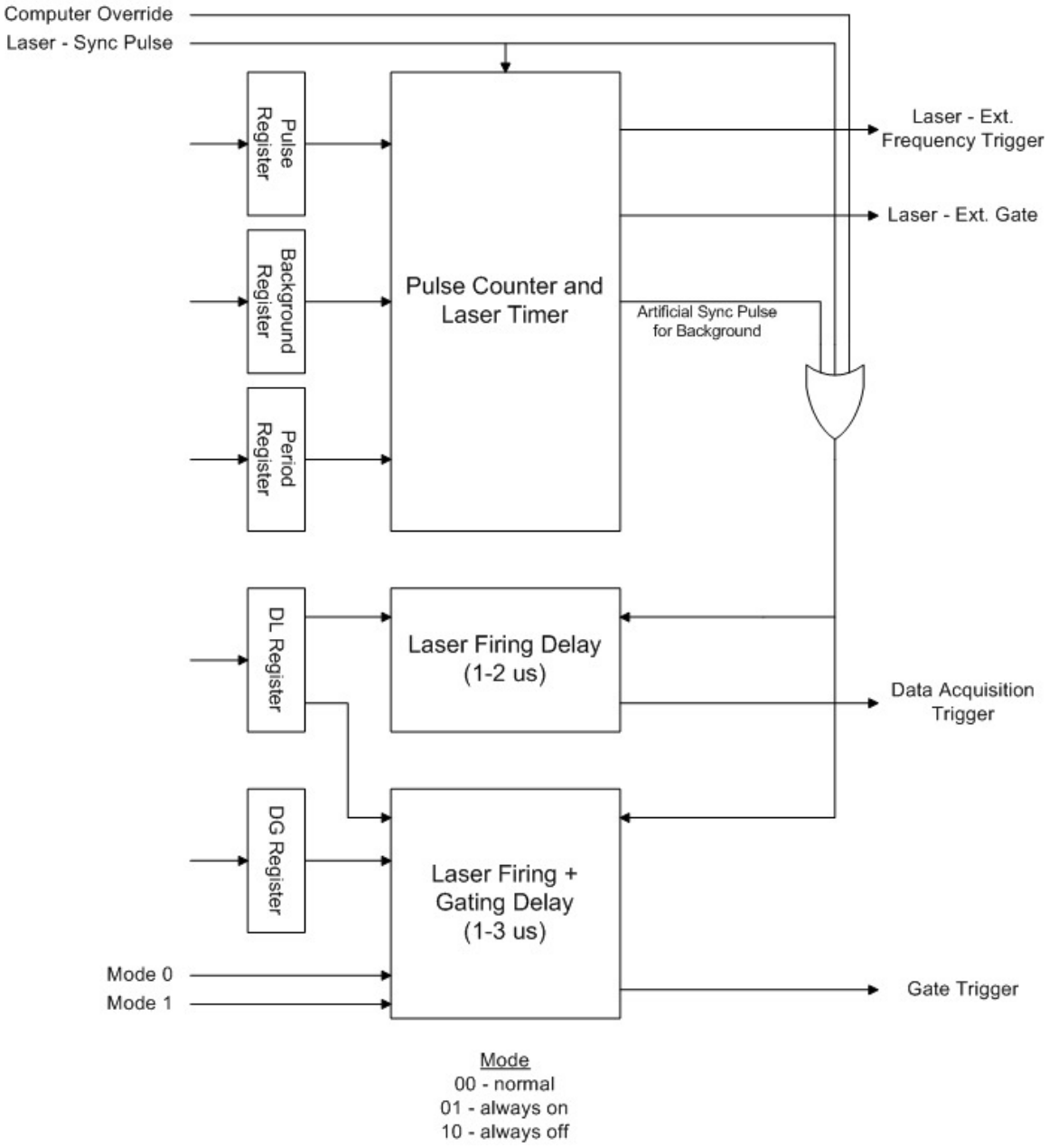

Fig. 3.5: Synchronizer functional diagram.

its normal operation mode. The remaining bits on the command bus are reserved for future needs. The 'data readback' bus is not represented on the basic information flow diagram but it is used to monitor the status of registers and counters to allow easy diagnostics from the embedded computer. The data that appears on the readback bus is also dictated by the control bus.

Normal operation of the FPGA will proceed as follows. (1) The registers will first be loaded with their corresponding values using the command and data buses. Initially, all of the counters will be reset to zero then an enable signal will trigger the FPGA to begin counting. (2) The frequency counter will start counting clock pulses until the period of a single laser pulse is reached. If the laser is to be pulsed at 10 kHz and the crystal has a 10 ns period, then the period of the laser pulse is 100 µs or 10,000 clock cycles. (3) When the terminal count of the frequency register is reached, several things will happen: (3a) If the pulse counter has not yet reached its terminal count, then it will increment by 1 and an output will be produced on the 'laser external frequency trigger' to tell the laser to fire once. Simultaneously, the 'laser external gate' will be turned on. (3b) When the laser receives this trigger signal, it will prepare to fire. Just before it is about to fire, it will produce a 'laser sync pulse' at a fixed time (about 1-2 µs) before the light will actually leave the laser head. (4a) The sync pulse will trigger the 'laser firing delay' counter to begin counting clock cycles. After 100-200 counts representing 1-2 µs (this is specified exactly with the delivered laser) the terminal count will be reached and will create an output pulse which is the data acquisition trigger. (4b) Similarly, the 'gate delay' counter will count off this laser delay time, in addition to an extra delay that may be introduced to gate the detectors from the initial laser burst.

This process (1-4) is repeated for each laser pulse until the pulse counter reaches its terminal count. (5) When this condition is detected, then the 'background counter' will increment by 1 instead of the pulse counter. In this case, no 'frequency trigger' signal will be sent to the laser. Instead, a sync signal will be artificially generated by the background counter and fed into the delay counters. To the rest of the system (i.e. the data acquisition and the detectors) it will appear identical to a normal laser firing sequence except there will be no actual laser pulse and only the background light will be detected. (6) Once the desired number of background pulse is reached, then both the pulse counter and the background counter will be showing a terminal count. When this condition is true then the counters will be reset and the process will begin again.

5) *Power Supplies and Power Conditioning*: As was depicted in fig. 2.2, the electronics in the AGLITE system require a variety of DC voltages to operate. A detailed list of the components was compiled along with their maximum power consumption and can be found in appendix F. These components include all of the devices that run on DC power, whether they are chips on the custom electronics board or modules that run external to this board but still use the same power supplies. The list is summarized in table 3.7.

The DC voltages required for the electronics system are provided with switching power supplies that run off of a 110 VAC input. To minimize the complexity of the power supplies, some of the required DC voltages are produced on the custom board instead of being provided directly. Specifically, the +15V, -15V, and +5V (digital) are input from one power supply. Using voltage regulators, the +5V (analog) and -5V lines are created from the +15V and -15V, respectively. Similarly, the +3.3V and +1.5V lines

TABLE 3.7
MAXIMUM CURRENT DRAW FOR INTERNAL VOLTAGE LINES

DC Voltage	Max Current (Amps)
+15 V	0.33
-15 V	0.40
+5 V (digital)	1.44
+3.3 V	1.3
+1.5 V	0.3
+5 V (analog)	0.23
-5 V	0.12
+24 V	4.26

TABLE 3.8
MAXIMUM CURRENT DRAW FROM DC POWER SUPPLIES

DC Voltage	Max Current (Amps)
+5 V	3.04
+15 V	0.55
-15 V	0.52
+24 V	4.26

are both created from +5V (digital) supply. The +24V line is provided with a separate power supply due to its high current needs. The part numbers of the regulators used in this circuitry are documented in appendix B.

By combining the current draw for the self-generated voltage lines into the supplied voltage lines, the total input current requirement was determined to be that shown in table 3.8. The power supplies chosen for to produce this power are produced by Artesyn Technologies. Open-frame power supplies were selected instead of enclosed supplies for two reasons – the open-frame formats have smaller physical dimensions and the combinations of output voltages were found to be more suitable for the project's

needs. The first three voltages are provided with a model NFS110-7604P supply. Assuming that the power supplies will be fan-cooled, the output of this supply can provide 10A, 5A, and 1A, respectively on the +5V, +15V, and -15V lines. The +24V line is provided by a model NLP150L-96S8 supply. Again, assuming that it will be fan-cooled, it can provide 6.5A of output current. These power supplies are rated to account for some growth in the system components (i.e. additional detector channels) but cannot accommodate the maximum number of devices eventually planned for this system. In the event that the project does expand to that point, different supplies will need to be selected. At this first stage in the project, however, it was not justifiable to use power supplies capable of the future potential power need. This is because the future need is somewhat difficult to predict and also because power supplies with a higher power rating would necessarily be self-cooled units that take up much more space in the instrument.

C. *Layout and Fabrication*

The physical layout of the electronics has been a consideration from the earliest stages of the project. One of the primary goals was to make an efficient use of space. Also, it was important to make the system easy to assemble in the field and to simplify the required interconnects between modules. The layout design consists of three hierarchal levels – the custom board layout, the custom electronics enclosure layout, and the rack organization. The board layout consists of the actual placement and arrangement of components and connectors on the custom electronics board. The enclosure is the rackmount box that houses the custom board as well as the DC power supplies, high voltage power supplies, and the relays. Finally, the rack organization considers all of the

rackmount modules including the laser controller, custom enclosure, motion controller, etc.

Each level of the electronics layout is dependent upon the configuration of the other levels. This relationship is especially true between the layout of the custom board and the layout of the custom enclosure. For example, the placement of the connectors on the custom board was influenced by the arrangement of the components inside the enclosure. Therefore, a good idea of how the components inside the enclosure would fit together was needed before the board layout could be completed. The arrangement of the connectors also affects the placing of the parts on the board while making considerations for trace lengths and signal integrity. Another important relationship is the interconnections between components in the custom enclosure (including the custom board) and the rest of the modules in the electronics rack. The routing and cabling of all the various signals had to be considered. The layout design presented here is the end result of these considerations and tradeoffs, and it has undergone a number of revisions throughout the course of the project. Currently, the custom board is in its fabrication stage and the most of the other components in the electronic system are on-hand. With the completion of the custom board, full-scale integration of the components will begin. This includes the assembly of the components in their chassis, the assembly of the custom cables, and software integration.

1) *Custom Board Layout*: The custom board consists of the custom circuits described in previous sections, i.e. the temperature sensors, the relay controller, the high voltage power supply controller, and the synchronizer. While each of these circuits is functionally independent of the others, they are interconnected on a board level where

they share their connections to the digital I/O card and the ADC card. All the circuits on the board also share common power planes and grounds. A block diagram depicting the high level connections of the custom electronics board is shown in fig. 3.6. This includes

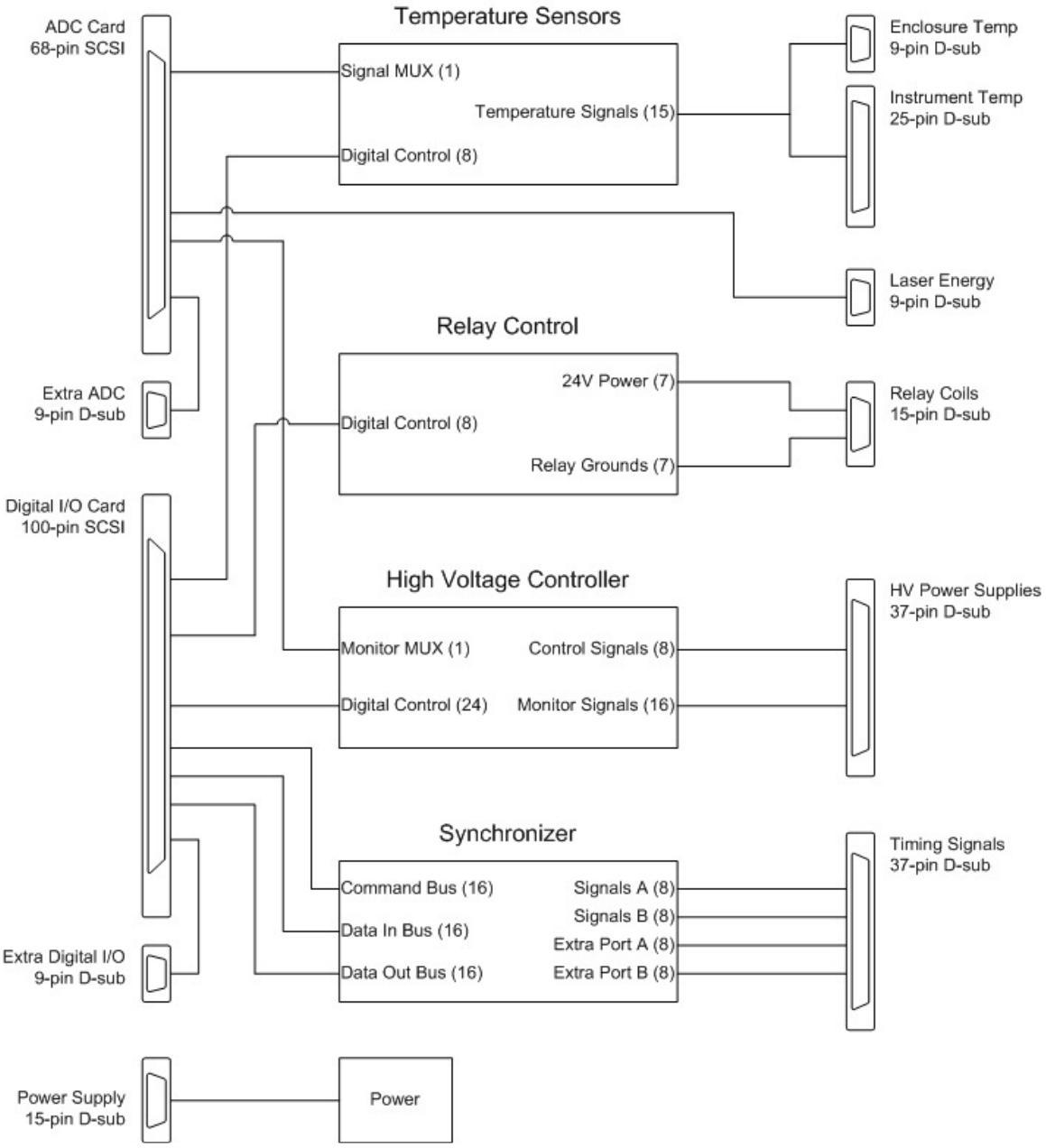

Fig. 3.6: High-level signal routing of the custom electronics board.

all of the external connectors.

The two large connectors shown in fig. 3.6 are 68-pin and 100-pin SCSI connectors that go directly to the ADC card and digital I/O card, respectively. Each of these cards has a few surplus channels that are routed to 9-pin D-sub connectors on the custom card for future use. Most of the channels, however, connect directly to the four main custom circuits. The exact port assignments that correlate the ports on the PCI cards their custom circuit are given in appendix E. The other connections shown on in the figure are connections that interface to the other components in the system besides the embedded computer. These are all comprised of D-sub connectors of various sizes. The details of the individual pin assignments for each connector are given in appendix D. This information contains specifications for the connector types for each end of the cable, pin number assignments, cable type to be used (coax, twisted pair, etc.), and a functional description.

As mentioned before, the layout of the custom board was partially dependent on the place of other components in the enclosure and in the system as a whole. The basic layout plan used in the fabrication of the board is shown in fig. 3.7. This placement plan also took into account the routing of traces on the board to minimize the trace lengths and overlapping traces. The two SCSI connectors were placed at the top of the board because these will be flush-mounted on the enclosure back panel. This allows the cables coming from the PCI cards in the embedded computer to connect directly to the card. The other connectors were positioned close to their respective external components while considering the simplest possible routing plan for the board traces. The synchronizer circuitry was placed in the upper-right corner because it possesses the most connections

to the digital I/O connector. This also creates very short traces to the synchronizer connector for the timing signals. The high voltage controller also has a large number of digital I/O connections, so this was placed next to the synchronizer in the upper-left corner and down the left edge of the board. This also places it close to the HV connector to provide short trace lengths for the outgoing analog signals. The extra ADC channel connector and the laser energy sensor connector consume almost all of the analog in channels so these are placed as close as possible to the ADC connector at the top of the board. The remaining space along the bottom of the board provided a convenient place for the much less sensitive circuits for the temperature sensors, the power distribution, and the relay control. The corresponding connectors and circuitry were placed near to

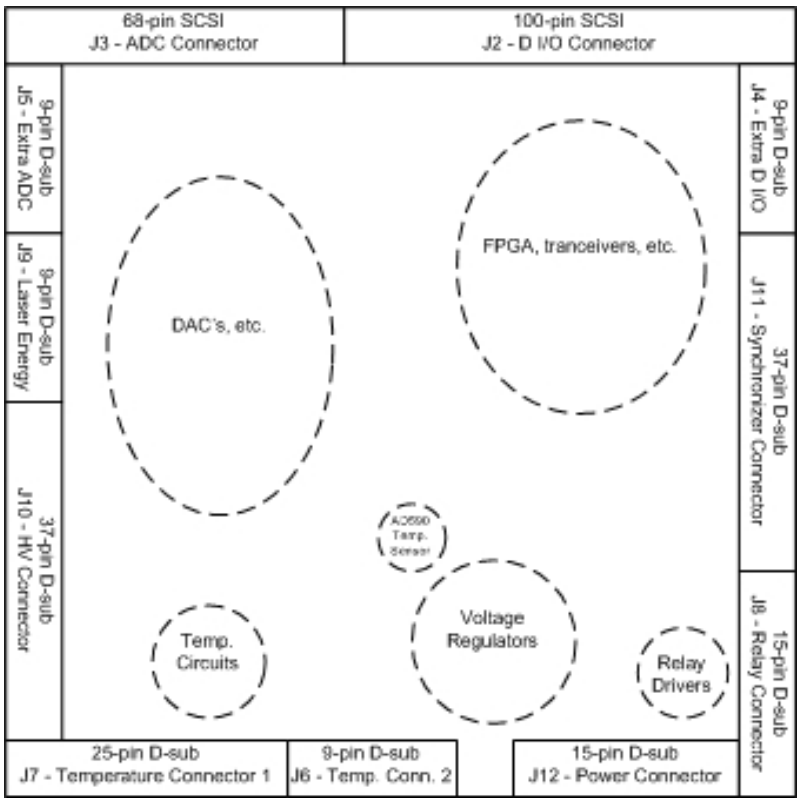

Fig. 3.7: Custom electronics board layout.

one another for easy routing.

After the basic floor plan was established, the fine details of laying out the board were performed by a layout technician at SDL. I was involved in all the critical decisions. In cooperation with the technician, we determined the trace widths for the signal and power traces, accounted for the current load for high power connections, designed the power planes, established the via dimensions, and planned the routing for

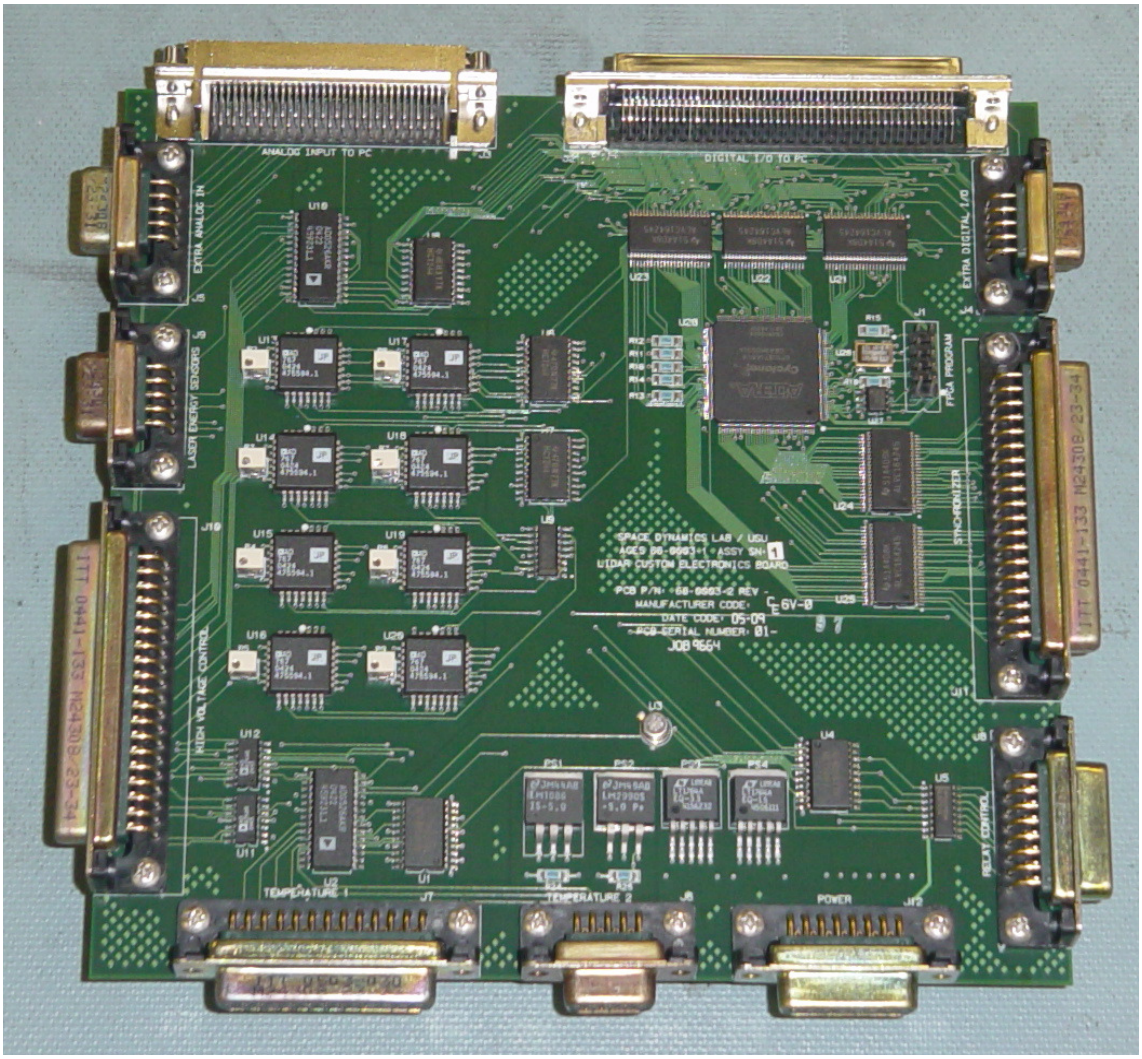

Fig. 3.8: Photograph of the completed custom electronics board.

the sensitive signals. In general, the board is slightly over-designed with regard to dimensioning in order to provide physical robustness. The final design of the PCB is a six layer board using 1 oz. copper. The top and bottom layers are the signal layers and the inner four are power planes. The planes are all split except for the digital ground plane. In designing the planes, the potential for capacitive coupling was considered between the digital planes (+5, +3.3, +1.5, DGND) and analog planes (+15, -15, AGND) and they were laid out to minimize the possibility of interference. Overall, every reasonable precaution was taken to ensure signal integrity on the board. A photograph of the completed board is shown in fig. 3.8.

2) *Custom Electronics Enclosure Layout*: The custom electronics enclosure is a rackmount enclosure custom made to house the electronics board, the DC power supplies, the high voltage power supplies, and the relays. Basically, this provides a housing for all the components that are not already contained in their own rackmount enclosure. The enclosure is designed to fit in a 2U height (3.5 inches) in a standard 19-inch wide rack. The layout description given here is only a plan for designing the actual enclosure. That design is being performed by one of the mechanical engineers on the project. A diagram showing the layout is shown in fig. 3.9. All of the components are drawn to scale for an accurate conceptualization of the available space.

The enclosure layout diagram shows three different views. The first is a top view looking down into the enclosure with the rear of the enclosure at the top. The custom electronics board is positioned flush with the back panel for the PCI card connections. Space is left around the perimeter of the board for the other cables that will be routed around the board. The two high voltage power supplies are in the lower left corner which

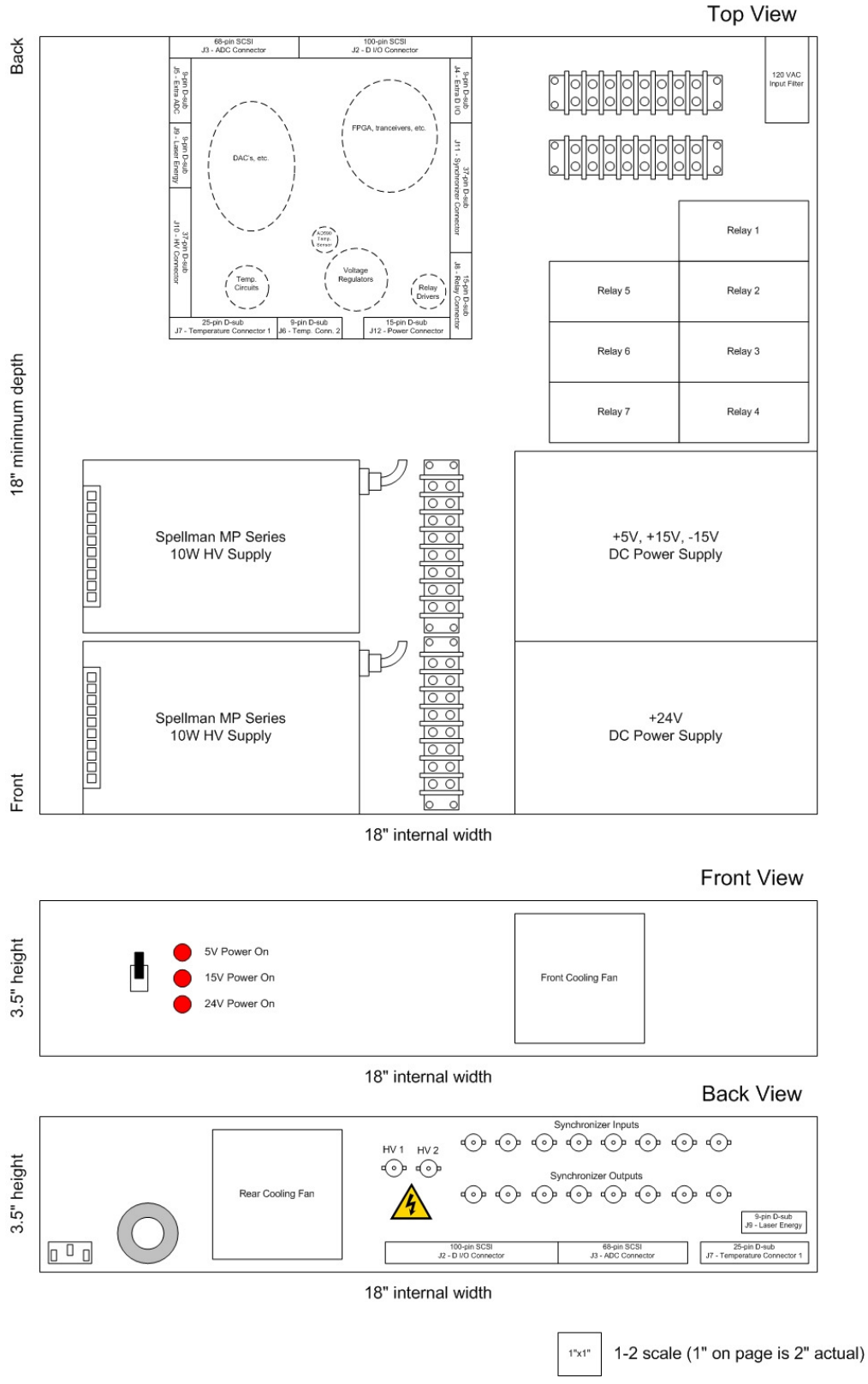

Fig. 3.9: Custom electronics enclosure layout.

is also very near to the high voltage control connector on the custom board. Next to these, in the lower right corner, are the DC power supplies. These are positioned horizontally for good ventilation. The power supplies specify an airflow direction normal to the longest dimension; otherwise, the airflow has no significant cooling effect. Note that there is a pair of fans in the front and rear panels to provide this airflow. The DC power supplies will terminate their output at sets of screw terminals in the center of the enclosure. This allows an easy junction for splitting the power to the appropriate devices. The final set of devices in the enclosure is the group of relays positioned in the upper right. The coils for these relays are all connected to the custom board but their switching terminals are routed to the rear panel to be attached to an arbitrary supply voltage and load.

The second view on the enclosure layout diagram shows the front panel of the enclosure. This panel contains a simple switch for turning on/off the AC input power to the power supplies and a power indicator light. The only other feature on the front panel is an air intake fan. The rear panel is shown in the third view. This panel contains all of the interconnection points to interface the enclosure contents to the rest of the instrument. It also contains another fan to provide an outlet for the cooling air. The first connector is an AC input plug to power the DC supplies. Next, a terminal strip provides the external connections for the relays. On the right-hand side of the panel are the connections to the custom board. Across the bottom are the two connectors that go to the embedded computer. To the right of these are D-sub connectors that are merely extensions of the connectors on the board for the temperature sensors and the laser energy sensors. Above these are 16 BNC connectors for the timing signals that interface to the synchronizer.

Internal to the enclosure, these all branch directly off of the D-sub connector on the custom board. Lastly, two high voltage BNC connections provide a terminal for the output of the high voltage power supplies. These outputs are transmitted over high voltage cables to the instrument.

3) *Rack Space Organization*: The last part of the electronics layout is the rack organization. The modules included in the main rack are the embedded computer, the custom enclosure, the photon counting data system, the laser controller, the motion controller, and a monitor/mouse/keyboard module. All together, these modules comprise 14U or 24.5 inches of rack space and require a rack depth of 24 inches. Housed in a separate module is the laser cooler which is 4U (7 inches) in height. The racks chosen for these components are shock absorbent portable racks made by SKB. These were chosen due to the nature of the deployment of the AGLITE instrument. It will likely be transported either by freight or in a custom trailer over long distances. This requires a robust enclosure that can protect the electronics from vibration. Figure 3.10 shows the likely arrangement of the modules in the rack. It also specifies the rack sizes of the proposed phase 2 hardware additions.

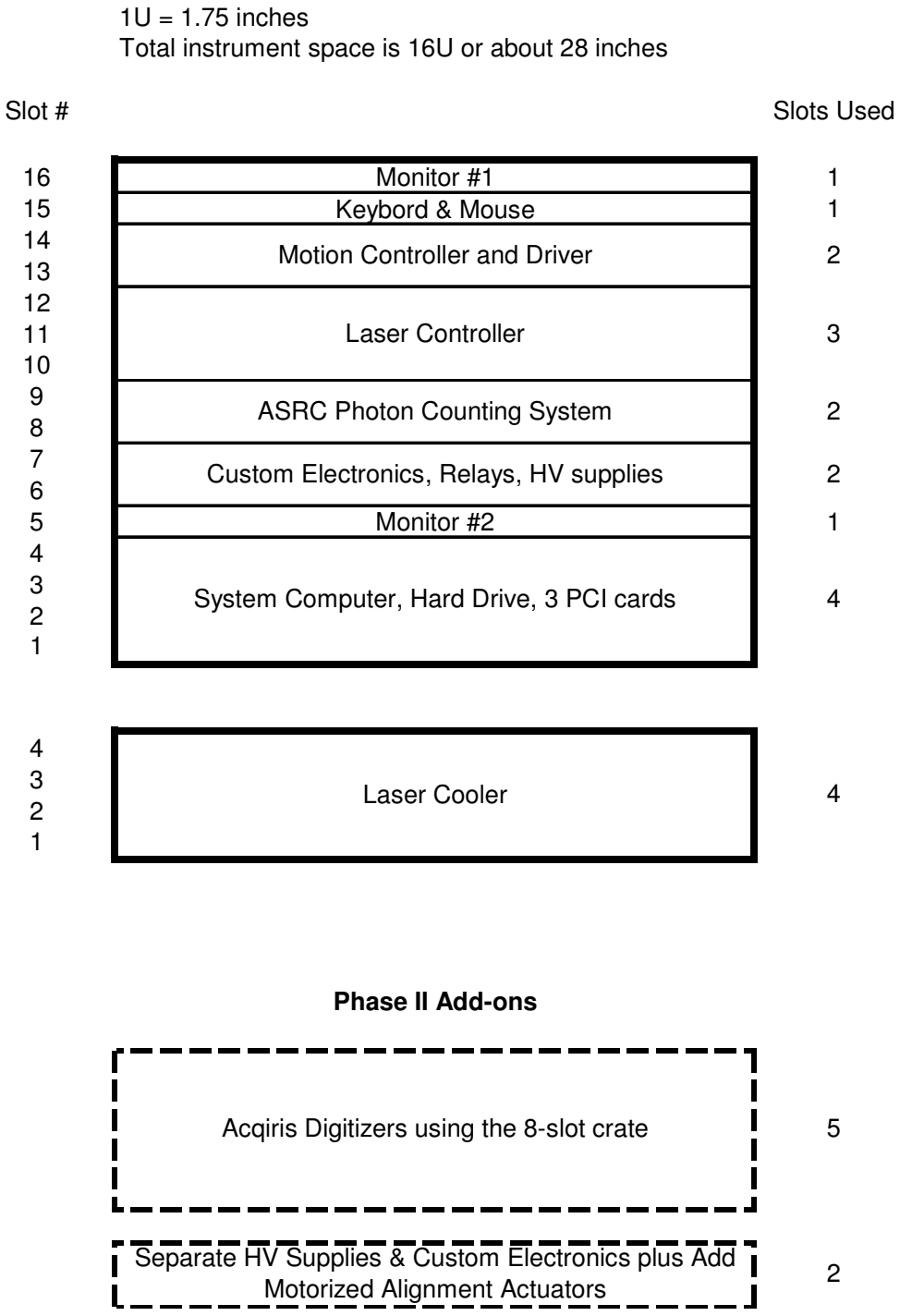

Fig. 3.10: Rack space utilization.

CHAPTER 4

CONCLUSIONS

The design of the AGLITE electronics system has been a challenging and diverse project. The design of this system drew on experience gleaned from work with other lidar systems and in many ways is a representation of their best features and proven approaches. Conversely, experience has also led to the improvement of things found lacking in other systems. Presently, the design work on the electronics system of the AGLITE instrument is complete and the project is moving rapidly into the assembly, test, and calibration stages. Assembly and test is expected to be completed in April 2005 and calibration will likely extend for many months after that.

This project is somewhat unique compared to many engineering designs in that there were very few initial specifications and the final product was not clearly defined or known at the outset. This is a direct result of the experimental nature of the instrument's mission. Even with the completion of the design, the future applications and possible additions to the instrument are the subject of continued discussion. Perhaps the strongest feature of the electronics design is its versatility and expandability to meet the needs of those applications. Accommodations have been put in place for all the foreseeable additions to the system with some allowance for even the unforeseen additions. It is very likely that in the next several years of development and experimentation, many of these additions will be implemented. Eventually, if the AGLITE instrument is able to deliver the meaningful data for which it is designed, many more similar instruments may be built. The electronics design, as it presently stands, will continue to facilitate these future

plans for years to come.

This design also represents another step in a trend in lidar technology towards compact, remotely operable, turnkey instruments. This trend has been facilitated by advances in laser and detector technology, computer electronics, and a general maturing of the lidar industry, making specialized lidar electronics and components more readily available and less expensive. With these advances, the implementation of airborne and spaceborne lidar systems is becoming more realistic. The AGLITE electronics system has an architecture that could easily be adapted to a very compact and portable form in future designs where the precise system specifications were known and the need for expandability did not exist. The biggest change would be the replacement of the embedded computer with an SBC (single-board computer) that had built-in digital and analog I/O and just enough peripheral ports to accommodate the essential hardware. The photon counting data acquisition system and the custom electronics could be removed from their chasses and, without modification, be stacked with the SBC. This would result in a complete and powerful electronics core the size of a small shoebox. Even without the miniaturization of the other peripheral electronics such as the laser controller and the beam steering controller, the entire electronics package could be compacted to an easily manageable size for airborne deployment. This type of layout would also be very practical in the 'production' model of the AGLITE if it reaches that point in the future.

REFERENCES

The references listed here provide information on several topics. First, references are given to other lidar systems (HARLIE and AROL) that were used as a starting point in the design of the AGLITE system. Hands-on experience with these systems inspired many of the features of the new lidar. The other publications and texts are given as a general reference to the design of lidar systems. These provide examples of other lidar projects, such as the Cloud Physics Lidar, whose purpose is similar to AGLITE, namely to design a powerful yet compact and efficient atmospheric lidar instrument.

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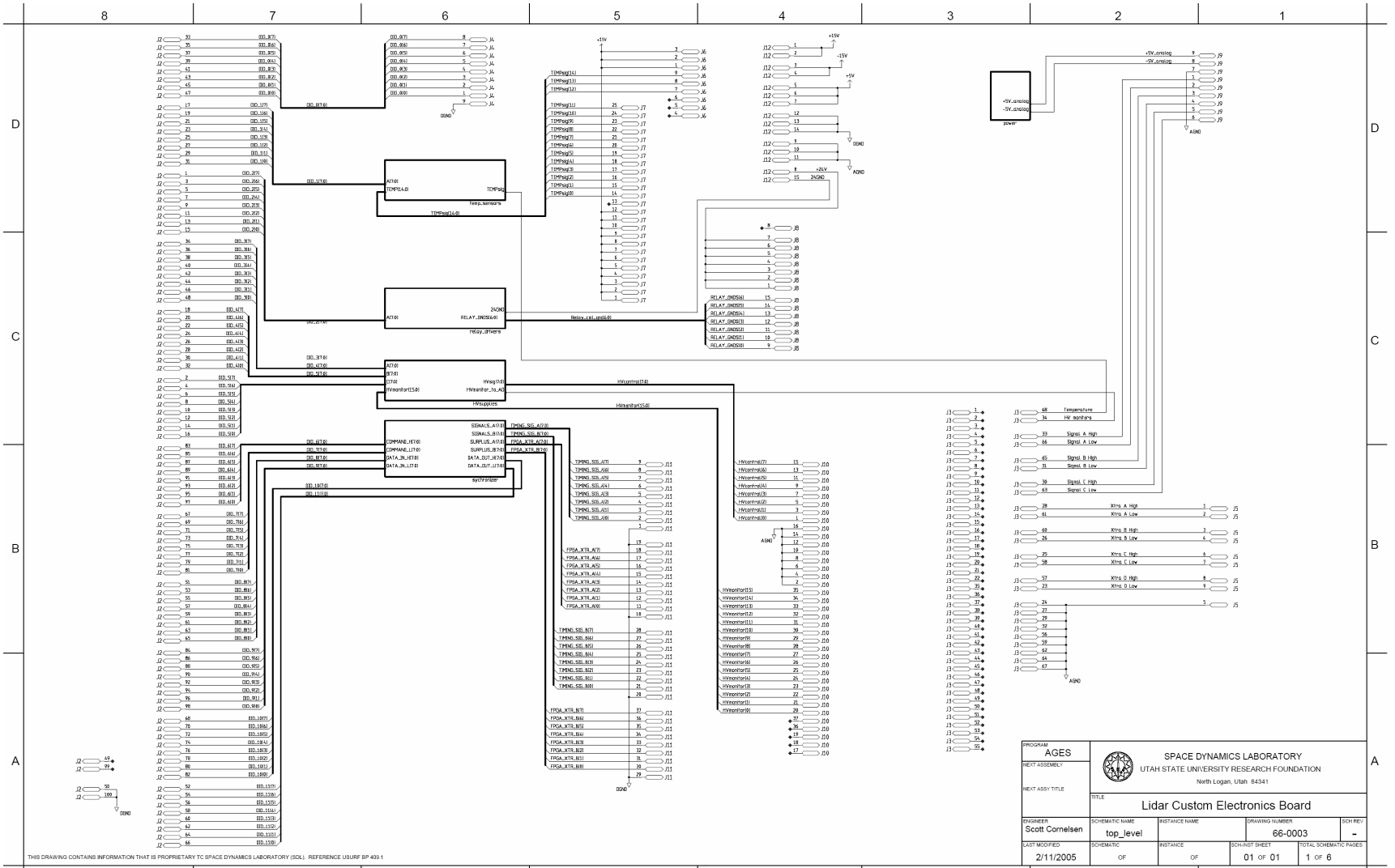
APPENDICES

APPENDIX A

CIRCUIT SCHEMATICS

The schematics for the custom electronics board were produced using Mentor Graphics. They are contained on six sheets including a top-level schematic that shows the other five schematics depicted as blocks in the top level. The other blocks, in the order shown here, are the power circuit, the high voltage controller, the temperature sensors, the synchronizer, and the relay drivers.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relay_drivers
HVsupplies
synchronizer
power
Lidar Custom Electronics Board
SPACE DYNAMICS LABORATORY
UTAH STATE UNIVERSITY RESEARCH FOUNDATION
North Logan, Utah 84341
PROGRAM AGES
NEXT ASSEMBLY
NEXT ASSY TITLE
ENGINEER Scott Cornelsen
SCHEMATIC NAME top_level
INSTANCE NAME
DRAWING NUMBER 66-0003
SCH REV -
LAST MODIFIED 2/11/2005
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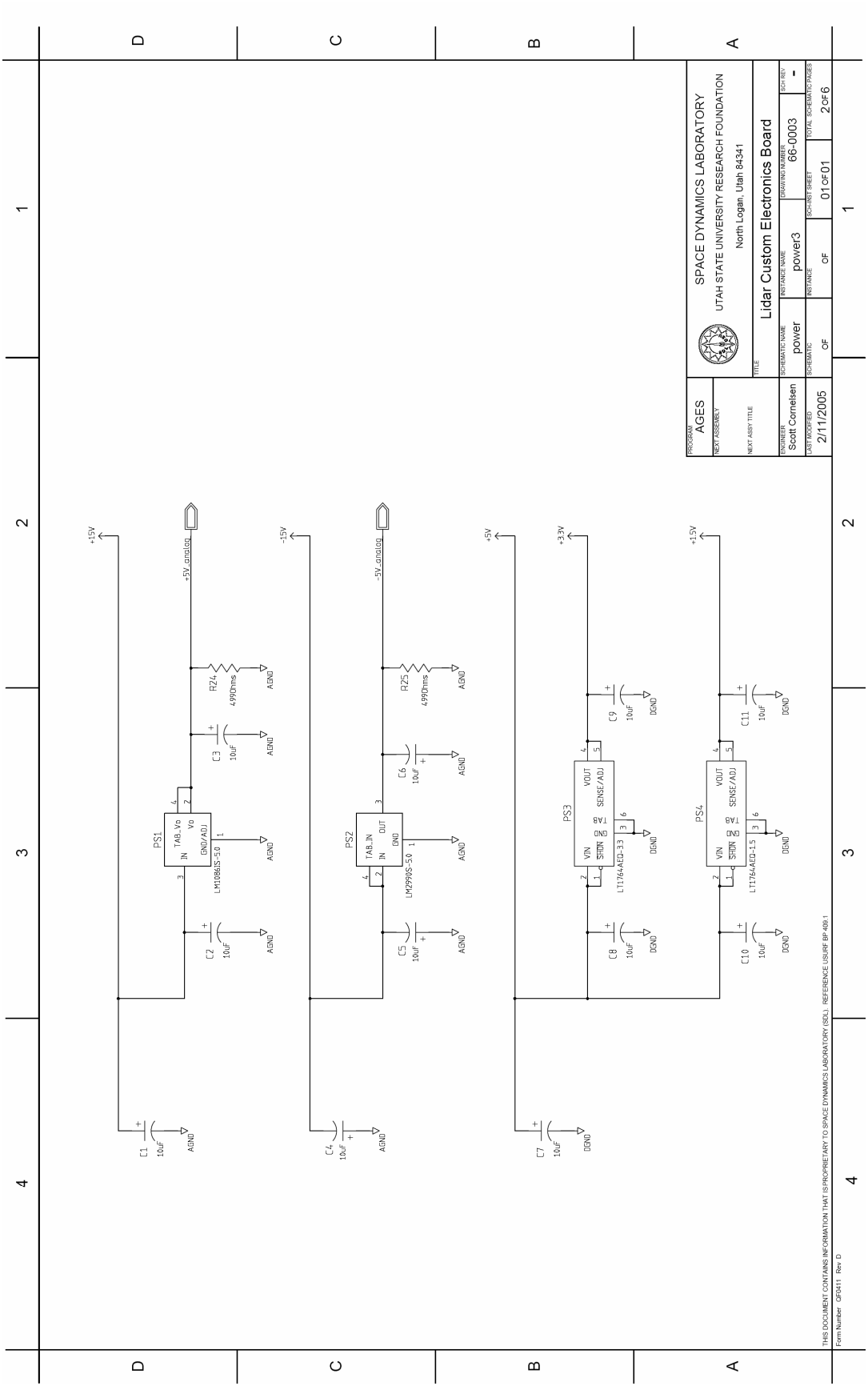
INSTANCE OF
SCH-INST SHEET 01 OF 01
TOTAL SCHEMATIC PAGES 1 OF 6
THIS DRAWING CONTAINS INFORMATION THAT IS PROPRIETARY TO SPACE DYNAMICS LABORATORY (SDL). REFERENCE USURF BP 409.1
Form No. QF0412 Rev D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UTAH STATE UNIVERSITY RESEARCH FOUNDATION
North Logan, Utah 84341
Lidar Custom Electronics Board
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NEXT ASSY TITLE
ENGINEER Scott Cornelsen
LAST MODIFIED 2/11/2005
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INSTANCE NAME power3
SCHEMATIC OF
INSTANCE OF
DRAWING NUMBER 66-0003
SCH REV -
SCH/SHT SHEET 01OF01
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PS1
LM1086CS-5.0
PS2
LM2990S-5.0
PS3
LT1764AEQ-3.3
PS4
LT1764AEQ-1.5
+15V
-15V
+5V
+3.3V
+5V_analog
-5V_analog
AGND
DGND
R24 499Ohms
R25 499Ohms
C1 10uF
C2 10uF
C3 10uF
C4 10uF
C5 10uF
C6 10uF
C7 10uF
C8 10uF
C9 10uF
C10 10uF
C11 10uF
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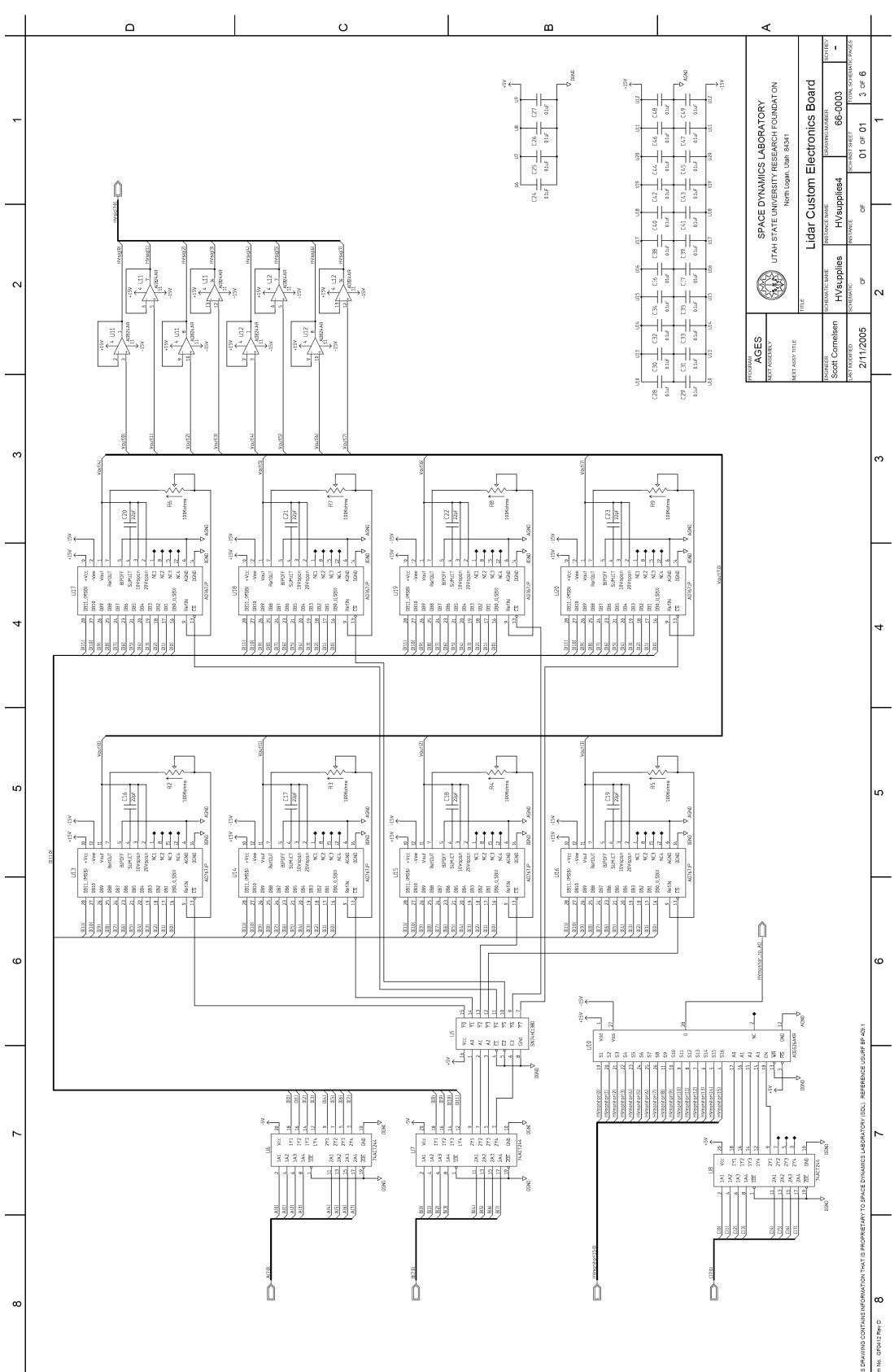
Form Number GP0411 Rev D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NEXT ASSEMBLY
NEXT ASSY TITLE
SPACE DYNAMICS LABORATORY
UTAH STATE UNIVERSITY RESEARCH FOUNDATION
North Logan, Utah 84341
TITLE
Lidar Custom Electronics Board
DRAWN BY
Scott Cornelsen
SCHEMATIC NAME
HVsupplies
INSTANCE NAME
HVsupplies4
DRAWING NUMBER
66-0003
REVISION
-
ART RELEASED
2/11/2005
SCHEMATIC
OF
INSTANCE
OF
SCHEMATIC SHEET
01 OF 01
TOTAL SCHEMATIC PAGES
3 OF 6
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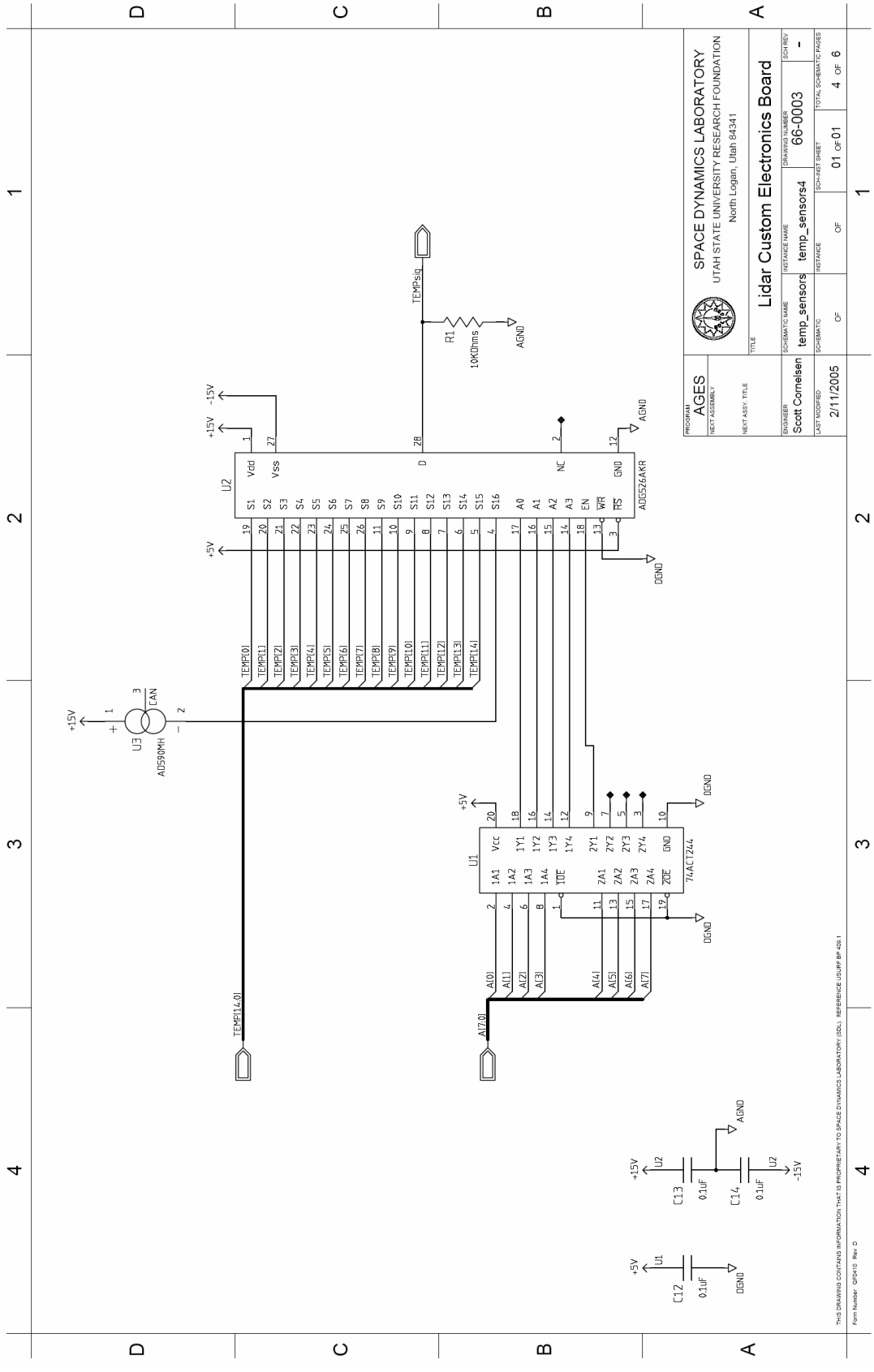
SPACE DYNAMICS LABORATORY
UTAH STATE UNIVERSITY RESEARCH FOUNDATION
North Logan, Utah 84341
Lidar Custom Electronics Board
PROGRAM AGES
ENGINEER Scott Cornelsen
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INSTANCE NAME temp_sensors4
DRAWING NUMBER 66-0003
SCH REV -
SCHEMATIC OF
INSTANCE OF
SCH-INST SHEET 01 OF 01
TOTAL SCHEMATIC PAGES 4 OF 6
U2 AD5526AKR
U1 74ACT244
U3 AD590MH
R1 10KOhms
C12 0.1uF
C13 0.1uF
C14 0.1uF
+5V
+15V
-15V
AGND
DGND
TEMPsig
TEMP[14..0]
A[7..0]
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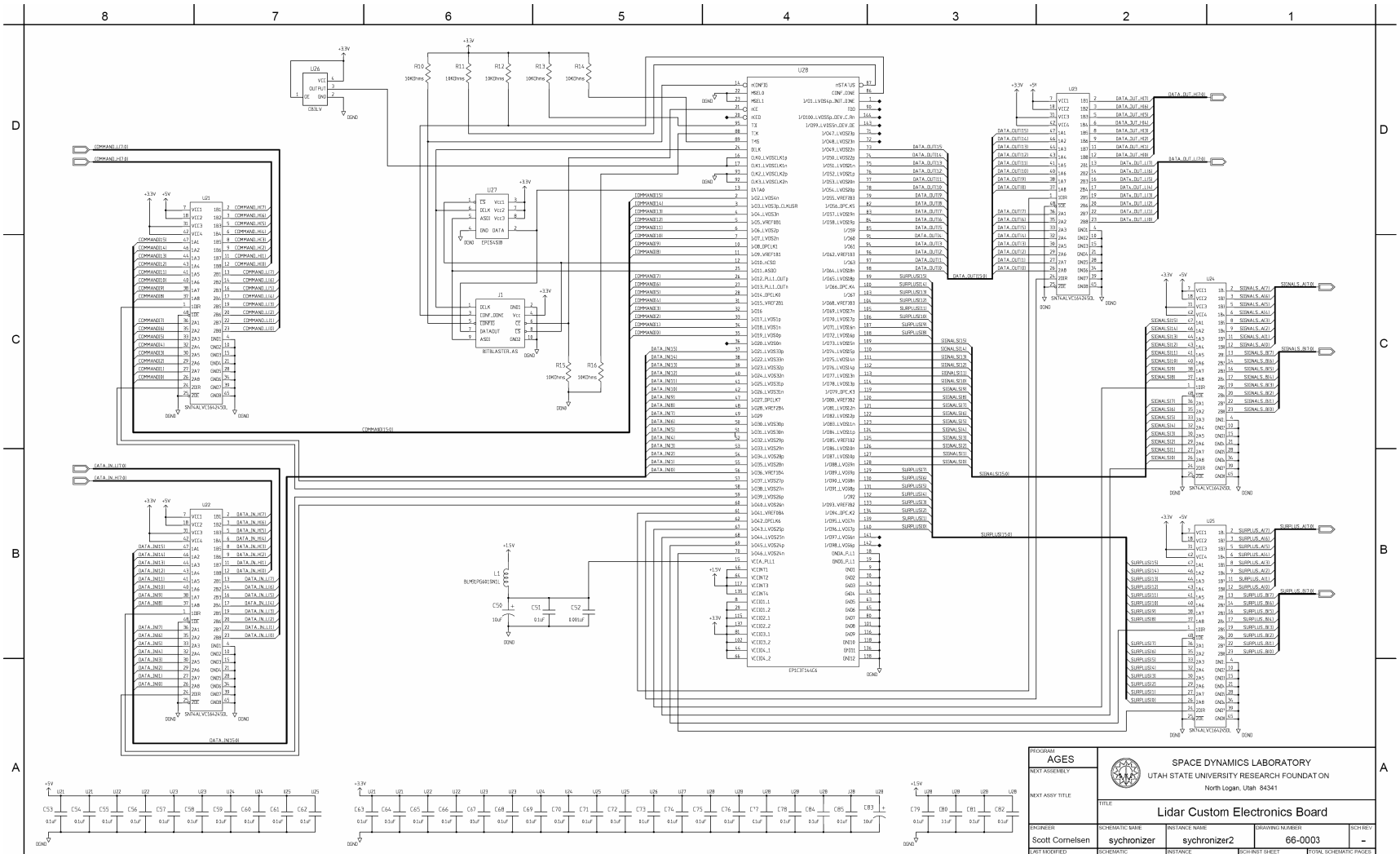
Form Number: QP410 Rev: D



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INSTANCE NAME	sychronizer2
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INSTANCE	OF
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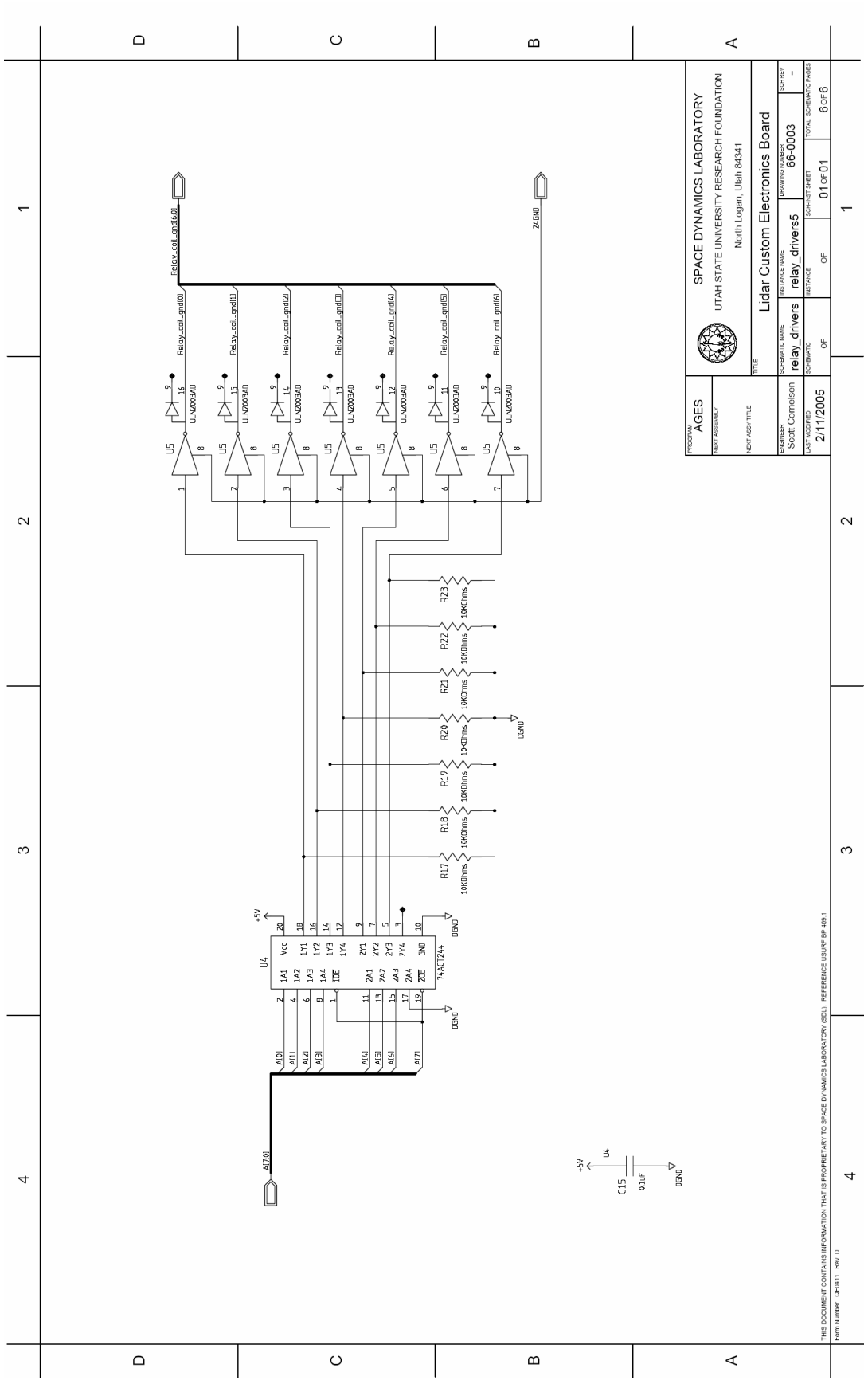
SPACE DYNAMICS LABORATORY
UTAH STATE UNIVERSITY RESEARCH FOUNDATION
North Logan, Utah 84341
Lidar Custom Electronics Board
PROGRAM AGES
NEXT ASSEMBLY
NEXT ASSY TITLE
TITLE
ENGINEER Scott Cornelsen
LAST MODIFIED 2/11/2005
SCHEMATIC NAME relay_drivers
SCHEMATIC OF
NEXT ASSY OF
PATHNAME relay_drivers5
DRAWING NUMBER 66-0003
SCH SHEET 01 OF 01
TOTAL SCHEMATIC PAGES 6 OF 6
SCH REV -
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Form Number GF0411 Rev D
ULN2003AD
74ACT244
R17 10KOhms
R18 10KOhms
R19 10KOhms
R20 10KOhms
R21 10KOhms
R22 10KOhms
R23 10KOhms
C15 0.1uF
+5V
DGND
Z4GND
Relay_coil_gnd[0..7]
A1[7..0]

APPENDIX B

PARTS LIST

This is a complete list of all the parts used on the schematics in appendix A. The reference designators listed here correlate to those shown in the schematics.

PARTS LIST

TITLE: AGES Lidar Custom Electronics Board

DRAWING NO: 3 | PL REVISION: | ASSEMBLY NO: 66-0003-1

SPACE DYNAMICS LABORATORY
USU RESEARCH FOUNDATION
North Logan, Utah 84341

Item	Qty	Part Number	Description	Reference Designator
1	1	66-0003-2	AGES Lidar Custom Electronics Board	
2	2	ADG526AKR	16 Channel Mux	U2,U10
3	1	AD590MH	Temperature Transducer	U3
4	8	AD767JP	12-bit A/D Concerter	U13-U20
5	2	AD824AR	Precision Op Amp	U11-U12
6	1	BITBLASTER_AS	10 Pin Double Row Connector	J1
7	1	BLM31PG601SN1L	600 Ohm 1.5 A Ferrite Bead	L1
8	1	CB3LV-3C-50.0000	LCC Oscillator	U26
9	1	EPCS4SI8	Configuration PROM	U27
10	1	EP1C3T144C6	FPGA Commercial Temp	U28
11	1	LM1086IS-5.0	1.5 Amp 5V Regulator	PS1
12	1	LM2990S-5.0	-5V 1 Amp Regulator	PS2
13	1	LT1764AEQ-1.5	1.5V 3A Regulator	PS4
14	1	LT1764AEQ-3.3	3.3V 3A Regulator	PS3
15	15	RK73H2B1002F	10.0K Ohm 250mW Resistor	R1,R10-R23
16	2	RK73H2B4990F	499 Ohm 250mW Resistor	R24-R25
17	4	SND9F5R700G	9-pin Right Angle Receptical	J4-J6,J9
18	2	SND15F5R700G	15-pin Right Angle Receptical	J8,J12
19	1	SND25F5R700G	25-pin Right Angle Receptical	J7
20	2	SND37F5R700G	37-pin Right Angle Receptical	J10-J11
21	5	SN74ALVC164245DL	16-bit Bus Transceiver	U21-U25
22	5	SN74HCT244DW	CMOS Octal Tri-State Buffer	U1,U4,U6-U8
23	1	SN74HC138D	Inverting 3 to 8 Decoder/Demux	U9
24	13	TAJC106K035R	10uF 35V Tantalum Cap	C1-C11,C50,C83
25	1	ULN2003AD	Darlington Transistor Array	U5
26	8	3214W-1-101E	100 OHM Trimmer Resistor	R2-R9
27	63	12061C104KAT2A	.1uF 100V X7R Capacitor	C12-C15,C24-C49,C51,C53-C82,C84-C85
28	8	12065A220JAT2A	22pF 50V NPO Capacitor	C16-C23
29	1	12065C102KAT2A	1000pF 50V X7R Capacitor	C52
30	1	174225-5	68 pin Right Angle Plug	J3
31	1	787169-9	Right Angle Receptical	J2
32	18	MS51957-13	SCREW, Pan Head Phillips #4-40 x1/4	Use with items 17,18,19 & 20
33	4	MS51957-3	SCREW, Pan Head Phillips #2-56 x1/4	Use with items 30 & 31
34	AR	SN63-285/66	Solder, Kester	
35	AR	6-SN63-287-H	Solder Paste	

APPENDIX C

FPGA PIN LISTING

FPGA Assignment			External Assignment	
Pin #	Pin Name/Function	Bank	Bus Name	Net #
1	I/O1_INIT_DONE	A	-	
2	I/O2	A	Command_H	7
3	I/O3	A	Command_H	6
4	I/O4	A	Command_H	5
5	I/O5	A	Command_H	4
6	I/O6	A	Command_H	3
7	I/O7	A	Command_H	2
8	VCCIO1_1		-	
9	GND1		-	
10	I/O8	A	Command_H	1
11	I/O9	A	Command_H	0
12	I/O10_nCSO	A	-	
13	DATA0		-	
14	nCONFIG		-	
15	VCCA_PLL1		-	
16	CLK0		-	
17	CLK1		-	
18	GNDA_PLL1		-	
19	GNDG_PLL2		-	
20	nCEO		-	
21	nCE		-	
22	MSEL0		-	
23	MSEL1		-	
24	DCLK		-	
25	I/O11_ASD0	A	-	
26	I/O12	A	Command_L	7
27	I/O13	A	Command_L	6
28	I/O14	A	Command_L	5
29	VCCIO1_2		-	
30	GND2		-	
31	I/O15	A	Command_L	4
32	I/O16	A	Command_L	3
33	I/O17	A	Command_L	2
34	I/O18	A	Command_L	1
35	I/O19	A	Command_L	0
36	I/O20	A	-	
37	I/O21	B	DataIn_H	7
38	I/O22	B	DataIn_H	6
39	I/O23	B	DataIn_H	5
40	I/O24	B	DataIn_H	4
41	I/O25	B	DataIn_H	3
42	I/O26	B	DataIn_H	2
43	GND3		-	
44	VCCIO4_1		-	
45	GND4		-	
46	VCCINT1		-	
47	I/O27	B	DataIn_H	1

FPGA Assignment			External Assignment	
Pin #	Pin Name/Function	Bank	Bus Name	Net #
48	I/O28	B	DataIn_H	0
49	I/O29	B	DataIn_L	7
50	I/O30	B	DataIn_L	6
51	I/O31	B	DataIn_L	5
52	I/O32	B	DataIn_L	4
53	I/O33	B	DataIn_L	3
54	I/O34	B	DataIn_L	2
55	I/O35	B	DataIn_L	1
56	I/O36	B	DataIn_L	0
57	I/O37	B	DIR_Comm_H	-
58	I/O38	B	DIR_Comm_L	-
59	I/O39	B	DIR_Din_H	-
60	I/O40	B	DIR_Din_L	-
61	I/O41	B	DIR_Dout_H	-
62	I/O42	B	DIR_Dout_L	-
63	GND5		-	
64	VCCINT2		-	
65	GND6		-	
66	VCCIO4_2		-	
67	I/O43	B	DIR_Sig_A	-
68	I/O44	B	DIR_Sig_B	-
69	I/O45	B	DIR_Surp_A	-
70	I/O46	B	DIR_Surp_B	-
71	I/O47	B	-	
72	I/O48	B	-	
73	I/O49	C	DataOut_H	7
74	I/O50	C	DataOut_H	6
75	I/O51	C	DataOut_H	5
76	I/O52	C	DataOut_H	4
77	I/O53	C	DataOut_H	3
78	I/O54	C	DataOut_H	2
79	I/O55	C	DataOut_H	1
80	GND7		-	
81	VCCIO3_1		-	
82	I/O56	C	DataOut_H	0
83	I/O57	C	DataOut_L	7
84	I/O58	C	DataOut_L	6
85	I/O59	C	DataOut_L	5
86	CONF_DONE		-	
87	nSTATUS		-	
88	TCK		-	
89	TMS		-	
90	TDO		-	
91	I/O60	C	DataOut_L	4
92	CKL3		-	
93	CLK2		-	
94	I/O61	C	DataOut_L	3
95	TDI		-	
96	I/O62	C	DataOut_L	2
97	I/O63	C	DataOut_L	1

FPGA Assignment			External Assignment	
Pin #	Pin Name/Function	Bank	Bus Name	Net #
98	I/O64	C	DataOut_L	0
99	I/O65	C	Surplus_A	7
100	I/O66	C	Surplus_A	6
101	GND8		-	
102	VCCIO3_2		-	
103	I/O67	C	Surplus_A	5
104	I/O68	C	Surplus_A	4
105	I/O69	C	Surplus_A	3
106	I/O70	C	Surplus_A	2
107	I/O71	C	Surplus_A	1
108	I/O72	C	Surplus_A	0
109	I/O73	D	Signals_A	7
110	I/O74	D	Signals_A	6
111	I/O75	D	Signals_A	5
112	I/O76	D	Signals_A	4
113	I/O77	D	Signals_A	3
114	I/O78	D	Signals_A	2
115	VCCIO2_1		-	
116	GND9		-	
117	VCCINT3		-	
118	GND10		-	
119	I/O79	D	Signals_A	1
120	I/O80	D	Signals_A	0
121	I/O81	D	Signals_B	7
122	I/O82	D	Signals_B	6
123	I/O83	D	Signals_B	5
124	I/O84	D	Signals_B	4
125	I/O85	D	Signals_B	3
126	I/O86	D	Signals_B	2
127	I/O87	D	Signals_B	1
128	I/O88	D	Signals_B	0
129	I/O89	D	Surplus_B	7
130	I/O90	D	Surplus_B	6
131	I/O91	D	Surplus_B	5
132	I/O92	D	Surplus_B	4
133	I/O93	D	Surplus_B	3
134	I/O94	D	Surplus_B	2
135	VCCINT4		-	
136	GND11		-	
137	VCCIO2_2		-	
138	GND12		-	
139	I/O95	D	Surplus_B	1
140	I/O96	D	Surplus_B	0
141	I/O97	D	-	
142	I/O98	D	-	
143	I/O99_DEV_OE	D	-	
144	I/O100_DEV_CLRn	D	-	

APPENDIX D

CABLE PIN LISTINGS

The following chart documents every pin for the connectors found on the custom electronics card. This includes the on-board and off-board connector information as well as details about the cable interconnection. This is used as a design guide for the wire harness that will be built for all of the custom electronics.

AGLITE Electronics Board Cable Connection List

On-Board Connector				Cable					Off-Board Connector		
Designation	Connector Type	M/F	Pin #	Function	Wire Type	Pair Pin	Shield	Color	Connector Type	M/F	Pin #
J2	SCSI - 100	F	1	DIO 2.7	ready-made	-		N/A	D I/O Card		1
J2	SCSI - 100	F	2	DIO 5.7	ready-made	-		N/A	D I/O Card		2
J2	SCSI - 100	F	3	DIO 2.6	ready-made	-		N/A	D I/O Card		3
J2	SCSI - 100	F	4	DIO 5.6	ready-made	-		N/A	D I/O Card		4
J2	SCSI - 100	F	5	DIO 2.5	ready-made	-		N/A	D I/O Card		5
J2	SCSI - 100	F	6	DIO 5.5	ready-made	-		N/A	D I/O Card		6
J2	SCSI - 100	F	7	DIO 2.4	ready-made	-		N/A	D I/O Card		7
J2	SCSI - 100	F	8	DIO 5.4	ready-made	-		N/A	D I/O Card		8
J2	SCSI - 100	F	9	DIO 2.3	ready-made	-		N/A	D I/O Card		9
J2	SCSI - 100	F	10	DIO 5.3	ready-made	-		N/A	D I/O Card		10
J2	SCSI - 100	F	11	DIO 2.2	ready-made	-		N/A	D I/O Card		11
J2	SCSI - 100	F	12	DIO 5.2	ready-made	-		N/A	D I/O Card		12
J2	SCSI - 100	F	13	DIO 2.1	ready-made	-		N/A	D I/O Card		13
J2	SCSI - 100	F	14	DIO 5.2	ready-made	-		N/A	D I/O Card		14
J2	SCSI - 100	F	15	DIO 2.0	ready-made	-		N/A	D I/O Card		15
J2	SCSI - 100	F	16	DIO 5.0	ready-made	-		N/A	D I/O Card		16
J2	SCSI - 100	F	17	DIO 1.7	ready-made	-		N/A	D I/O Card		17
J2	SCSI - 100	F	18	DIO 4.7	ready-made	-		N/A	D I/O Card		18
J2	SCSI - 100	F	19	DIO 1.6	ready-made	-		N/A	D I/O Card		19
J2	SCSI - 100	F	20	DIO 4.6	ready-made	-		N/A	D I/O Card		20
J2	SCSI - 100	F	21	DIO 1.5	ready-made	-		N/A	D I/O Card		21
J2	SCSI - 100	F	22	DIO 4.5	ready-made	-		N/A	D I/O Card		22
J2	SCSI - 100	F	23	DIO 1.4	ready-made	-		N/A	D I/O Card		23
J2	SCSI - 100	F	24	DIO 4.4	ready-made	-		N/A	D I/O Card		24
J2	SCSI - 100	F	25	DIO 1.3	ready-made	-		N/A	D I/O Card		25
J2	SCSI - 100	F	26	DIO 4.3	ready-made	-		N/A	D I/O Card		26
J2	SCSI - 100	F	27	DIO 1.2	ready-made	-		N/A	D I/O Card		27
J2	SCSI - 100	F	28	DIO 4.2	ready-made	-		N/A	D I/O Card		28
J2	SCSI - 100	F	29	DIO 1.1	ready-made	-		N/A	D I/O Card		29
J2	SCSI - 100	F	30	DIO 4.1	ready-made	-		N/A	D I/O Card		30
J2	SCSI - 100	F	31	DIO 1.0	ready-made	-		N/A	D I/O Card		31
J2	SCSI - 100	F	32	DIO 4.0	ready-made	-		N/A	D I/O Card		32
J2	SCSI - 100	F	33	DIO 0.7	ready-made	-		N/A	D I/O Card		33
J2	SCSI - 100	F	34	DIO 3.7	ready-made	-		N/A	D I/O Card		34
J2	SCSI - 100	F	35	DIO 0.6	ready-made	-		N/A	D I/O Card		35
J2	SCSI - 100	F	36	DIO 3.6	ready-made	-		N/A	D I/O Card		36
J2	SCSI - 100	F	37	DIO 0.5	ready-made	-		N/A	D I/O Card		37
J2	SCSI - 100	F	38	DIO 3.5	ready-made	-		N/A	D I/O Card		38
J2	SCSI - 100	F	39	DIO 0.4	ready-made	-		N/A	D I/O Card		39
J2	SCSI - 100	F	40	DIO 3.4	ready-made	-		N/A	D I/O Card		40
J2	SCSI - 100	F	41	DIO 0.3	ready-made	-		N/A	D I/O Card		41
J2	SCSI - 100	F	42	DIO 3.3	ready-made	-		N/A	D I/O Card		42
J2	SCSI - 100	F	43	DIO 0.2	ready-made	-		N/A	D I/O Card		43
J2	SCSI - 100	F	44	DIO 3.2	ready-made	-		N/A	D I/O Card		44
J2	SCSI - 100	F	45	DIO 0.1	ready-made	-		N/A	D I/O Card		45
J2	SCSI - 100	F	46	DIO 3.1	ready-made	-		N/A	D I/O Card		46
J2	SCSI - 100	F	47	DIO 0.0	ready-made	-		N/A	D I/O Card		47
J2	SCSI - 100	F	48	DIO 3.0	ready-made	-		N/A	D I/O Card		48
J2	SCSI - 100	F	49	DIO +5V	ready-made	-		N/A	D I/O Card		49
J2	SCSI - 100	F	50	DIO GND	ready-made	-		N/A	D I/O Card		50
J2	SCSI - 100	F	51	DIO 8.7	ready-made	-		N/A	D I/O Card		51
J2	SCSI - 100	F	52	DIO 11.7	ready-made	-		N/A	D I/O Card		52
J2	SCSI - 100	F	53	DIO 8.6	ready-made	-		N/A	D I/O Card		53
J2	SCSI - 100	F	54	DIO 11.6	ready-made	-		N/A	D I/O Card		54

On-Board Connector				Cable					Off-Board Connector		
Designation	Connector Type	M/F	Pin #	Function	Wire Type	Pair Pin	Shield	Color	Connector Type	M/F	Pin #
J2	SCSI - 100	F	55	DIO 8.5	ready-made	-		N/A	D I/O Card		55
J2	SCSI - 100	F	56	DIO 11.5	ready-made	-		N/A	D I/O Card		56
J2	SCSI - 100	F	57	DIO 8.4	ready-made	-		N/A	D I/O Card		57
J2	SCSI - 100	F	58	DIO 11.4	ready-made	-		N/A	D I/O Card		58
J2	SCSI - 100	F	59	DIO 8.3	ready-made	-		N/A	D I/O Card		59
J2	SCSI - 100	F	60	DIO 11.3	ready-made	-		N/A	D I/O Card		60
J2	SCSI - 100	F	61	DIO 8.2	ready-made	-		N/A	D I/O Card		61
J2	SCSI - 100	F	62	DIO 11.2	ready-made	-		N/A	D I/O Card		62
J2	SCSI - 100	F	63	DIO 8.1	ready-made	-		N/A	D I/O Card		63
J2	SCSI - 100	F	64	DIO 11.1	ready-made	-		N/A	D I/O Card		64
J2	SCSI - 100	F	65	DIO 8.0	ready-made	-		N/A	D I/O Card		65
J2	SCSI - 100	F	66	DIO 11.0	ready-made	-		N/A	D I/O Card		66
J2	SCSI - 100	F	67	DIO 7.7	ready-made	-		N/A	D I/O Card		67
J2	SCSI - 100	F	68	DIO 10.7	ready-made	-		N/A	D I/O Card		68
J2	SCSI - 100	F	69	DIO 7.6	ready-made	-		N/A	D I/O Card		69
J2	SCSI - 100	F	70	DIO 10.6	ready-made	-		N/A	D I/O Card		70
J2	SCSI - 100	F	71	DIO 7.5	ready-made	-		N/A	D I/O Card		71
J2	SCSI - 100	F	72	DIO 10.5	ready-made	-		N/A	D I/O Card		72
J2	SCSI - 100	F	73	DIO 7.4	ready-made	-		N/A	D I/O Card		73
J2	SCSI - 100	F	74	DIO 10.4	ready-made	-		N/A	D I/O Card		74
J2	SCSI - 100	F	75	DIO 7.3	ready-made	-		N/A	D I/O Card		75
J2	SCSI - 100	F	76	DIO 10.3	ready-made	-		N/A	D I/O Card		76
J2	SCSI - 100	F	77	DIO 7.2	ready-made	-		N/A	D I/O Card		77
J2	SCSI - 100	F	78	DIO 10.2	ready-made	-		N/A	D I/O Card		78
J2	SCSI - 100	F	79	DIO 7.1	ready-made	-		N/A	D I/O Card		79
J2	SCSI - 100	F	80	DIO 10.1	ready-made	-		N/A	D I/O Card		80
J2	SCSI - 100	F	81	DIO 7.0	ready-made	-		N/A	D I/O Card		81
J2	SCSI - 100	F	82	DIO 10.0	ready-made	-		N/A	D I/O Card		82
J2	SCSI - 100	F	83	DIO 6.7	ready-made	-		N/A	D I/O Card		83
J2	SCSI - 100	F	84	DIO 9.7	ready-made	-		N/A	D I/O Card		84
J2	SCSI - 100	F	85	DIO 6.6	ready-made	-		N/A	D I/O Card		85
J2	SCSI - 100	F	86	DIO 9.6	ready-made	-		N/A	D I/O Card		86
J2	SCSI - 100	F	87	DIO 6.5	ready-made	-		N/A	D I/O Card		87
J2	SCSI - 100	F	88	DIO 9.5	ready-made	-		N/A	D I/O Card		88
J2	SCSI - 100	F	89	DIO 6.4	ready-made	-		N/A	D I/O Card		89
J2	SCSI - 100	F	90	DIO 9.4	ready-made	-		N/A	D I/O Card		90
J2	SCSI - 100	F	91	DIO 6.3	ready-made	-		N/A	D I/O Card		91
J2	SCSI - 100	F	92	DIO 9.3	ready-made	-		N/A	D I/O Card		92
J2	SCSI - 100	F	93	DIO 6.2	ready-made	-		N/A	D I/O Card		93
J2	SCSI - 100	F	94	DIO 9.2	ready-made	-		N/A	D I/O Card		94
J2	SCSI - 100	F	95	DIO 6.1	ready-made	-		N/A	D I/O Card		95
J2	SCSI - 100	F	96	DIO 9.1	ready-made	-		N/A	D I/O Card		96
J2	SCSI - 100	F	97	DIO 6.0	ready-made	-		N/A	D I/O Card		97
J2	SCSI - 100	F	98	DIO 9.0	ready-made	-		N/A	D I/O Card		98
J2	SCSI - 100	F	99	DIO +5V	ready-made	-		N/A	D I/O Card		99
J2	SCSI - 100	F	100	DIO GND	ready-made	-		N/A	D I/O Card		100
J3	SCSI - 68	M	1	NC - for digital use	ready-made	-		N/A	ADC Card		1
J3	SCSI - 68	M	2	NC - for digital use	ready-made	-		N/A	ADC Card		2
J3	SCSI - 68	M	3	NC - for digital use	ready-made	-		N/A	ADC Card		3
J3	SCSI - 68	M	4	NC - for digital use	ready-made	-		N/A	ADC Card		4
J3	SCSI - 68	M	5	NC - for digital use	ready-made	-		N/A	ADC Card		5
J3	SCSI - 68	M	6	NC - for digital use	ready-made	-		N/A	ADC Card		6
J3	SCSI - 68	M	7	NC - for digital use	ready-made	-		N/A	ADC Card		7
J3	SCSI - 68	M	8	NC - for digital use	ready-made	-		N/A	ADC Card		8
J3	SCSI - 68	M	9	NC - for digital use	ready-made	-		N/A	ADC Card		9

On-Board Connector				Cable					Off-Board Connector		
Designation	Connector Type	M/F	Pin #	Function	Wire Type	Pair Pin	Shield	Color	Connector Type	M/F	Pin #
J3	SCSI - 68	M	10	NC - for digital use	ready-made	-		N/A	ADC Card		10
J3	SCSI - 68	M	11	NC - for digital use	ready-made	-		N/A	ADC Card		11
J3	SCSI - 68	M	12	NC - for digital use	ready-made	-		N/A	ADC Card		12
J3	SCSI - 68	M	13	NC - for digital use	ready-made	-		N/A	ADC Card		13
J3	SCSI - 68	M	14	NC - for digital use	ready-made	-		N/A	ADC Card		14
J3	SCSI - 68	M	15	NC - for digital use	ready-made	-		N/A	ADC Card		15
J3	SCSI - 68	M	16	NC - for digital use	ready-made	-		N/A	ADC Card		16
J3	SCSI - 68	M	17	NC - for digital use	ready-made	-		N/A	ADC Card		17
J3	SCSI - 68	M	18	NC - for digital use	ready-made	-		N/A	ADC Card		18
J3	SCSI - 68	M	19	NC - for digital use	ready-made	-		N/A	ADC Card		19
J3	SCSI - 68	M	20	NC - for digital use	ready-made	-		N/A	ADC Card		20
J3	SCSI - 68	M	21	NC - for digital use	ready-made	-		N/A	ADC Card		21
J3	SCSI - 68	M	22	NC - for digital use	ready-made	-		N/A	ADC Card		22
J3	SCSI - 68	M	23	AI 15	ready-made	-		N/A	ADC Card		23
J3	SCSI - 68	M	24	AI GND	ready-made	-		N/A	ADC Card		24
J3	SCSI - 68	M	25	AI 6	ready-made	-		N/A	ADC Card		25
J3	SCSI - 68	M	26	AI 13	ready-made	-		N/A	ADC Card		26
J3	SCSI - 68	M	27	AI GND	ready-made	-		N/A	ADC Card		27
J3	SCSI - 68	M	28	AI 4	ready-made	-		N/A	ADC Card		28
J3	SCSI - 68	M	29	AI GND	ready-made	-		N/A	ADC Card		29
J3	SCSI - 68	M	30	AI 3	ready-made	-		N/A	ADC Card		30
J3	SCSI - 68	M	31	AI 10	ready-made	-		N/A	ADC Card		31
J3	SCSI - 68	M	32	AI GND	ready-made	-		N/A	ADC Card		32
J3	SCSI - 68	M	33	AI 1	ready-made	-		N/A	ADC Card		33
J3	SCSI - 68	M	34	AI 8	ready-made	-		N/A	ADC Card		34
J3	SCSI - 68	M	35	NC - for digital use	ready-made	-		N/A	ADC Card		35
J3	SCSI - 68	M	36	NC - for digital use	ready-made	-		N/A	ADC Card		36
J3	SCSI - 68	M	37	NC - for digital use	ready-made	-		N/A	ADC Card		37
J3	SCSI - 68	M	38	NC - for digital use	ready-made	-		N/A	ADC Card		38
J3	SCSI - 68	M	39	NC - for digital use	ready-made	-		N/A	ADC Card		39
J3	SCSI - 68	M	40	NC - for digital use	ready-made	-		N/A	ADC Card		40
J3	SCSI - 68	M	41	NC - for digital use	ready-made	-		N/A	ADC Card		41
J3	SCSI - 68	M	42	NC - for digital use	ready-made	-		N/A	ADC Card		42
J3	SCSI - 68	M	43	NC - for digital use	ready-made	-		N/A	ADC Card		43
J3	SCSI - 68	M	44	NC - for digital use	ready-made	-		N/A	ADC Card		44
J3	SCSI - 68	M	45	NC - for digital use	ready-made	-		N/A	ADC Card		45
J3	SCSI - 68	M	46	NC - for digital use	ready-made	-		N/A	ADC Card		46
J3	SCSI - 68	M	47	NC - for digital use	ready-made	-		N/A	ADC Card		47
J3	SCSI - 68	M	48	NC - for digital use	ready-made	-		N/A	ADC Card		48
J3	SCSI - 68	M	49	NC - for digital use	ready-made	-		N/A	ADC Card		49
J3	SCSI - 68	M	50	NC - for digital use	ready-made	-		N/A	ADC Card		50
J3	SCSI - 68	M	51	NC - for digital use	ready-made	-		N/A	ADC Card		51
J3	SCSI - 68	M	52	NC - for digital use	ready-made	-		N/A	ADC Card		52
J3	SCSI - 68	M	53	NC - for digital use	ready-made	-		N/A	ADC Card		53
J3	SCSI - 68	M	54	NC - for digital use	ready-made	-		N/A	ADC Card		54
J3	SCSI - 68	M	55	NC - for digital use	ready-made	-		N/A	ADC Card		55
J3	SCSI - 68	M	56	AI GND	ready-made	-		N/A	ADC Card		56
J3	SCSI - 68	M	57	AI 7	ready-made	-		N/A	ADC Card		57
J3	SCSI - 68	M	58	AI 14	ready-made	-		N/A	ADC Card		58
J3	SCSI - 68	M	59	AI GND	ready-made	-		N/A	ADC Card		59
J3	SCSI - 68	M	60	AI 5	ready-made	-		N/A	ADC Card		60
J3	SCSI - 68	M	61	AI 12	ready-made	-		N/A	ADC Card		61
J3	SCSI - 68	M	62	AI SENSE	ready-made	-		N/A	ADC Card		62
J3	SCSI - 68	M	63	AI 11	ready-made	-		N/A	ADC Card		63
J3	SCSI - 68	M	64	AI GND	ready-made	-		N/A	ADC Card		64
J3	SCSI - 68	M	65	AI 2	ready-made	-		N/A	ADC Card		65
J3	SCSI - 68	M	66	AI 9	ready-made	-		N/A	ADC Card		66

On-Board Connector				Cable					Off-Board Connector		
Designation	Connector Type	M/F	Pin #	Function	Wire Type	Pair Pin	Shield	Color	Connector Type	M/F	Pin #
J3	SCSI - 68	M	67	AI GND	ready-made	-		N/A	ADC Card		67
J3	SCSI - 68	M	68	AI 0	ready-made	-		N/A	ADC Card		68
J4	D-sub-9	F	1	Extra DIO - 0					NC		
J4	D-sub-9	F	2	Extra DIO - 1					NC		
J4	D-sub-9	F	3	Extra DIO - 2					NC		
J4	D-sub-9	F	4	Extra DIO - 3					NC		
J4	D-sub-9	F	5	Extra DIO - 4					NC		
J4	D-sub-9	F	6	Extra DIO - 5					NC		
J4	D-sub-9	F	7	Extra DIO - 6					NC		
J4	D-sub-9	F	8	Extra DIO - 7					NC		
J4	D-sub-9	F	9	Digital Ground					NC		
J5	D-sub-9	F	1	Extra ADC - A high					NC		
J5	D-sub-9	F	2	Extra ADC - A low					NC		
J5	D-sub-9	F	3	Extra ADC - B high					NC		
J5	D-sub-9	F	4	Extra ADC - B low					NC		
J5	D-sub-9	F	5	Analog Ground					NC		
J5	D-sub-9	F	6	Extra ADC - C high					NC		
J5	D-sub-9	F	7	Extra ADC - C low					NC		
J5	D-sub-9	F	8	Extra ADC - D high					NC		
J5	D-sub-9	F	9	Extra ADC - D low					NC		
J6	D-sub-9	F	1	Temperature Power 12	twisted pair	7	Y	red	Sensor 12	-	1
J6	D-sub-9	F	2	Temperature Power 13	twisted pair	8	Y	red	Sensor 13	-	1
J6	D-sub-9	F	3	Temperature Power 14	twisted pair	9	Y	red	Sensor 14	-	1
J6	D-sub-9	F	4	NC							
J6	D-sub-9	F	5	NC							
J6	D-sub-9	F	6	NC							
J6	D-sub-9	F	7	Temperature Signal 12	twisted pair	1	Y	black	Sensor 12	-	2
J6	D-sub-9	F	8	Temperature Signal 13	twisted pair	2	Y	black	Sensor 13	-	2
J6	D-sub-9	F	9	Temperature Signal 14	twisted pair	3	Y	black	Sensor 14	-	2
J7	D-sub-25	F	1	Temperature Power 0	twisted pair	14	Y	red	Sensor 0	-	1
J7	D-sub-25	F	2	Temperature Power 1	twisted pair	15	Y	red	Sensor 1	-	1
J7	D-sub-25	F	3	Temperature Power 2	twisted pair	16	Y	red	Sensor 2	-	1
J7	D-sub-25	F	4	Temperature Power 3	twisted pair	17	Y	red	Sensor 3	-	1
J7	D-sub-25	F	5	Temperature Power 4	twisted pair	18	Y	red	Sensor 4	-	1
J7	D-sub-25	F	6	Temperature Power 5	twisted pair	19	Y	red	Sensor 5	-	1
J7	D-sub-25	F	7	Temperature Power 6	twisted pair	20	Y	red	Sensor 6	-	1
J7	D-sub-25	F	8	Temperature Power 7	twisted pair	21	Y	red	Sensor 7	-	1
J7	D-sub-25	F	9	Temperature Power 8	twisted pair	22	Y	red	Sensor 8	-	1
J7	D-sub-25	F	10	Temperature Power 9	twisted pair	23	Y	red	Sensor 9	-	1
J7	D-sub-25	F	11	Temperature Power 10	twisted pair	24	Y	red	Sensor 10	-	1
J7	D-sub-25	F	12	Temperature Power 11	twisted pair	25	Y	red	Sensor 11	-	1
J7	D-sub-25	F	13	NC					NC		
J7	D-sub-25	F	14	Temperature Signal 0	twisted pair	1	Y	black	Sensor 0	-	2
J7	D-sub-25	F	15	Temperature Signal 1	twisted pair	2	Y	black	Sensor 1	-	2
J7	D-sub-25	F	16	Temperature Signal 2	twisted pair	3	Y	black	Sensor 2	-	2
J7	D-sub-25	F	17	Temperature Signal 3	twisted pair	4	Y	black	Sensor 3	-	2
J7	D-sub-25	F	18	Temperature Signal 4	twisted pair	5	Y	black	Sensor 4	-	2
J7	D-sub-25	F	19	Temperature Signal 5	twisted pair	6	Y	black	Sensor 5	-	2
J7	D-sub-25	F	20	Temperature Signal 6	twisted pair	7	Y	black	Sensor 6	-	2

On-Board Connector				Cable					Off-Board Connector		
Designation	Connector Type	M/F	Pin #	Function	Wire Type	Pair Pin	Shield	Color	Connector Type	M/F	Pin #
J7	D-sub-25	F	21	Temperature Signal 7	twisted pair	8	Y	black	Sensor 7	-	2
J7	D-sub-25	F	22	Temperature Signal 8	twisted pair	9	Y	black	Sensor 8	-	2
J7	D-sub-25	F	23	Temperature Signal 9	twisted pair	10	Y	black	Sensor 9	-	2
J7	D-sub-25	F	24	Temperature Signal 10	twisted pair	11	Y	black	Sensor 10	-	2
J7	D-sub-25	F	25	Temperature Signal 11	twisted pair	12	Y	black	Sensor 11	-	2
J8	D-sub-15	F	1	Relay Coil Power 0	twisted pair	9	N	red	Relay 0	-	1
J8	D-sub-15	F	2	Relay Coil Power 1	twisted pair	10	N	red	Relay 1	-	1
J8	D-sub-15	F	3	Relay Coil Power 2	twisted pair	11	N	red	Relay 2	-	1
J8	D-sub-15	F	4	Relay Coil Power 3	twisted pair	12	N	red	Relay 3	-	1
J8	D-sub-15	F	5	Relay Coil Power 4	twisted pair	13	N	red	Relay 4	-	1
J8	D-sub-15	F	6	Relay Coil Power 5	twisted pair	14	N	red	Relay 5	-	1
J8	D-sub-15	F	7	Relay Coil Power 6	twisted pair	15	N	red	Relay 6	-	1
J8	D-sub-15	F	8	NC					NC		
J8	D-sub-15	F	9	Relay Coil Ground 0	twisted pair	1	N	black	Relay 0	-	2
J8	D-sub-15	F	10	Relay Coil Ground 1	twisted pair	2	N	black	Relay 1	-	2
J8	D-sub-15	F	11	Relay Coil Ground 2	twisted pair	3	N	black	Relay 2	-	2
J8	D-sub-15	F	12	Relay Coil Ground 3	twisted pair	4	N	black	Relay 3	-	2
J8	D-sub-15	F	13	Relay Coil Ground 4	twisted pair	5	N	black	Relay 4	-	2
J8	D-sub-15	F	14	Relay Coil Ground 5	twisted pair	6	N	black	Relay 5	-	2
J8	D-sub-15	F	15	Relay Coil Ground 6	twisted pair	7	N	black	Relay 6	-	2
J9	D-sub-9	F	1	Signal A High	twisted pair	2	Y	red			
J9	D-sub-9	F	2	Signal A Low	twisted pair	1	Y	black			
J9	D-sub-9	F	3	Signal B High	twisted pair	4	Y	red			
J9	D-sub-9	F	4	Signal B Low	twisted pair	3	Y	black			
J9	D-sub-9	F	5	Signal C High	twisted pair	6	Y	red			
J9	D-sub-9	F	6	Signal C Low	twisted pair	5	Y	black			
J9	D-sub-9	F	7	Analog Ground	twisted 3	8,9	Y	black			
J9	D-sub-9	F	8	Analog -5V	twisted 3	7,9	Y	white			
J9	D-sub-9	F	9	Analog +5V	twisted 3	7,8	Y	red			
J10	D-sub-37	F	1	HVControl 0	twisted pair	2	Y	red	HV 0		7
J10	D-sub-37	F	2	HVRef 0	twisted pair	1	Y	black	HV 0		9
J10	D-sub-37	F	3	HVControl 1	twisted pair	4	Y	red	HV 1		7
J10	D-sub-37	F	4	HVRef 1	twisted pair	3	Y	black	HV 1		9
J10	D-sub-37	F	5	HVControl 2	twisted pair	6	Y	red	NC		
J10	D-sub-37	F	6	HVRef 2	twisted pair	5	Y	black	NC		
J10	D-sub-37	F	7	HVControl 3	twisted pair	8	Y	red	NC		
J10	D-sub-37	F	8	HVRef 3	twisted pair	7	Y	black	NC		
J10	D-sub-37	F	9	HVControl 4	twisted pair	10	Y	red	NC		
J10	D-sub-37	F	10	HVRef 4	twisted pair	9	Y	black	NC		
J10	D-sub-37	F	11	HVControl 5	twisted pair	12	Y	red	NC		
J10	D-sub-37	F	12	HVRef 5	twisted pair	11	Y	black	NC		
J10	D-sub-37	F	13	HVControl 6	twisted pair	14	Y	red	NC		
J10	D-sub-37	F	14	HVRef 6	twisted pair	13	Y	black	NC		
J10	D-sub-37	F	15	HVControl 7	twisted pair	16	Y	red	NC		
J10	D-sub-37	F	16	HVRef 7	twisted pair	15	Y	black	NC		
J10	D-sub-37	F	17	NC					NC		
J10	D-sub-37	F	18	NC					NC		
J10	D-sub-37	F	19	NC					NC		
J10	D-sub-37	F	20	HV voltage monitor 0	single	-	Y	blue	HV 0		3
J10	D-sub-37	F	21	HV current monitor 0	single	-	Y	yellow	HV 0		6
J10	D-sub-37	F	22	HV voltage monitor 1	single	-	Y	blue	HV 1		3

On-Board Connector				Cable					Off-Board Connector		
Desig nation	Connector Type	M/F	Pin #	Function	Wire Type	Pair Pin	Shield	Color	Connector Type	M/F	Pin #
J10	D-sub-37	F	23	HV current monitor 1	single	-	Y	yellow	HV 1		6
J10	D-sub-37	F	24	HV voltage monitor 2	single	-	Y		NC		
J10	D-sub-37	F	25	HV current monitor 2	single	-	Y		NC		
J10	D-sub-37	F	26	HV voltage monitor 3	single	-	Y		NC		
J10	D-sub-37	F	27	HV current monitor 3	single	-	Y		NC		
J10	D-sub-37	F	28	HV voltage monitor 4	single	-	Y		NC		
J10	D-sub-37	F	29	HV current monitor 4	single	-	Y		NC		
J10	D-sub-37	F	30	HV voltage monitor 5	single	-	Y		NC		
J10	D-sub-37	F	31	HV current monitor 5	single	-	Y		NC		
J10	D-sub-37	F	32	HV voltage monitor 6	single	-	Y		NC		
J10	D-sub-37	F	33	HV current monitor 6	single	-	Y		NC		
J10	D-sub-37	F	34	HV voltage monitor 7	single	-	Y		NC		
J10	D-sub-37	F	35	HV current monitor 7	single	-	Y		NC		
J10	D-sub-37	F	36	NC					NC		
J10	D-sub-37	F	37	NC					NC		
J11	D-sub-37	F	1	Analog Ground	coax shield	2-9	Y	-	BNC	F	GND
J11	D-sub-37	F	2	Timing Signals A 0	coax inner	1	Y	-	BNC	F	1
J11	D-sub-37	F	3	Timing Signals A 1	coax inner	1	Y	-	BNC	F	1
J11	D-sub-37	F	4	Timing Signals A 2	coax inner	1	Y	-	BNC	F	1
J11	D-sub-37	F	5	Timing Signals A 3	coax inner	1	Y	-	BNC	F	1
J11	D-sub-37	F	6	Timing Signals A 4	coax inner	1	Y	-	BNC	F	1
J11	D-sub-37	F	7	Timing Signals A 5	coax inner	1	Y	-	BNC	F	1
J11	D-sub-37	F	8	Timing Signals A 6	coax inner	1	Y	-	BNC	F	1
J11	D-sub-37	F	9	Timing Signals A 7	coax inner	1	Y	-	BNC	F	1
J11	D-sub-37	F	10	Analog Ground					NC		
J11	D-sub-37	F	11	Xtra FPGA A 0					NC		
J11	D-sub-37	F	12	Xtra FPGA A 1					NC		
J11	D-sub-37	F	13	Xtra FPGA A 2					NC		
J11	D-sub-37	F	14	Xtra FPGA A 3					NC		
J11	D-sub-37	F	15	Xtra FPGA A 4					NC		
J11	D-sub-37	F	16	Xtra FPGA A 5					NC		
J11	D-sub-37	F	17	Xtra FPGA A 6					NC		
J11	D-sub-37	F	18	Xtra FPGA A 7					NC		
J11	D-sub-37	F	19	Analog Ground					NC		
J11	D-sub-37	F	20	Analog Ground	coax shield	21-28	Y	-	NC	F	GND
J11	D-sub-37	F	21	Timing Signals B 0	coax inner	20	Y	-	BNC	F	1
J11	D-sub-37	F	22	Timing Signals B 1	coax inner	20	Y	-	BNC	F	1
J11	D-sub-37	F	23	Timing Signals B 2	coax inner	20	Y	-	BNC	F	1
J11	D-sub-37	F	24	Timing Signals B 3	coax inner	20	Y	-	BNC	F	1
J11	D-sub-37	F	25	Timing Signals B 4	coax inner	20	Y	-	BNC	F	1
J11	D-sub-37	F	26	Timing Signals B 5	coax inner	20	Y	-	BNC	F	1
J11	D-sub-37	F	27	Timing Signals B 6	coax inner	20	Y	-	BNC	F	1
J11	D-sub-37	F	28	Timing Signals B 7	coax inner	20	Y	-	BNC	F	1
J11	D-sub-37	F	29	Analog Ground					NC		
J11	D-sub-37	F	30	Xtra FPGA B 0					NC		
J11	D-sub-37	F	31	Xtra FPGA B 1					NC		
J11	D-sub-37	F	32	Xtra FPGA B 2					NC		
J11	D-sub-37	F	33	Xtra FPGA B 3					NC		
J11	D-sub-37	F	34	Xtra FPGA B 4					NC		
J11	D-sub-37	F	35	Xtra FPGA B 5					NC		
J11	D-sub-37	F	36	Xtra FPGA B 6					NC		
J11	D-sub-37	F	37	Xtra FPGA B 7					NC		
J12	D-sub-15	F	1	Power +15V	single	-	N	orange	terminals	-	

On-Board Connector				Cable					Off-Board Connector		
Designation	Connector Type	M/F	Pin #	Function	Wire Type	Pair Pin	Shield	Color	Connector Type	M/F	Pin #
J12	D-sub-15	F	2	Power +15V	single	-	N	orange	terminals	-	
J12	D-sub-15	F	3	Power -15V	single	-	N	blue	terminals	-	
J12	D-sub-15	F	4	Power -15V	single	-	N	blue	terminals	-	
J12	D-sub-15	F	5	Power +5V	single	-	N	red	terminals	-	
J12	D-sub-15	F	6	Power +5V	single	-	N	red	terminals	-	
J12	D-sub-15	F	7	Power +5V	single	-	N	red	terminals	-	
J12	D-sub-15	F	8	Power +24V	single	-	N	yellow	terminals	-	
J12	D-sub-15	F	9	Power AGND	single	-	N	brown	terminals	-	
J12	D-sub-15	F	10	Power AGND	single	-	N	brown	terminals	-	
J12	D-sub-15	F	11	Power AGND	single	-	N	brown	terminals	-	
J12	D-sub-15	F	12	Power DGND	single	-	N	black	terminals	-	
J12	D-sub-15	F	13	Power DGND	single	-	N	black	terminals	-	
J12	D-sub-15	F	14	Power DGND	single	-	N	black	terminals	-	
J12	D-sub-15	F	15	Power 24GND	single	-	N	gray	terminals	-	

APPENDIX E

ADC AND DIGITAL I/O CARD PORT ASSIGNMENTS

The ADC and Digital I/O PCI cards in the embedded computer both have a number of ports that correspond to their respective connector pin-outs. Since these are hardwired, the function of each port in this system is fixed. These port assignments, as they relate to the circuits on the custom card, are given in the following charts.

Digital I/O Card				
Port #	In/Out	Bits	Circuit	Function
0	NC	0-7	Extra D I/O	None
1	Out	0-7	Temperature Sensors	Multiplexer control
2	Out	0-7	Relay Controller	On/Off signal to individual relays
3	Out	0-7	HV Controller	Data bus bits 0-7
4	Out	0-3	HV Controller	Data bus bits 8-11
4	Out	4-7	HV Controller	Chip select control
5	Out	0-7	HV Controller	Multiplexer control
6	Out	0-7	Synchronizer	Command (high) bits 8-15
7	Out	0-7	Synchronizer	Command (low) bits 0-7
8	Out	0-7	Synchronizer	Data In (high) bits 8-15
9	Out	0-7	Synchronizer	Data In (low) bits 0-7
10	In	0-7	Synchronizer	Data Out (high) bits 8-15
11	In	0-7	Synchronizer	Data Out (low) bits 0-7

Analog-to-Digital (ADC) Card				
Port #	Single/Diff	Diff Pair	Circuit	Function
0	Single	-	Temperature	Temperature sensor signal
1	Diff	9	Laser Energy Sensors	Sensor A high
2	Diff	10	Laser Energy Sensors	Sensor B high
3	Diff	11	Laser Energy Sensors	Sensor C high
4	NC	-	Extra Analog In	None
5	NC	-	Extra Analog In	None
6	NC	-	Extra Analog In	None
7	NC	-	Extra Analog In	None
8	Single	-	HV Controller	HV monitor signal
9	Diff	1	Laser Energy Sensors	Sensor A low
10	Diff	2	Laser Energy Sensors	Sensor B low
11	Diff	3	Laser Energy Sensors	Sensor C low
12	NC	-	Extra Analog In	None
13	NC	-	Extra Analog In	None
14	NC	-	Extra Analog In	None
15	NC	-	Extra Analog In	None

APPENDIX F

DC POWER BUDGET

Description	Part Number	Qty.	+15 V		-15 V		+5 V (digital)		+3.3 V	
			Each	Total	Each	Total	Each	Total	Each	Total
Voltage regulator +5V	LM1086IS-5.0	1	0.02	0.02		0		0		0
Voltage regulator -5V	LM2990S-5.0	1		0	0.015	0.015		0		0
Voltage regulator +3.3V	LT1764AEQ-3.3	1		0		0	0.001	0.001		0
Voltage regulator +1.5V	LT1764AEQ-1.5	1		0		0	0.001	0.001		0
Temperature sensor	AD590	16	0.0003	0.0048		0		0		0
Analog mux	ADG526AKR	2		0		0		0		0
DAC	AD767JP	8	0.013	0.104	0.023	0.184		0		0
Op amp	AD824AR	2	0.1	0.2	0.1	0.2		0		0
Bus drivers	74ACT244	5		0		0	0.07	0.35		0
3 to 8 decoder	SN74HC138N	1		0		0	0.05	0.05		0
3.3V-5V tranceiver	SN74ALVC164245DL	5		0		0	0.2	1	0.2	1
FPGA	EP1C3T144C6	1		0		0		0	0.3	0.3
				0		0		0		0
Relays	LY1-SPDT-24VDC	7		0		0		0		0
HV power supplies	MP2.5N24	4		0		0		0		0
Discriminators	AD6	4		0		0	0.01	0.04		0
Laser energy sensors	PS19	3		0		0		0		0
				0		0		0		0
				0		0		0		0
				0		0		0		0
Total Current Per Load Voltage (Amps)				0.3288		0.399		1.442		1.3

Total +15 V Supply Current (Amps)	0.5538
Total -15 V Supply Current (Amps)	0.519
Total +5 V Supply Current (Amps)	3.042
Total +24 V Supply Current (Amps)	4.259

Description	Part Number	Qty.	+1.5 V		+24 V		+5 V (analog)		-5 V (analog)	
			Each	Total	Each	Total	Each	Total	Each	Total
Voltage regulator +5V	LM1086IS-5.0	1		0		0		0		0
Voltage regulator -5V	LM2990S-5.0	1		0		0		0		0
Voltage regulator +3.3V	LT1764AEQ-3.3	1		0		0		0		0
Voltage regulator +1.5V	LT1764AEQ-1.5	1		0		0		0		0
Temperature sensor	AD590	16		0		0		0		0
Analog mux	ADG526AKR	2		0		0		0		0
DAC	AD767JP	8		0		0		0		0
Op amp	AD824AR	2		0		0		0		0
Bus drivers	74ACT244	5		0		0		0		0
3 to 8 decoder	SN74HC138N	1		0		0		0		0
3.3V-5V tranceiver	SN74ALVC164245DL	5		0		0		0		0
FPGA	EP1C3T144C6	1	0.3	0.3		0		0		0
				0		0		0		0
Relays	LY1-SPDT-24VDC	7		0	0.037	0.259		0		0
HV power supplies	MP2.5N24	4		0	1	4		0		0
Discriminators	AD6	4		0		0		0		0
Laser energy sensors	PS19	3		0		0	0.075	0.225	0.04	0.12
				0		0		0		0
				0		0		0		0
				0		0		0		0
				0		0		0		0
Total Current Per Load Voltage (Amps)				0.3		4.259		0.225		0.12

Total +15 V Supply Current (Amps)	0.5538
Total -15 V Supply Current (Amps)	0.519
Total +5 V Supply Current (Amps)	3.042
Total +24 V Supply Current (Amps)	4.259