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Fabrication of Suspended Microbolometers on SOI Wafers

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Introduction

A bolometer is a device to measure radiation energy by converting photon energy into heat on an isolated absorber. We plan to use carbon-nanotube (CNT) based absorber to enhance the photon absorption. The absorber is a few microns in size and is suspended with micron-sized bridges which also support metal lines for electrical measurements.

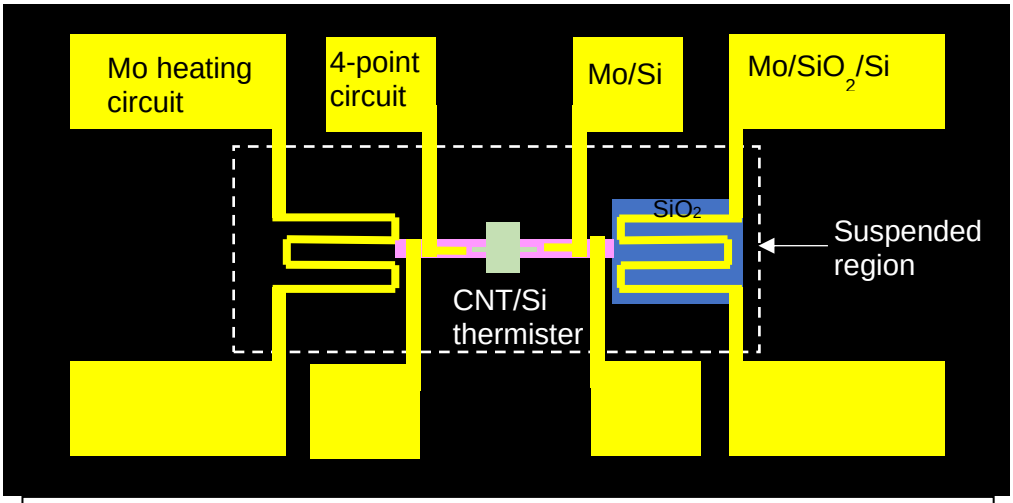

Fig.1 Schematic of the CNT-based microbolometer.

The heat leads to temperature and resistance change of the absorber. By measuring the resistance change and the known temperature coefficient of the Si resistance, we can deduce how much light energy has impinged on the absorber. We also want to know the dissipation of heat from the absorber through the bridge. Two serpentine circuits on each side of the absorber were designed to measure the thermal conductivity across the absorber. One circuit will pass a current to generate heat which will transfer across the two bridges to the sensing circuit. Measuring the resistance change of the sensing circuit, we can determine the temperature and heat input. From the dimensions of the bridges, we can thus calculate the thermal conductivity. The performance of a bolometer is characterized by the thermal conductivity and heat capacity of the absorber. For sensitive applications, we need a low thermal conductivity but for fast-change applications, we need high thermal conductivity. The masks contain 40 designs of different bridge and absorber geometries to test the performance of each design.

To reduce the heat loss to the substrate, the absorber and the heating/sensing area has to be suspended from the substrate and supported by 4 thin bridges. A common way to create a suspended structure is to use a SOI wafer which consists of a buried oxide (BOX) layer sandwiched between a Si device layer, typically a few microns thick, and the Si handle (typically 400 μm thick). Once the top Si layer is fabricated with windows to expose the BOX to buffered HF (BHF) solution, the oxide layer can be etched off to suspend the devices on the Si layer. In the previous attempt to fabricate suspended structures, we find that one of the photomasks, M4, was not designed correctly. As a result, the BHF etched off the metal structures and ruined the device. The goals of this project is to test (1) a newly designed M4 photomask and (2) a back alignment system in the mask aligner. The backside alignment kit allows an alternative approach to suspend the absorber. An existing M5 photomask will open up windows in the backside of the SOI wafer. An inverted-pyramid-shaped hole in the handle will be created by a

KOH etch through the window. Then, the BOX will be etched through this hole and the absorber will be suspended. Then the front-side device fabrication will begin.

We chose to use a double-sided Si wafer instead of a much more expensive SOI wafer to perform these tests. The final product, therefore, will not be a functional device but we will be able to test each process and find out problems.

Backside alignment

First, a new backside alignment system for photolithography was installed in the ABM mask aligner. (Fig 2) This new system uses infrared to penetrate a wafer from the backside to the microscope above the front side. This new upgrade allows users to align the front side features with those on the backside when double-side lithography is conducted. We first encountered a defected part that broke the chuck vacuum when the wafer was in contact with the mask. After receiving a replacement part from the manufacturer, the mask aligner worked properly. We can see the etched holes in the backside of the wafer from the front side. Unfortunately, M5 needs to be redesigned because the alignment marks are outside of the infrared windows of the new chuck.

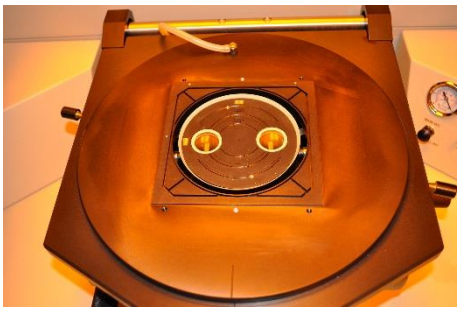

Fig.2 Chuck and mask holder for the backside alignment system

Device fabrication

1. Photolithgraphy-M5

To etch Si on the backside, we need to protect the front side. We use nLOF2035 to coat the front side followed by a blank UV exposure and double the post exposure bake (PEB) time to ensure the oxide layer on the front side will be protected against KOH. Then we used AZ1512 resist and mask M5 to conduct photolithography to define the windows to be opened in the backside oxide layer.

2. Oxide window etch

After photolithography, we put the wafer in RIE-1C to conduct reactive ion etching (RIE). The gases were CHF_3:O_2 =10:1 Pa and the plasma power was 50 W at 15 ^oC. We used Nanoscope 3000 to check if the oxide in the window was completely removed.

3. Anisotropic Si etch

We dip the wafer into a 25 wt % KOH solution at 52 ^oC for 12.5 h to etch the backside Si through the SiO_2 window. (Fig.3) The rest of the Si area on both sides should be protected by the remaining oxide. The etch depth was 7.5 μm. It is not clear why the etch rate was 20 times lower than before. However, we find that the wafer cannot be etched longer because the oxide on both sides has been significantly etched as well. More work needs to be done to study the KOH etch rate on both Si(100) and SiO_2.

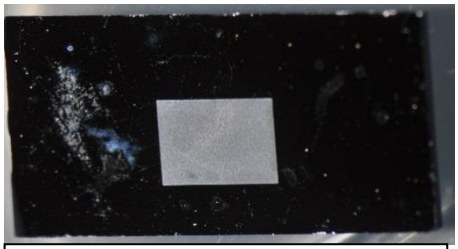

Fig.3 An etched hole on the backside of the Si wafer.

4. Photolithography-M1

After cleaning the wafer by Piranha solution after the backside etch, we used photomask M1 to conduct a photolithography to define a pattern of oxide supporting the Mo contact pads and the heating/sensing circuitry on the front side. In this step we first spin coated a layer of nLOF 2020 resist, followed by softbake, UV exposure, PEB and development.

5. Descum and oxide RIE

After photolithography, we use O_2-RIE to clean up the residue photoresist followed by a check by Nanoscpec 3000 to ensure a complete removal of the photoresist in the patterned area. Then the wafer was put in RIE-1C to conduct the CHF_3/O_2 RIE to remove the oxide in the patterned area (the yellow region in Fig. 4). Note that the oxide is not always green. In fact SiO_2 thin film is transparent, so different thickness expresses different color due to optical interference.

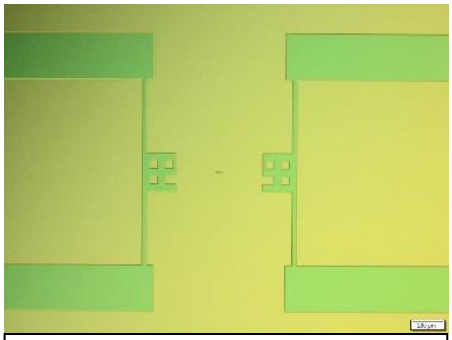

Fig.4 Optical image of oxide (green) and Si (yellow) region.

6. Photolithography-M2

After stripping off photoresist from step-5, we proceed to use photolithography and mask M2 to define the absorber and prepare to coat this area with Al_2O_3 and Fe for CNT growth. It is important to align M2 with features in M1 so the absorber will be positioned precisely as designed. After development, the whole wafer was covered with a layer of nLOF2020 except the absorber region.

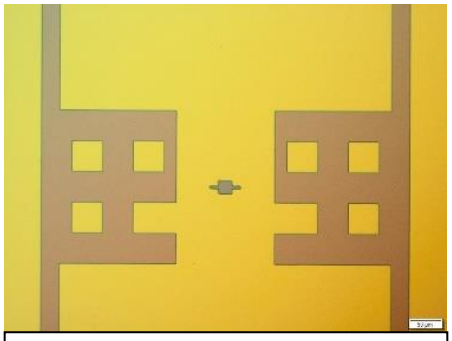

Fig.5 The absorber (center) was coated with Al_2O_3 and Fe.

7. Coating Al_2O_3 and Fe

We sputtered a layer of 40 nm Al_2O_3 on the wafer first followed by a layer of 2-nm Fe. Then we conducted the liftoff process to remove all metal layers except in the absorber region. Note that the oxide region is brown in Fig.5 because of a different thickness compared to the location in Fig.4. One can notice a slight color change of the absorber due to the 40 nm of Al_2O_3.

8. Photolithography-M3

After stripping off the photoresist of step-6, the next photolithography is to use mask M3 to define the heating and sensing circuitry on the oxide pattern. We used the same photoresist and process as in step-6.

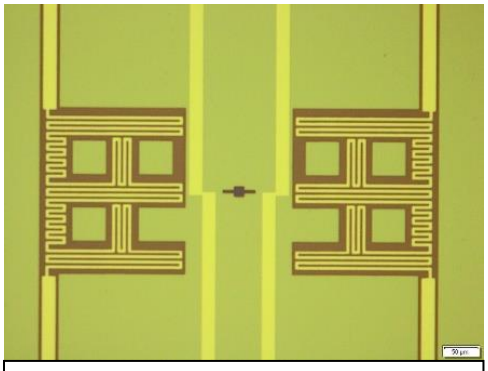

Fig.6 The serpentine Mo heating and sensing circuitry (yellow).

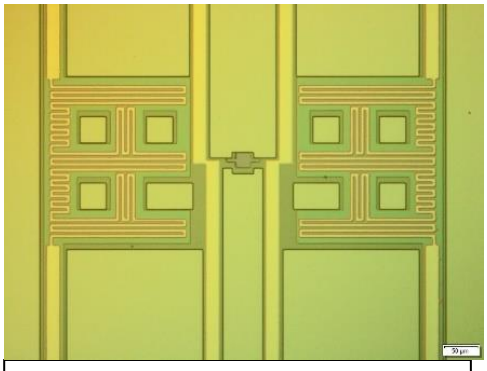

Fig.7 Patterns defined by photolithography in step-10.

9. Coating Mo

After development, we sputtered 100-nm thick Mo layer followed by the liftoff process. Figure 6 shows that M3 and M2 are aligned quite well. The Mo lines are reflective so the color

is yellow. The serpentine form of the Mo line is to increase resistance so the electrical heating can be efficient and the resistance change can be maximal for sensing. Mo has a high melting point so the film will not dewet during CNT growth.

10. Photolithography-M4

After stripping off the photoresist of step-8, the next photolithography is to use mask M3 to define the Si area to be etched to expose the BOX for the suspension etch. We use the same resist and process as in step-8. The y-alignment was off by 4 μm as shown in Fig. 7. Unfortunately, we cannot redo the process because the Mo coating cracked on the alignment mark of M3. Another round of resist stripping could remove the marks completely and we cannot align M4 with M3 patterns. This is an important lesson for future work.

11. Dicing

With the photoresist still intact, we proceed to dice the wafer into individual die of 5mmx10mm so that we can fine tune the conditions for Si and BHF etch for a few pieces instead of the whole wafer.

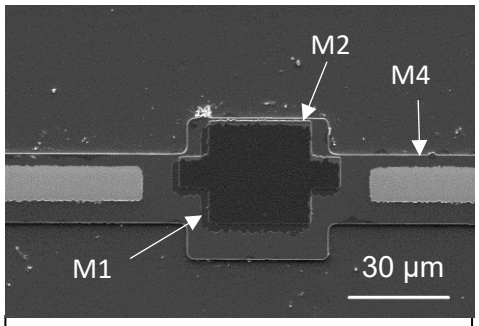

Fig.8 Misalignments of M4 with M1/M2 at the absorber island.

12. Si RIE

We put a few pieces patterned in step-10 in RIE-1C to etch Si. The gases used were SF_6:O_2=18:9 Pa with a power of 30 W at 15 °C. The etch follows the photoresist pattern quite well but one can see clearly the misalignment between M1/M2 and M4 in Fig. 8.

13. BHF etch

Because of the misalignment of M4 with M1, the BHF etched off the SiO_2 underneath the Mo and Fe/Al_2O_3 pattern after 2.5h. (as marked in Fig. 9) The Mo lines were not damaged in this test. However, they will be lifted off after a 25 h BHF etch if we want to suspend the entire heating and sensing islands.

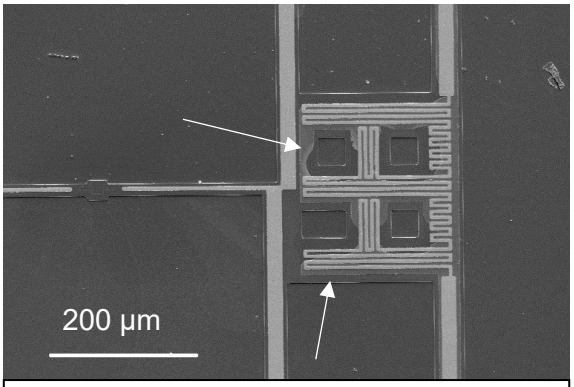

Fig.9 After 2.5h BHF etch, part of the oxide underneath the Mo lines was etched off.

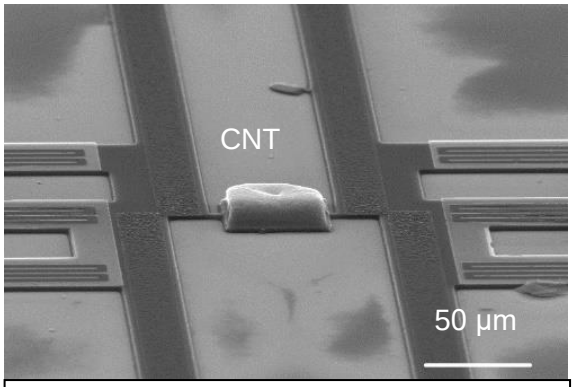

Fig.10 A 9-μm CNT forest was grown on the absorber.

14. CNT growth

We stripped resist from a piece of the un-etched device and put in CVD reactor. The gas mixture was C_2H_4:H_2:Ar=75:250:175 sccm at 750 °C for 20 min. A CNT forest of 9 μm tall was generated. (Fig. 10) This test demonstrates that after many rounds of photoresist coating and stripping the Fe/Al_2O_3 coating in step-7 remains intact. However, the height was only 9 μm

which is much less than a few hundreds of microns that have been experienced regularly from less complicated fabrication process. More work is needed to investigate why the growth rate was so low.

Conclusion

Our main goals were to test the new back-alignment system and the new photomask M4. The installation of the new backside alignment system took some work, but it did make the backside patterns observable from the front side. Photomask M4 did cover more of the bolometer circuitry than the old mask and the etching damage was reduced. We expect a much better result if the alignment can be made better in the future.