Radiation Hardened by Design 8 bit RISC with Dual I2C Bus Support and SPI for External NVM Support

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Outline

• Structured ASIC 90nm IBM 9LP Process Overview
• Radiation Hardened by Design
• Mini-PnP SASIC Block Diagram and Toplevel
• Mini-PnP SASIC 3x3 mm Die Bonded Out to 172 pin CQFP for Evaluation
• Evaluation Board with 172 pin CQFP Socket
• Mini-PnP Power Consumption Measurements
• Post Silicon Verification Tests
  – Functional Tests
  – Wishbone Cores
  – Complex Flows
• Structured ASIC Verification
• Conclusions
• Questions
Funding Support

- The development of the Mini-PnP Structured ASIC has been funded by the Air Force Research Laboratory (AFRL).

- The Post Silicon Verification effort has been funded through an AF SBIR Enhancement by AFRL to functionally test the ASIM chips and develop evaluation and radiation test boards and investigate a packaging road map.
Structured ASIC 90nm CMOS IBM 9LP
Hardness Estimate:

- TID > 1Mrad(Si)
- SEU > 1e-5 Errors/day
- SEL > 100 MeV-cm²/mg (LET)
RHBD Circuit Approach (SEU and SET)

- Data latch SEU/SET mitigation
  - Temporal sampling to achieve both spatial and time redundancy
  - Variable sampling delay for hardness / performance tradeoff
  - Immune to multiple node strikes and transients on any node
  - Self scrubbing, does not integrate errors as normal TMR

- SRAM SEU/MBU/SET mitigation
  - Conventional 4T data storage with PMOS access (single and dual port)
  - EDAC for single bit errors
  - Scrubbing to reduce multiple bit error accumulation over time
  - Architectural solution to SETs and MBUs

Ref: Mavis, Eaton 2002
Ref: Mavis, MRQW 2007
Mini-PnP SASIC High Level Block Diagram

- Micro-RDC Microsystems Research Development Corporation

- 25th Annual AIAA/USU Conference on Small Satellites
Mini-PnP SASIC Features

Enhanced Open Cores PIC 8 bit RISC CPU
• 50 MHz Clock
• Watch Dog Timer
• External Interrupts
• Wishbone Cross Bar Switch Support

Memory Sub Systems
• On Chip 2x96x8 Register Files
  Temporal Latch based Flip Flops
• On Chip 4Kx14 Program RAM
  Bootup from External SPI EEPROM
  Design Hardened 4Kx14 Program SRAM w/EDAC
• On Chip ROM for Testing and Bootup
• SPI Slave for Firmware Download and Upload to Silicon
• Support for 128 KBytes External SPI Non Volatile Memory

Peripherals
• I2C Primary Master/Slave
• I2C Secondary Master
• SPI Master with 5 Slave Selects

Power Supply
Dual Voltage Supply 1.2 V Core and 1.2V to 3..3V I/O
Software Development Support

- Full Support for C and Assembly Firmware Development
- C API for SPI Master, I2C, Serial Interface
- Firmware Download to Silicon via USB/SPI Interface
- Tool for EEPROM Programming from Intel Hex Checksum File
- Tool to Write XTEDS to EEPROM and Other Data
Mini-PnP SASIC Memory Subsystem, Bootup and XTEDS Support

SPI Serial NVM
1 Mbit (128K x 8)
e.g. ATML AT25128A
Firmware/XTEDS

SPI Bootup Master/
RISC SPI Master Select

MOSI CLK Sel MISO

Load (Bootup)

SPI Slave Download

R/W ADDR DODI

InstrMemorySelect

14-bit Memory Code
13-bit Memory Address

Instruction Memory ROM

RISC

Wishbone Bus

SPI Master OpenCores

clk rst_n
MINI-PNP SASIC DIE

Specifications of the Mini-PnP SASIC Die.

**Die Size**
- 3.156mm X 3.543mm
- 64 micron pad pitch
- 50 micron x 50 micron pad size
- .7 mil Al bond wire recommended

**Die thickness**
- 470μm
Mini-PnP SASIC Pins

Mini-PnP SASIC uses 172 pins which are comprised of:

- 96 CMOS General Purpose I/O
- 17 VSS0
- 18 VSS1
- 17 3.3V Vdd IO
- 18 1.2V Vdd Core
- 6 Grounded Signals
172 Pin Ceramic Quad Flat Pack Package for Post Silicon Verification
172 Pin Ceramic Quad Flat Pack Package for Post Silicon Verification
Mini-PnP SASIC Evaluation Board

- 172 pin CQFP Socket
- Separate supplies for Core (1.2V), Chip IO (3.3v) and Peripherals (3.3V).
- Current monitoring of all supplies.
- Single 5V supply support.
- Support for 8 GPIO signals.
- Debounced switches for reset, SPI Download, manual Bootup, automatic Bootup, interrupts.
- Program Counter for logic analyzer monitoring and debug.
- RS-232 DTE and DCE.
- SMA CPU Clock input.
- Dual I2C Buss interface.
- On Board ATMEL Flash (128Kx8) for Bootup and XTEDS.
- Connectors for SPI Firmware download/upload via USB/SPI interface to PC.
- 4 digit Seven Segment display for debug and software development.
- Support for SPI Master and Slave using PMODs (12 pin).
Assembled SASIC Mini-PnP Evaluation Board
Measured Power Consumption Taped Out Silicon Mini-PnP SASIC ASIM

Mini-PnP SASIC Power versus Clock Frequency

- Core Vdd=1.2V
- IO Vdd=3.3V

Power (mW)

- Core
- IO
- Total Power

Clock Frequency

- 75.00MHz
- 50.00MHz
- 25.00MHz
- 12.50MHz
- 6.25MHz
- 3.12MHz
- 1.56MHz
- 390.62KHz
- 0
## Mini-PnP SASIC Silicon Current Measurements

**Core and IO**

<table>
<thead>
<tr>
<th>Frequency</th>
<th>Power (mW)</th>
<th>Current (mA)</th>
<th>Power (mW)</th>
<th>Current (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>75.00MHz</td>
<td>44.04</td>
<td>36.7</td>
<td>7.11</td>
<td>2.844</td>
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<tr>
<td>50.00MHz</td>
<td>27.36</td>
<td>22.8</td>
<td>4.44</td>
<td>1.774</td>
</tr>
<tr>
<td>25.00MHz</td>
<td>14.52</td>
<td>12.1</td>
<td>2.50</td>
<td>1.000</td>
</tr>
<tr>
<td>12.50MHz</td>
<td>7.32</td>
<td>6.1</td>
<td>1.55</td>
<td>0.618</td>
</tr>
<tr>
<td>6.25MHz</td>
<td>3.72</td>
<td>3.1</td>
<td>0.98</td>
<td>0.392</td>
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<tr>
<td>3.12MHz</td>
<td>2.016</td>
<td>1.68</td>
<td>0.70</td>
<td>0.280</td>
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<tr>
<td>1.56MHz</td>
<td>1.104</td>
<td>0.92</td>
<td>0.57</td>
<td>0.226</td>
</tr>
<tr>
<td>390.62KHz</td>
<td>1.104</td>
<td>0.92</td>
<td>0.57</td>
<td>0.226</td>
</tr>
<tr>
<td>143.229KHZ</td>
<td>0.276</td>
<td>0.23</td>
<td>0.48</td>
<td>0.197</td>
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<tr>
<td>0</td>
<td>0.1956</td>
<td>0.163</td>
<td>0.27</td>
<td>0.108</td>
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</tbody>
</table>
Mini-PnP SASIC Post Silicon Functional Verification Tests

- Functional Unit Tests
- Wishbone Cross Bar Switch Cores
- Complex Flows Tests
## Functional Unit Tests

<table>
<thead>
<tr>
<th>No.</th>
<th>Test Name</th>
<th>Block Tested</th>
<th>Function</th>
<th>Pass</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>uart</td>
<td>Built in UART</td>
<td>Output characters at 38400 bps</td>
<td>Yes</td>
</tr>
<tr>
<td>2</td>
<td>i2c_0_master</td>
<td>I2C Core 0 on Wishbone Bus Master</td>
<td>Read I2C ADC (Proximity Detector) Write DAC</td>
<td>Yes</td>
</tr>
<tr>
<td>3</td>
<td>i2c_0_slave</td>
<td>I2C Core 0 on Wishbone Bus Slave</td>
<td>Program I2C Address, Scan for Address, Verify Slave Address, Write</td>
<td>Yes</td>
</tr>
<tr>
<td>4</td>
<td>i2c_1</td>
<td>I2C Core1 on Wishbone Bus Master</td>
<td>Read I2C ADC (Proximity Detector) Write DAC</td>
<td>Yes</td>
</tr>
<tr>
<td>5</td>
<td>spi_core</td>
<td>SPI Core/Wishbone Bus</td>
<td>Read SPI EEPROM Manufacture ID/XTEDS</td>
<td>Yes</td>
</tr>
<tr>
<td>6</td>
<td>wdt_cop</td>
<td>Watchdog Timer Core/Wishbone Bus</td>
<td>Setup WDT and generate reset on mcu_rst_rld_n</td>
<td>Yes</td>
</tr>
<tr>
<td>7</td>
<td>on_chip_reg_banks</td>
<td>On chip register banks 96 bytes each</td>
<td>Write sequence and read back and check both bank0 and bank1</td>
<td>Yes</td>
</tr>
<tr>
<td>8</td>
<td>interrupt_i2c_0</td>
<td>interrupt flow, mask, status reg, i2c 0 core</td>
<td>Generate interrupt on Rx and Tx in I2C Core 0. Verify ISR for Ext. Interrupt</td>
<td>Yes</td>
</tr>
<tr>
<td>9</td>
<td>interrupt_i2c_1</td>
<td>interrupt flow, mask, status reg, i2c 1 core</td>
<td>Generate interrupt on Rx and Tx in I2C Core 1. Verify ISR for Ext. Interrupt</td>
<td>Yes</td>
</tr>
<tr>
<td>10</td>
<td>interrupt_wdt_cop</td>
<td>interrupt flow, wdt mask, status, WDT COP Core</td>
<td>Generate interrupt on WDT count down to zero. Verify ISR invoked and status showing interrupt</td>
<td>Yes</td>
</tr>
</tbody>
</table>
# Complex Flows Tests

<table>
<thead>
<tr>
<th>No.</th>
<th>Flow Name</th>
<th>Blocks Tested</th>
<th>Function</th>
<th>Pass</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>SPI_DOWNLOAD_PROGRAM_RAM_EXECUTION_WRITE</td>
<td>SPI Slave 4Kx14 EDAC Distributed RAM</td>
<td>Download code through SPI Slave, Execute from Distributed RAM, Upload via SPI Slave and Verify RAM</td>
<td>Yes</td>
</tr>
<tr>
<td>2</td>
<td>EEPROM_Bootup</td>
<td>SPI EEPROM Master, Muxes to Distributed RAM, Bypass Mode, Manual</td>
<td>Copy code from EEPROM into Distributed RAM with SPI Master, Execute and Test Distributed</td>
<td>Yes</td>
</tr>
<tr>
<td>3</td>
<td>Automatic_Reload_EPSROM</td>
<td>SPI EEPROM Master, Muxes to Distributed RAM, Bypass Mode, Reload and Automatic Reset RAM Select, Soft Reset RISC</td>
<td>Copy code from EEPROM into Distributed RAM with SPI Master, Execute and Test Distributed RAM Program Memory Instruction Execution. Automatic Mode.</td>
<td>Yes</td>
</tr>
</tbody>
</table>
Mini-PnP SASIC Multi-Chip Module

Power
Core 1.2V
IO 3.3V

Test UART
CMOS
Rx Tx

SPI_NVM_CONTROL

SCL_0
SDA_0

SCL_1
SDA_1

12C Slave/Master BUS

scli_0
sda0_0
scl0_0

12C Master BUS

scli_1
sda1_0
scl1_0

Mini_PnP SASIC
3x3 mm

SPI_NVM Die
2x2 mm

2x2 mm NVM Die

8

CLK
GPIO

RST_n
RELOAD

RST_RLD_n

NVM_MOSI
NVM_SCLK
NVM_SSEL
NVM_MISO

28 Pin MCM
Mini-PnP SASIC Die Chip on Board (COB)

Mini-PnP COB: Illustration Only (Subject to Design Rules of Manufacturer)
Note Power and Ground Rings
Structured ASIC Verification

- Verification of SASIC Logic Fabric running at 75 MHz Clock with 50% utilization on 3x3 Chip

- Verification of Dual Port Distributed RAM at 75 MHz Clock
  - Configured as 4Kx14 RAM with EDAC
Conclusions

- Mini-PnP SASIC 3x3 Die Taped Out on IBM 90nm 9LP CMOS Process.
- Mini-PnP SASIC Chip uses RHBD Techniques Including Temporal Latches for SEU Immunity.
- Up to 75 MHz Clock
- Mini-PnP SASIC Chip Achieves Very Low Power Consumption.
- Power Reduction Through Clock Scaling.
- Evaluation Board Fabricated and Built for Post Silicon Verification Tests of all Functional Units, Complex Flows and all Interfaces.
- All Functional Tests Pass in Post Silicon Verification.
- All Cores Interfaced to Open Cores PIC Based RISC CPU using Wishbone Crossbar Switch Pass Post Silicon Verification tests.
- Built in ROM and SPI Firmware Download Capability Allow all Functional Units and Complex Flows to be Tested in Silicon.
- 172 pin CQFP Package and Evaluation Board with Socket Allow for Full Hardware Integration Evaluation in Spaceborne Systems with Complete Software/Hardware Development Support.
- Support for SPA-1 Space Avionics Plug and Play Systems.
References

Lyke, James, *Bringing the Vision of Plug-and-play to High-Performance Computing on Orbit*, HPEC 2009


