FPGA-based Coherent MSK Spread Spectrum Modem for Small Satellites TT&C Transponders

Prepared by
Ahmed Maghawry
Research Assistant
NARSS/Egypt
Overview

- Type II MSK DS-SS Modulator
- Type II MSK DS-SS Demodulator/Synchronizer
- Demodulator Front-end (HPF and AGC)
- Signal Suppression Factor
- Frequency Detector
- Carrier and Clock Recovery
- Phase Ambiguities Solver and PRS Code Acquisition
- Modem performance
Coherent Digital Modems

- 3dB BER improved performance
- Coherent carrier and clock
- Tracking using DS-SS
- Suitable for low SNR links
Type II MSK DS-SS Modulator

- The sinusoidal weighting functions do not alter the polarities of modulating data in I or Q channels.

\[
\begin{array}{c|c|c}
\text{type I} & \text{type II} \\
K = 1 & \text{clk of } 4T_s \\
K_{Ts} = T_s & \text{clk of } 4T_s \\
\end{array}
\]

- Control signal for addition or subtraction of phase

- WPI weighting function

- CPI carrier phase increment

- LUT modulated signal
Type II MSK DS-SS Modulation

- Spectrum for random data
- $f_o = 5.7 \text{ MHz}$
- Symbol rate 1 MHz
- $f_1 = 5.5 \text{ MHz}$
- $f_2 = 6 \text{ MHz}$
Type II MSK DS-SS Cont’

- Spectrum for I & Q channels modulated by PRSs
- $f_o = 5.8$ MHz
- Symbol rate 1 MHz
- $f_1 = 5.55$ MHz
- $f_2 = 6.05$ MHz
Subsampled Type II MSK Signal

- Subsampling frequency = 5 MHz
- Aliases arise due to frequency beating
MSK Demodulator/ Synchronizer

- Demodulator front end
- Squarer
- Frequency Detector
- Carrier and clock recovery
- Phase ambiguities solver and PRS code acquisition.
- Demodulator

Subsampled MSK modulated signal plus Gaussian noise

Demodulator front-end (HPF & AGC)

Squarer

Frequency detector

Carrier and clock recovery

Phase ambiguities solver and PRS code acquisition

Demodulator

Detected I channel PRS
Detected Q channel PRS
MSK synchronizer acquisition/tracking state diagram

- Start
- High pass filtering
- Automatic gain control
  - Spectrum levels below threshold
  - Frequency levels below threshold
  - LPLLs' lock detectors levels below threshold
  - Frequency acquisition
  - Phase and clock tracking
  - Code acquisition counter time out
  - Code correlator output below threshold
  - LPLLs lock
  - Phase ambiguities solving and PRS code acquisition
- Data extraction
Digital Demodulator Front-End

HPF

ADC output \( N_{ADC} = 14 \)

Overrange bit of ADC

\( N_{ADC} + 1 = 15 \)

High pass filter

HPF output

DC component

HPF input

HPF output
Digital Demodulator Front-End

AGC

\[ G(V_c(t)) = G_0 V_c(t) \]

\[ A_{\text{out}}(t \to \infty) = A_{SS} \]

LAGC

\[ G(V_c(t)) = G_0 \exp(G_1 V_c(t)) \]

EAGC

\[ A_{\text{out}}(t \to \infty) = A_{SS} \]
LAGC and EAGC Early Time Response
LAGC and EAGC Late Time Response
Signal Suppression Factor
MSK Frequency Detector

Squared subsampled MSK modulated signal plus Gaussian noise

- BPF at 2f_1s
- LAGC_1
- Baseband quadrature downconverter at 2f_1s
- IDF (dump rate = f_s/12)
- IDF (dump rate = f_s/12)
- CFFT
- Power calculation and peak search
- Actual frequency to phase increment calculator

- Constant phase increment equivalent to Doppler frequency shift (PDFS)
Digitally Implemented LPLL

$R = \text{rate reduction}$

$\text{Shift} = n$

$\text{Shift} = m$

$\text{Register}$

$R = \text{rate reduction}$

$8+\text{ceil}(\ln(R)/\ln2)$

$\text{FSA}$

$\text{FSA}/R$

$\text{Register}$

$\text{LUT}$

$\text{PD}$

$\text{MDDS}$

$\text{Increment}$

$\text{DDS}$

$\text{IDF}$

$\text{PIF}$
LPLL Pull-In Process
Carrier and Clock Recovery

Subsampled MSK modulated signal plus Gaussian noise

Carrier and clock recovery

Phase increment equivalent to Doppler frequency shift (PDFS), from frequency detector

180° out phase chip clocks

180° phase manipulation block

Quadrupled carrier phase

Doubled chip clock phase

Chip clock generator

Quadrature carriers generator

Phase increment equivalent to 2f1s = 1MHz

Phase increment equivalent to 2f2s = 2MHz

Carrier lock detector

Carrier lock detector

Carrier lock indicators

Carrier lock indicators

PDFS

PDFS

IDF

IDF

PIF

PIF

LPLL for 2f2s sinusoidal signal

LPLL for 2f1s sinusoidal signal

R

R

32

32

R

R

33

33

LUT

LUT

LUT

LUT

90°

90°

90°

90°

Increment equivalent to 2f1s = 1MHz

Increment equivalent to 2f2s = 2MHz

Phase manipulation block

R

R

34

34

10 MSB

10 MSB

1 MSB

1 MSB

180° out phase

Delay by ½ chip

118 MS

118 MS

Quadrature carriers

Delay by ½ chip

Chip clock generator

Quadrature carrier generator

90°

90°

Center 799.99 kHz

Span 10 kHz

RFW: 200 Hz M1 799.99 kHz 9.8 dBm

VBW: 10 Hz M2 -1 MHz -3 dBm

SW 49.01's Ref: 15.0 dBm Att: 30

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Maghawry
Phase Ambiguities Solver and PRS Code Acquisition

Phase ambiguities solver and PRS code acquisition

Start

Control signals assuming no PhAs in either the carrier or the phase

Correlation over ten PRS patterns

Is the peaks found?

Yes

End

Correct the signs of the extracted data

No

Is PhAs control signals combinations scanned

Yes

Change the PhAs control signals combination

No

Shift the local PRS by one chip

Begin with PRS lock indicator

Is the correlation repeated \( N_{\text{PRS}} \) times

Yes

In-phase and quadrature chip clocks router

180° out phase clock

Control signals for data sign correction

In-phase clock

180° out phase clock

IDF \( (10N_{\text{PRS}} \) periods)

BS, I channel baseband data

BSQ, Q channel baseband data

In-phase carrier

Quadrature carriers router

Carrier lock indicators

Quadrature carriers

Phase ambiguities solver algorithm and PRS code acquisition

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Correlation Spectrum of PRS Code Acquisition

- Three valued for one chip shifts
- Five valued for half chip shifts
MSK Demodulator

Subsampled MSK modulated signal plus Gaussian noise

In-phase channel baseband data

BS_i

In-phase carrier

Quadrature carrier

Baseband downconverter

In-phase clock (chip rate)

Threshold and sign correction

Control signals for data sign correction

Threshold and sign correction

In-phase clock (chip rate)

Quadrature clock (chip rate)

Spreading code I generator (half sines)

Spreading code Q generator (half sines)

BS_i

BS_o

BS_i

BS_o

Start of data extraction

Demodulator

PRS lock indicator

PRS_i

PRS_o
BER and Carrier and Clock Phase Variances

Theoretical vs implemented SEP curves for coherent MSK signal
# FPGA Utilization Summary

<table>
<thead>
<tr>
<th>Resources</th>
<th>Utilization</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of slices</td>
<td>2923 out of 13696</td>
<td>21%</td>
</tr>
<tr>
<td>Number of RAMB16s</td>
<td>11 out of 136</td>
<td>8%</td>
</tr>
<tr>
<td>Number of MULT18X18s</td>
<td>44 out of 136</td>
<td>32%</td>
</tr>
<tr>
<td>Number of BUFGMUXs</td>
<td>7 out of 16</td>
<td>43%</td>
</tr>
<tr>
<td>Number of external IOBs</td>
<td>86 out of 644</td>
<td>13%</td>
</tr>
<tr>
<td>Number of DCMs</td>
<td>1 out of 8</td>
<td>12%</td>
</tr>
</tbody>
</table>
Conclusions

- Implementation using minimum resource (i.e. ≈ 21%)
- Low power Consumption due to employing subsampling
- Tested with simulated real environment (i.e. Doppler shift & low SNR)
- A library of standard blocks can be used in new designs (e.g. AGC &LPLL)
- Suggestion of including in-flight BER and SNR measurements in CCSDS TM/TC recommendation and/or reports
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Thanks