5-2024

Design and Implementation of an Accelerated Lifetime Testing Platform for Silicon Carbide MOSFETs

Conner Deppe
Utah State University, a02270072@usu.edu

DESIGN AND IMPLEMENTATION OF AN ACCELERATED LIFETIME TESTING PLATFORM FOR SILICON CARBIDE MOSFETS

by

Conner Deppe

A thesis submitted in partial fulfillment
of the requirements for the degree

of

MASTER OF SCIENCE

in

Electrical Engineering

Approved:

Hongjie Wang, Ph.D. Major Professor	Regan Zane, Ph.D. Committee Member
Nick Roberts, Ph.D. Committee Member	D. Richard Cutler, Ph.D. Vice Provost of Graduate Studies

UTAH STATE UNIVERSITY
Logan, Utah

2024

ABSTRACT

Design and Implementation of an Accelerated Lifetime Testing Platform for Silicon Carbide MOSFETs

by

Conner Deppe, Master of Science

Utah State University, 2024

Major Professor: Hongjie Wang, Ph.D.
Department: Electrical and Computer Engineering

Electric vehicle charging reliability is crucial to aid the widespread adoption of electric vehicles. Wide-band-gap devices known as Silicon Carbide MOSFETs are being increasingly deployed in state-of-the-art charging technology. Though there are many benefits of this device chemistry, the reliability of the device is not as well understood as the previously used technology. To help understand semiconductor reliability, remaining useful lifetime modelling is typically used along with online health monitoring in the attempt to prevent the need for corrective maintenance caused by catastrophic failure. This research investigates how accelerated lifetime testing can be used to collect data for modeling the remaining useful lifetime of Silicon Carbide MOSFETs. Power cycling using dc current is used to accelerate the aging while monitoring the variation in on-resistance. The resulting use of this data will be a new understanding of Silicon Carbide MOSFETs aging, while providing insights into online health monitoring of electric vehicle chargers.

(80 pages)

PUBLIC ABSTRACT

Design and Implementation of an Accelerated Lifetime Testing Platform for Silicon Carbide MOSFETs

Conner Deppe

In the last several years, the United States has seen a significant increase in sales of electric vehicles. The increase of electric vehicles brings the need for increased availability of public charging stations. In the last two years, satisfaction levels for public chargers have fallen significantly due to unreliability, which is raising concerns for new potential electric vehicle owners. To mitigate the reliability concerns, chargers must be physically understood so they can be consistently monitored to assess their health status. To understand the electric vehicle charging reliability, electrical components must first be understood. In the cutting-edge charging technology, the relatively new wide-band-gap semiconductor devices known as Silicon Carbide MOSFETs have been widely deployed. Given the relative novelty of these devices, their reliability remains unexplored. This thesis presents the use of accelerated lifetime testing, used on previous semiconductor devices, to collect data which may be used in the future to develop models for remaining useful lifetime detection. The chosen method of accelerated lifetime testing is dc power cycling, which causes degradation to the device similar to what is seen after extended use in real systems.

To my wife and my family.

CONTENTS

LIST OF TABLES

LIST OF FIGURES

ACRONYMS

ac	Alternating Current
ALT	Accelerated Lifetime Testing
dc	Direct Current
EV	Electric Vehicle
HTGB	High Temperature Gate Bias
HTRB	High Temperature Reverse Bias
IGBT	Insulated-gate Bipolar Transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PoF	Physics of Failure
PWM	Pulse-Width Modulation
RUL	Remaining Useful Lifetime
Si	Silicon
SiC	Silicon Carbide
TC	Thermal Cycling
TS	Thermal Shock

CHAPTER 1

INTRODUCTION

1.1 Electric Vehicle Charging

Electric vehicles (EVs) continue to represent a shift toward a more sustainable future of transportation. Figure 1.1 highlights this trend over recent years for light-duty vehicle sales, where hybrid, battery electric, and plug-in hybrid together made up a 16% share in 2023. Though a steady increase is seen, there are still concerns which are hindering the widespread adoption of EVs.

One critical aspect that impacts the viability of EVs is the availability and reliability of charging infrastructure. EV chargers can be categorized into three types: Level 1, Level 2, and Level 3 (dc fast charging). Level 1 chargers are typically used in residential applications for slow, overnight charging with low power. Public chargers are typically Level 2, but there is an increasing number of Level 3 chargers due to the higher power capabilities, which results in much shorter charge times. Accessible and reliable charging stations are essential to ensure users have positive experiences, thereby alleviating concerns of range anxiety. Recent studies, such as the annual EV experience public charging study by J.D.

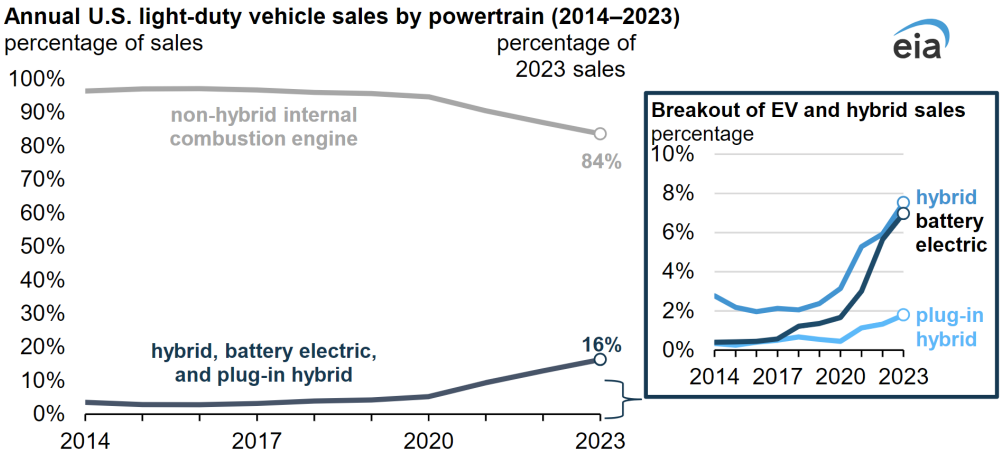


Fig. 1.1: EV Sales Over Recent Years [1]

Power, highlight the challenges that EV users experience with charging [4]. Results of this study show that 20% of users across the U.S. experience non-charge events, which heavily indicates the lack of reliability. Customer satisfaction on public Level 2 chargers has reached the lowest it has ever been since the start of the study in 2021. Similarly, the satisfaction ratings decreased even more for Level 3 dc fast chargers. Ensuring reliability is essential to overcome these frequent challenges and accelerate EV adoption.

1.2 Power Converter Applications of Silicon Carbide MOSFETs

Recent advancement in power electronics devices has increased the use of wide-band-gap devices such as Silicon Carbide (SiC) metal-oxide-semiconductor field-effect transistor (MOSFETs) in various power conversion systems. These SiC MOSFETs are now commonly seen in newly deployed applications such as EV charging [5–8] and renewable energy applications [9], owing to their increased efficiency, thermal capabilities, switching frequency, and power density.

However, as the utilization of SiC MOSFETs continues to increase, there is a pressing need for a comprehensive understanding of their reliability. Unreliability in power conversion systems presents itself as unscheduled downtime, frequently extending over prolonged periods, thereby posing challenges for both users and owners/operators. In EV charging equipment, reliability issues lead to user frustration, heightened range anxiety, negative perception of EVs, and loss of revenue from decreased use and increased maintenance costs. Similarly, in renewable energy power conversion systems, reliability concerns may lead to operational disruptions, loss of revenue from decreased output, and increased maintenance expenditures.

Given these challenges, prioritizing reliability considerations during deployment of SiC MOSFET-based systems is essential. Through enhancing understanding of reliability implications, stakeholders can ensure smooth integration and operation of the continually advancing technologies.

1.3 SiC MOSFETs Power Cycling Accelerated Lifetime Testing

SiC MOSFET failures are classified as package level and chip level failures, where possible failure locations include gate oxide, body diode, solder joints, and bond wires. At each of these failure locations, there exist physical parameters to monitor that drift over time. To gain a better understanding of the reliability of these devices, a technique known as accelerated lifetime testing (ALT) that has previously been widely deployed on Silicon (Si) MOSFETs and insulated-gate bipolar transistors (IGBT) is now being used on SiC MOSFETs [10–12]. The purpose of the accelerated testing is to put the device under high stress conditions and monitor specific characteristics that can indicate a change in state of health. The result of ALT is data which can be used to develop technologies used in online health monitoring. Many types of ALT exist including high-temperature gate bias, high-temperature reverse bias, power cycling, thermal cycling, and thermal shock, but it is seen that power cycling is the preferred test [10, 11].

The two types of power cycling tests on semiconductor devices are known as alternating current (ac) and direct current (dc) tests. In each of these, power cycling is used to thermally cycle the device, which results in expansion and contraction. However, each test has different effects on the physical structure of the device, and therefore different physical characteristics are monitored throughout the tests. In ac power cycling, even the input power factor can change the effects on the failure locations, but it affects the device on both package level and chip level. In dc power cycling, it is seen that the effects are high on the package level locations including the die attachment and bond wires [13].

The focus of this thesis is to provide the data which is necessary to understand the reliability of SiC MOSFETs used in power converter applications. With this data, equipment health monitoring, remaining useful lifetime (RUL) analysis, and preventative maintenance can all be developed and deployed for the variety of systems in which SiC MOSFETs are used. To produce this data, it is desired to perform the commonly used power cycling ALT while consistently monitoring device on-resistance (R_{DS_on}).

CHAPTER 2
BACKGROUND AND LITERATURE REVIEW

2.1 Wide-bandgap MOSFETs

The rise of wide-bandgap technologies signifies a groundbreaking development in the field of power electronics. Previous use of Si brought challenges in development in both onboard and off board EV charging due to the need for larger passive components and high cooling demands [14]. SiC MOSFETs have enhanced the performance of EV charging systems through increased efficiency, increased thermal capabilities, and higher power density [9].

The advantage of wide-bandgap chemistry on efficiency is seen through a reduction in both conduction and switching losses. MOSFET conduction loss (P_{con}) is calculated using equation 2.1, where P_{con} is proportional to R_{DS_on}. As seen in equation 2.2, MOSFET switching loss (P_{sw}) is directly proportional to the switching frequency (f_{sw}). However, the significance of the SiC MOSFETs is the reduced gate charge (Q_G), which directly relates to a decrease in both the rise time (t_r) and fall time (t_f), therefore decreasing P_{sw}. As a result of the overall reduction in loss, systems that incorporate SiC MOSFETs can push the limits of efficiency [15].

$$P_{con} = I^2 * R_{DS\_on} \tag{2.1}$$

$$P_{sw} = 0.5 * V * I * (t_r + t_f) * f_{sw} \tag{2.2}$$

As shown by the authors in [16], the thermal performance of SiC MOSFETs is superior to Si under many different loading conditions. The SiC MOSFETs thermal capabilities allow for better heat dissipation, which is crucial especially in high power conversion systems.

Resulting benefits include less device wear down due to reduced stress and improved system capability to perform in variable operating conditions. The power density improvement is useful in systems where size constraints exist, especially as the power requirements for EV charging equipment are consistently on the rise. Power density improvement comes from increased f_{sw}, increased thermal conductivity, and reduced loss. In general, it is seen that passive components including capacitors and inductors shrink with the increased f_{sw}. Due to these improvements in thermal conductivity and reduced loss in the system, cooling requirements are significantly lower and therefore so is the size of cooling equipment.

2.2 Remaining Useful Lifetime Estimation

Although the primary focus of this thesis does not center on estimating the remaining useful lifetime (RUL) of SiC MOSFETs, it constitutes a potential outcome of future research stemming from this work. A significant objective in this field, as emphasized in [17], is the ability to estimate RUL for entire systems, rather than individual components. However, before achieving system-level RUL estimation, a comprehensive understanding of long-term behavior and reliability of individual electrical components is essential. Given the relative novelty of SiC MOSFETs, there is a lack of confidence in their long term reliability, as comprehensive assessments have yet to be conducted. Various techniques have been explored to evaluate RUL and create algorithms and models for lifetime prediction including data-driven approaches, Physics-of-Failure (PoF) models, or a combination of the two [2, 18, 19]. Accelerated lifetime testing (ALT) is commonly employed to gather the necessary data for modeling, involving subjecting components to extreme stresses comparable to those encountered in real world applications.

2.3 Accelerated Lifetime Testing

Accelerated lifetime testing is a methodology often used to characterize long term reliability of a system or device in a time shorter than the actual expected lifetime. Before the reliability of a whole system can be understood and estimated, reliability of individual components of a system must be understood. This includes understanding the performance

of devices under unique conditions as well as how the device changes over time after extended use. To do this, the ALTs identify potential failure mechanisms and weaknesses under different types of extreme stresses and conditions. Generally, the steps for running ALT are: (1) stress selection, (2) test design, execution, and data collection, (3) result analysis and interpretation. When it is desired to understand reliability of semiconductor devices, this general process is widely followed. This section provides insight into running ALT on SiC MOSFETs.

2.3.1 Stress Selection

For the stress selection phase of ALT of SiC MOSFETs, it is crucial to first understand the failure modes and indicators present at both the chip and package levels. While Figure 2.1 shows a chip level structure of a SiC MOSFET, Figure 2.2 shows the package level structure. Chip level failures often come from critical areas including the gate oxide and body diode. Common package level failures occur at solder joints (die attach and substrate attach) and bond wires. Due to device packaging, it is difficult to directly monitor and assess the health of the failure modes, so the use of physical (failure) indicators is common.

Common indicators of failure at the gate oxide include gate leakage current (I_{gss}), change in voltage threshold (ΔV_{th}), drain leakage current (I_{dss}), and Miller Plateau (V_{gs_mp}). Indicators for failure at the body diode include I_{dss} and body diode forward voltage (V_F). Indicators for failure at the solder layers include thermal resistance ($R_{\Theta JC}$) and solder layer resistance. Finally, indicators for failure at the bond wires include on-state drain to source voltage (V_{ds_on}), bond wire resistance, and R_{DS_on} [2]. With the knowledge of the failure modes and indicators, the type of ALT can be chosen based on the desired targeted failure.

2.3.2 Test Design, Execution, and Data Collection

High temperature gate bias (HTGB) is a test where a device is placed under the maximum temperature rating, then the gate is biased at either the maximum or minimum voltage for an extended period of time. As shown in [20], testing under the HTGB conditions shows promising results. The authors used V_{th} and R_{DS_on} as the failure indicators, and

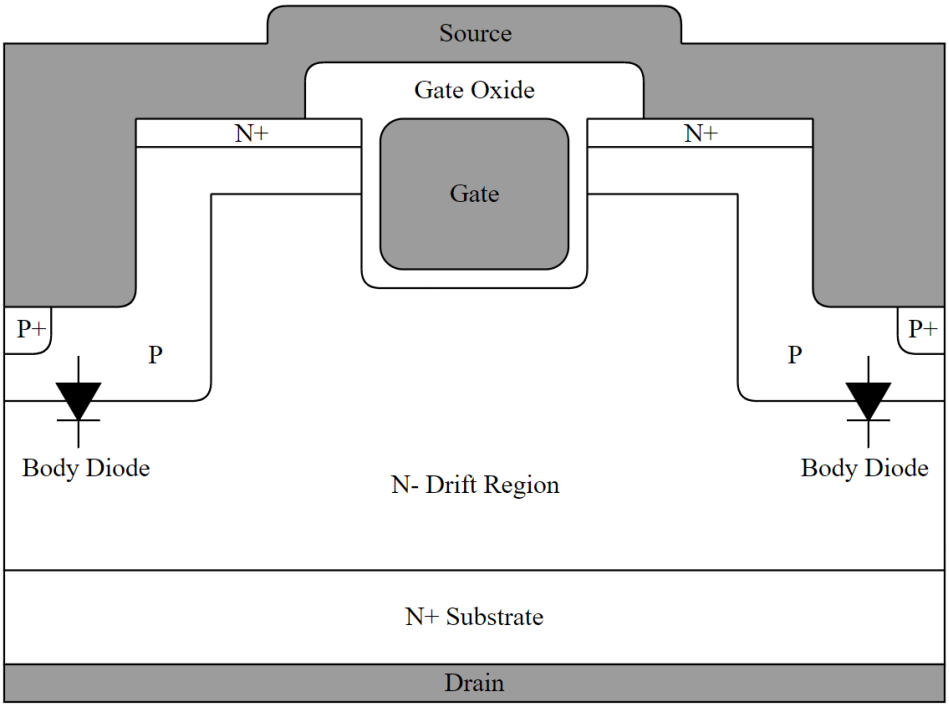


Fig. 2.1: Chip Level Structure of a SiC MOSFET

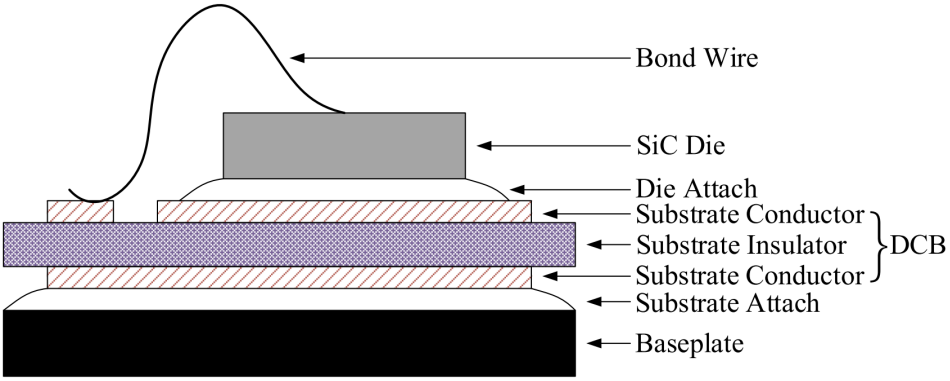


Fig. 2.2: Package Level Structure of a SiC MOSFET [2]

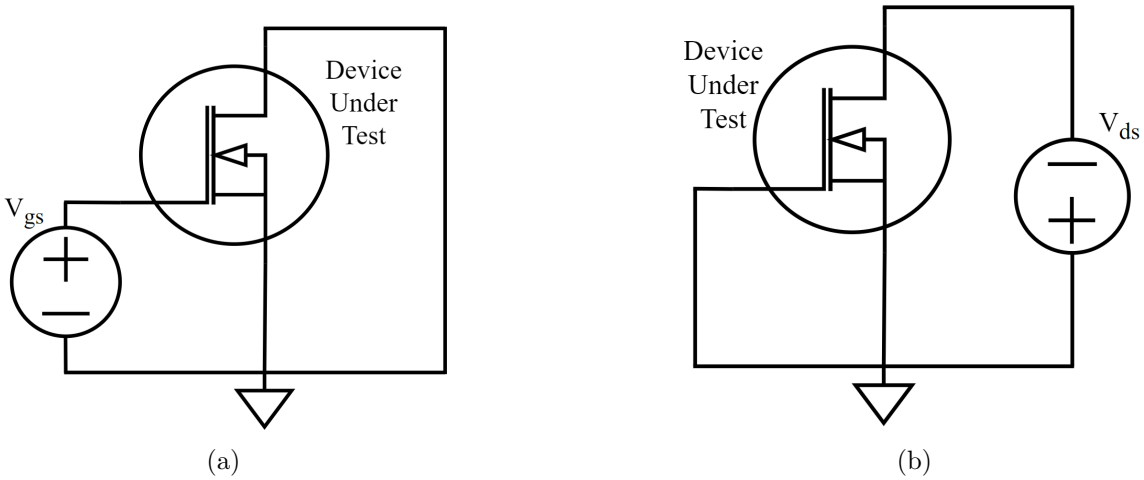


Fig. 2.3: (a) High temperature gate bias and (b) high temperature reverse bias

results show that both of these indicators show positive shifts over time of testing. An example test circuit for HTGB is shown in 2.3a. High temperature reverse bias (HTRB) is a test where a device is placed under the maximum temperature rating, then the device's drain to source voltage (V_{DS}) is negatively biased to a near maximum potential while the gate and source are shorted. An example test circuit for HTRB is shown in 2.3b. Testing presented in [21] shows that under long periods of stress (around 1000 hours), a significant increase in I_{gss} can be used to indicate failure of the device. In both of these tests, it is typically seen that testing is periodically interrupted to take measurements of the failure indicators instead of doing it during the testing.

Thermal cycling (TC) and thermal shock (TS) are ALTs in which the device is externally headed and cooled for extended periods of time. Both of these tests are known to target stress on the package level, where TC is used to stress the bond wires and TS is more known to stress the copper bonding of the base plate of the device. The failure indicators are R_{DS_on} and $R_{\Theta JC}$ for TC and TS respectively [2]. In TC, the junction temperature (T_j) of the device is rapidly changed, then kept at extreme temperatures for a period of time. Various testing profiles are used, but tuning of the tests is useful and is shown from the authors in [22], where they found that shorter cycle times with higher temperature swings accelerate the degradation, allowing for quick and better results to be captured. The differ-

ence between TC and TS is that the cycle duration for TS is much larger because the test aims for a more uniform heat distribution throughout the device which takes more time. Both tests are periodically interrupted for failure indicator measurement to avoid challenges of sensing during ALT operation.

Power cycling is one of the most commonly used ALT. In these tests, the devices are heated by pulses of current to cause thermal cycling of the junction of the device. Typically, the testing cycles are controlled by sensed T_j, which has predefined maximum (T_{j_max}) and minimum (T_{j_min}) values set by the user. Power cycling tests have several failure indicators that may used including R_{DS_on}, V_{th}, I_{gss}, drain to source capacitance (C_{DS}), on-state voltage (V_{DS_on}), and body diode forward voltage (V_F) [2]. Two primary categories of power cycling tests, ac and dc, are commonly used.

In the dc power cycling tests, the device is turned on for the duration of the heating portion of the cycle to utilize the conduction loss as the source of heat. Common topologies for dc power cycling tests are shown in Figure 2.4. In the ac power cycling tests, the device gate is sent a pulse-width-modulated (PWM) signal to incorporate both conduction loss and switching loss. For both tests, once T_j reaches T_{j_max}, the device turns off and external cooling such as water or fans are used to return the device to T_{j_min}. Topologies used in ac power cycling tests can range from a single device to many different complicated topologies for power converters such as the back-to-back three-phase inverter demonstrated in [13]. Various methods are employed to measure failure indicators for power cycling ALT, with measurements occurring either concurrently with the testing or through intermittent interruptions of the tests to assess the failure indicators. In many cases, it is desired to avoid interruptions in testing, so sensing circuits are included in the testing topologies, where the processing unit takes care of measurement timing.

2.3.3 Result Analysis and Interpretation

Following the conclusion of the ALT, data analysis is crucial to understand the outcomes of the testing. The collected data typically undergoes rigorous analysis to extract any meaningful behavior of the SiC MOSFET. It is typical to use data visualization through

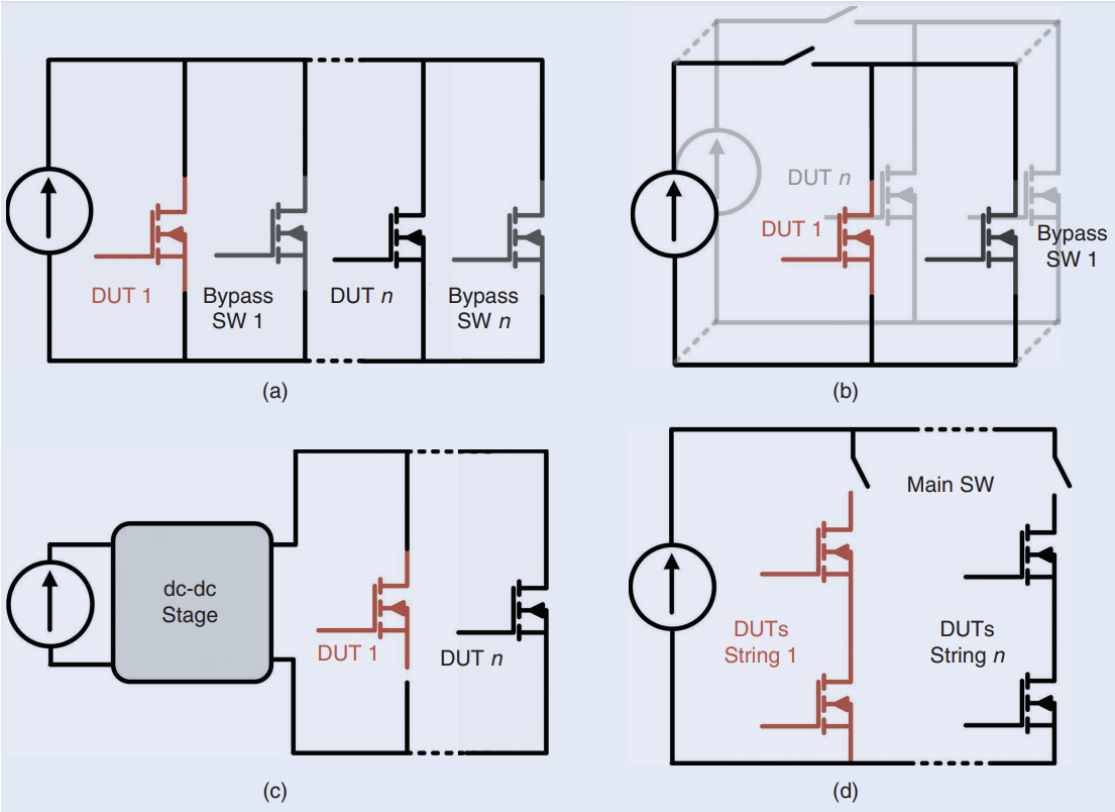


Fig. 2.4: Multi-device dc Power Cycling Testing Schematics. (a) Parallel, (b) Independent, (c) Stages Parallel, and (d) Series [3]

scatter plots and trend lines and analysis. After data analysis, conclusions can be drawn about the validity of the data by observation and comparison to expected results.

2.4 Existing Accelerated Lifetime Testing on Semiconductors Approaches and Results

Existing literature about the ALT methods and results for IGBTs often show that power cycling is the ideal test. In [23], the authors present the implementation of power cycling on IGBT devices while monitoring on-state collector-emitter voltage (V_{ce}). In this study, results clearly indicated internal damages, and sudden spikes in V_{ce} were attributed to bond wire lift offs toward the end of testing after a significant deviation from initial measurements had already occurred.

As seen in IGBT ALT, Si MOSFET ALT shows that power cycling is the preferred testing method as it continues to closely represent real world device application. In [24], a testing platform is presented for the testing of several devices simultaneously while monitoring R_{DS_on}. To perform this testing, a circuit structure similar to Figure 2.4 (a) is used, where a single current source supplying $n * I_D$ A to n devices is used. The current in each leg is not exactly balanced, but the use of bypass switches allows for devices under test (DUTs) to turn off and cool whenever necessary. From further discussion in [10], promising results were shown from several thermal patterns with ranging ΔT_j and T_{j_max}. General trends show that higher temperature threshold and swings are significantly damaging to the devices, and therefore significantly decrease total time for testing. From these results, the authors were able to employ the Coffin-Manson model to model the end of life of the devices, the Palmgren-Miner linear damage accumulation rule for RUL, and eventually Kalman filtering with exponential degradation models to provide a complete RUL estimation.

Other existing results for Si MOSFETs are presented from the NASA Ames Research Center, where ac power cycling tests were successfully employed. In these tests, various measurements including voltage, current, thermal characteristics, and semiconductor impedances at various voltage levels on the gate and drain of the device were taken [25].

The results of these experiments successfully showed degradation to the die-attach of the Si MOSFET, which is seen as an increase in R_{DS_on} after extended thermal stressing [26]. Later on, results from the experiments were used in degradation modeling with three different techniques for comparison [11]

More recently, power cycling tests are being deployed on SiC MOSFETs as seen in [12, 13, 27]. The authors of [27] demonstrate ac power cycling using a half-bridge topology which resulted in a steady increase in R_{DS_on} (measured every 1000 cycles) over the several hundred-thousand cycles. The hardware presented in [10, 24] was repurposed and demonstrated the use on SiC MOSFETs dc power cycling in [12] with R_{DS_on} as the failure precursor. These tests subject the devices to peak temperatures exceeding the rated values specified in the datasheet, revealing a consistent increase in R_{DS_on} (measured every 200 cycles) over several thousand cycles. Through the use of scanning acoustic microscopy (C-SAM) and X-ray imaging, it is seen that degradation occurred in both the die attachment and the bond wire attachment. Most recently, ac power cycling testing has been found to degrade the SiC MOSFET in both the chip level and package level locations [13]. In these tests, 3-phase back-to-back inverters using both power modules and parallel discrete devices are used to test ac power cycling tests under power factor values. The devices are removed from the tests every 300 cycles to evaluate several parameters which can be used as failure precursors including V_{th}, R_{DS_on}, reverse voltage drop V_{SD}, and parasitic capacitances.

2.5 Proposed work

The objective of this research is to develop a new method for dc power cycling ALT on SiC MOSFETs. SiC MOSFETs are being increasingly used in EV charging equipment, but this presents concerns with the lack of reliability analysis. This research will entail the design and implementation of hardware to produce data which can be used in the future for the design of lifetime modeling.

CHAPTER 3

REVISION ONE

3.1 DC Power Cycling Testing Design

To develop hardware to run the dc power cycling ALT on SiC MOSFETs, initial system specifications must be identified. First, the system is able to handle a wide range of operating points for different devices with various voltage, current, and temperature ratings. Second, the failure precursor for these tests is R_{DS_on}, which is calculated from real-time sensing results of I_D and V_{DS} through the use of Ohm's law. Also, sensing T_c is necessary to monitor the temperature of the device and control the system. Third, power cycling is applied by controlling the state of the SiC MOSFET. Control is based on the device's temperature, so the temperature swing is predetermined and configurable by the user, but remains the same for the duration of the testing. To heat the device, it is turned on to allow current to flow. To cool the device, it is turned off and active fan cooling is applied. Fourth, the system is autonomously operated from the start of test to the complete failure of the DUT. This decision is important to aid in data collection since these tests are expected to run as long as several weeks. To perform this task, the system controller communicates with a PC for the duration of the tests to provide data and receive control signals. Fifth, the circuit used is a single module of parallel MOSFETs as shown in Figure 3.1. The left SiC MOSFET is the DUT, and the right SiC MOSFET is the secondary, which is used to carry current while the DUT is in the cooling portion of the cycle.

Considering these initial specifications, system level design takes the structure as shown in Figure 3.2. In this system, a field-programmable-gate-array (FPGA) is chosen as the controller to provide configurability. The FPGA is used to communicate with the PC through a MATLAB interface. In combination, the PC and FPGA controls the states of the SiC MOSFETs, controls cooling, and reads sensed values for voltage, current, and

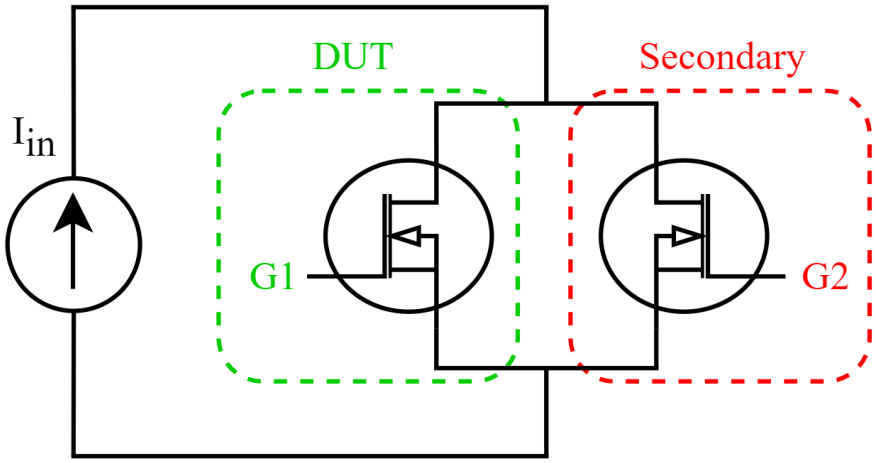


Fig. 3.1: System Circuit

temperature. The dc supply is set to feed constant current to either of the SiC MOSFETs, so there is no need to have control over it. Since this supply is in constant current mode, the voltage across the parallel devices is expected to be low, but will change over time of testing as R_{DS_on} increases. To carry out all of these design specifications, this project will have a large amount of both hardware and software design, which are discussed in the following sections.

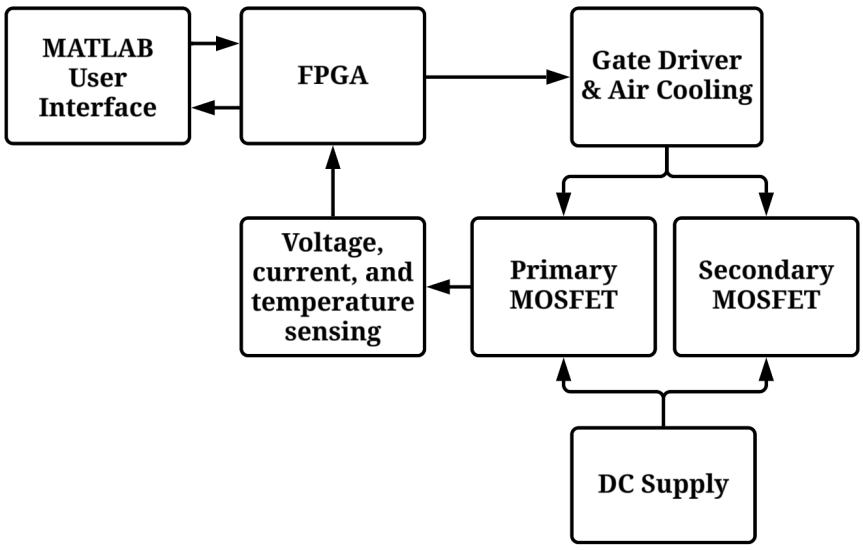


Fig. 3.2: System Block Diagram

3.2 Hardware Design

The hardware in this system consists of one FPGA, two SiC MOSFET and gate driving circuits, one voltage sensing circuit, one current sensing circuit, one temperature sensing circuit, and two controllable brush-less dc (BLDC) fans.

3.2.1 SiC MOSFETs and Gate Drivers

To determine the hardware requirements for the SiC MOSFET and gate driver circuits, a survey of currently implemented technologies was taken at Utah Power Electronics Laboratory (UPEL). The selected SiC MOSFET (NVH4L020N120SC1) for this system is one used in a megawatt wireless charging system [6]. The electrical characteristics of this device are a typical $R_{DS\_on} = 20\ m\Omega$, $I_{D\_MAX} = 102\ A$, and breakdown voltage $V_{(BR)DSS} = 1200\ V$. This is a discrete device in a typical TO-247-4L package, so only small changes would need to be made to the hardware to allow other devices of the same package to be tested. The gate driving voltages suggested for this SiC MOSFET are $+20V$ for turn on and $-5V$ for turn off, which are typical values used for other, similar components. The chosen gate driver integrated circuit (IC), IX4351NE, has plenty of capability for this system and provides a few extra useful things including a regulated output voltage, which can be used to power ICs such as digital isolators. Though the expected voltages across the parallel SiC MOSFETs is low, the gate driving circuit implements a desaturation circuit as suggested by the datasheet.

3.2.2 Sensing

In this system, it is necessary to measure synchronized V_{DS}, I_D, and T_c to correctly calculate the failure indicator R_{DS_on} as well as control the system. The main goal of this research is to collect data, so accurate sensing is absolutely crucial to ensure the quality.

For the voltage and current sensing circuits shown in Figures 3.3 and 3.4, a fully differential amplifier (FDA) and a differential successive approximation register (SAR) analog to digital converter (ADC) to read values and send them to the controller. Differential signals

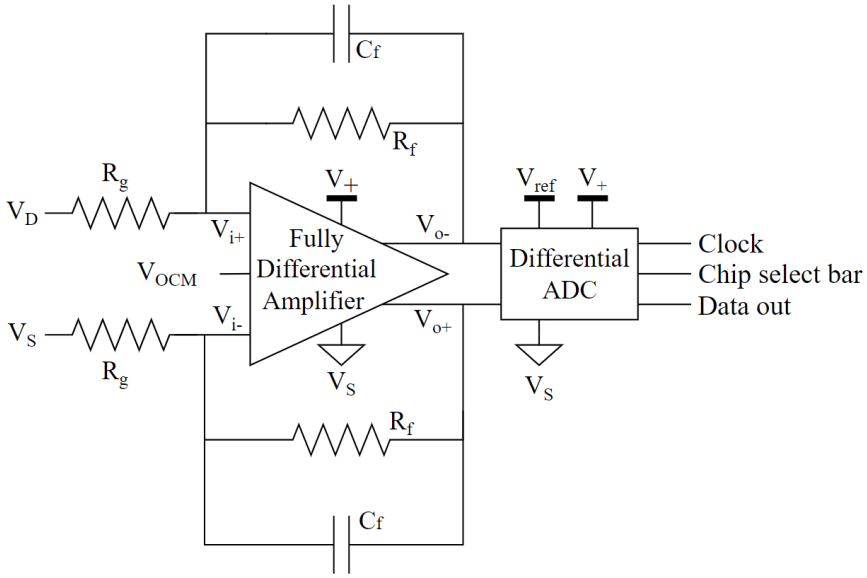


Fig. 3.3: Voltage Sensing Circuit

are used for common mode noise rejection, which can be common in printed circuit boards (PCB).

In the voltage sensing circuit, the two voltage input pins to the FDA, V_{i-} and V_{i+}, are connected to the drain and source pins of the DUT. On the output voltage pins, V_{o-} and V_{o+}, voltages amplified by the ratio of R_f to R_g are seen with a common mode of V_{OCM} and are sent to the differential ADC. The current sensing circuit utilizes a hall effect sensor

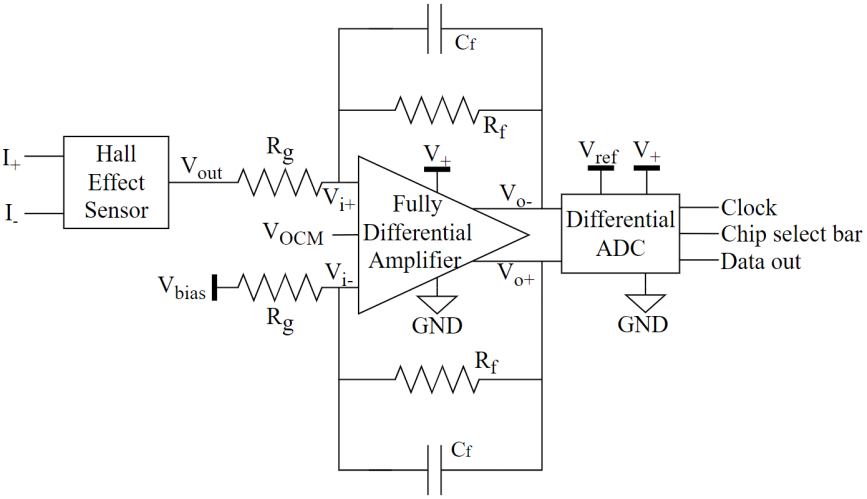


Fig. 3.4: Current Sensing Circuit

IC to translate the current passing through the chip to a voltage. That voltage is then converted to a differential signal and amplified by the FDA then fed into the differential ADC. The difference in the FDA circuit for the current sensing circuit as compared to the voltage sensing circuit is the voltage bias (V_{bias}) applied to the V_{i-} pin of the FDA. Since the voltage expected on the output of the hall effect sensor has a symmetrical, known range, V_{bias} is used to extend the output range of the FDA and utilize the full range of the ADC, which is from $-V_{ref}$ to V_{ref}.

To choose the gain resistance values, equation 3.1 is used, where $V_{out\ diff}$ is the difference of V_{o+} and V_{o-}. The FDA chosen for this design (AD8138ARZ) is specifically designed for differential ADC driving. The rail voltages are V_+ and V_s for positive and negative rails respectively. When using a $+5\ V$ positive rail and $0\ V$ negative rail, the linear operating range for this device is from $0\ V - 3.8\ V$. Using the testing operating current condition and MOSFET R_{DS_on}, the FDA input voltage can be estimated. Once the maximum expected voltage is found, it is used in equation 3.1 to find the gain, then R_f and R_g are selected to maximize the range of use of the FDA. Since the gain is dependent on only two resistance values, this circuit is easily configurable for different SiC MOSFETs which may operate at different current levels with different R_{DS_on} values.

$$V_{out\ diff} = \frac{R_f}{R_g}(V_{i+} - V_{i-}) \tag{3.1}$$

In this design, a type-T thermocouple with a range of $-200 - 370^\circ\ C$ is used to sense the DUT T_c. A thermocouple does not read the temperature at the end of the leads, it measures the temperature difference between the measuring and terminal points. This brings the need for cold junction compensation, which gets rid of the ambient temperature effects at the terminal points to give a more accurate reading. To successfully do this, a cold junction compensated IC with an integrated ADC is used. The MAX31855TASA+ is specifically made to work with type-T thermocouples with a given resolution of $0.25^\circ\ C$, so that is the chosen IC for this design.

All ADCs used in this design use passive Serial Peripheral Interface (SPI) communication which consists of three wires: clock ($SCLK$), chip select bar ($\overline{CS}$), and data out (SDO or SO). An example timing diagram for a 32-bit ADC is shown in Figure 3.5. When the $\overline{CS}$ signal goes low, the ADC begins to convert the voltage to a digital signal which is sent bit-by-bit across the SDO line at the rate given by $SCLK$.

3.2.3 Cooling

The chosen method for cooling of SiC MOSFETs in this design is through the use of BLDC fans with low gate threshold MOSFETs in series to allow for conduction control. The circuit diagram is shown in 3.6, where both fan signals come from the system controller. Large fans are desired to minimize thermal cycle duration, and therefore minimize the total ALT time.

3.2.4 Controller

The system controller chosen for this design is the CMOD-A7, which is a small 48-pin board that includes the Xilinx Artix-7 FPGA, USB-JTAG programming, USB-UART bridge, clock source, and more. Due to the use of different types of ADCs and the various ports that need controlling, this FPGA was a more than capable choice. Through digital system design on Xilinx Vivado discussed in Section 3.3.1, the FPGA is capable of reading and storing all ADC values, controlling fan and SiC MOSFET states, and interpreting and sending information across a UART line to the PC.

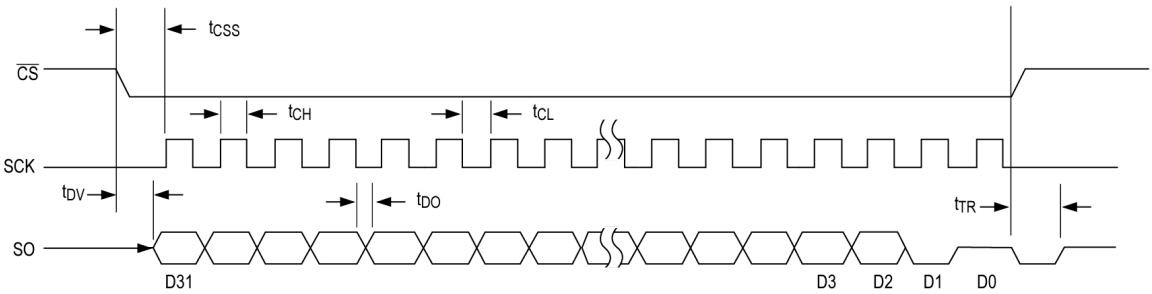


Fig. 3.5: 32-bit ADC Serial-Interface Timing

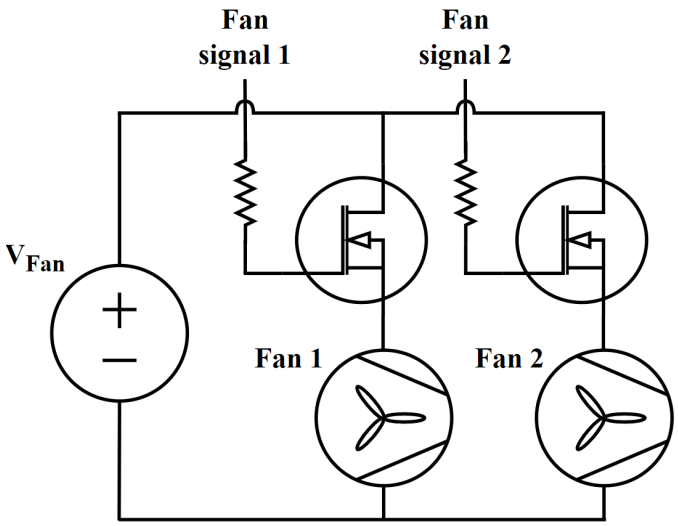


Fig. 3.6: Fan Circuit

3.2.5 PCB Layout

To design the PCB to house the previously described portions of this hardware, a list of considerations in order of importance is made. The first consideration is the placement of the SiC MOSFETs. In power electronics, one of the primary considerations of laying out semiconductor devices with gate driving circuits is to minimize the gate-to-source loop. In this case, extreme heat surrounding the SiC MOSFETs could potentially cause problems for all surrounding circuits, so a separation of 12 mm between the gate driver and the SiC MOSFET footprint. Also, the footprint for the DUT includes two different parallel ports in the case that one gets too damaged from heat during testing or soldering. The second consideration is the path of the main input current. The path was determined to take the majority of one side of the board and is laid out as a polygon with a minimum width of 32 mm. The third consideration is to place the sensing circuits as close as possible to the sensed points. The voltage and current sensing circuits take a central placement on the board next to the SiC MOSFET and input current path. The temperature sensing circuit needed to be placed along an edge of the board to allow for the thermocouple mount to plug in with minimum length thermocouple leads. The fourth is to provide separation of cooling circuit and fans from other components on the board. All components including

the cooling control MOSFETs, the fans and wire terminals, and input power filtering have space to separate from important signals such as sensing and gate drive signals. The fifth consideration is to keep all signals sent and received by the FPGA isolated from the rest of the board, so the FPGA lays on the opposite side of the board from the SiC MOSFET with the use of digital isolators to carry signals across an isolation barrier.

The final PCB layout is shown in Figure 3.7, which breaks down the board into significant sections.

3.3 Software Design

The software necessary for this system includes MATLAB and Vivado, which are used to make a connection between the user (PC) and the FPGA.

3.3.1 Vivado

The software compatible with the CMOD-A7 FPGA is Xilinx Vivado, which is used to create the bitstreams that create the digital circuit on the FPGA. The main components of

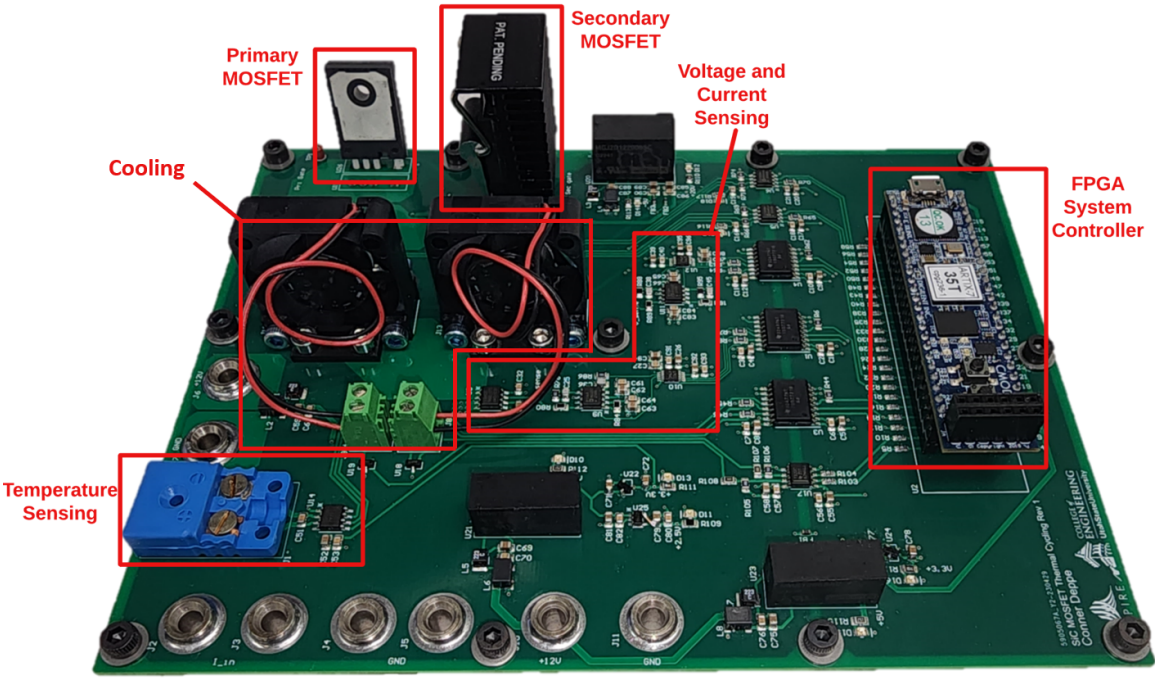


Fig. 3.7: Revision One Final PCB

the model (written in Verilog) include clock generation, ADCs, UART, parameter wrapping, protections, and controls. In this model, the clock wizard from the IP catalog is used to generate a 100 MHz clock for monitoring faults, a 300 MHz clock for parameter wrapping, a 7.3728 MHz clock which is the UART baud rate, and a 5 MHz clock used for voltage, current, and temperature sensing.

The ADCs for the voltage and current sensing circuits are both 14-bit signals, while the temperature sensing ADC outputs a 32-bit signal. Since all ADCs use passive (read-only) SPI communication, the same Verilog module is used to control all of them. The overarching control of this module comes from a $\overline{CS}$ signal that is generated in the main module with configurable sampling frequencies. The ADC module only does anything useful when the $\overline{CS}$ signal is driven low, the signals the on-board ADCs to start the conversion which is sent bit-by-bit over one line. The data is saved into one register which is complete at the end of 32 clock cycles. Results of ADC implementation are shown in Figure 3.8, where the yellow waveform is $\overline{CS}$, the blue waveform is $SLCK$, and the magenta waveform is SDO. Protections and controls for the system are implemented in the Verliog model as hard coded values that can only be overwritten through the MATLAB communication line. The protections are implemented by comparing all ADC results to the respective limits which are user controllable. To prevent potential false readings, fault registering logic exists. This logic runs on the 100 MHz clock and implements counts to register how many times the high signals is seen. Once the FPGA has seen four or more consecutive high readings, the system enable pin goes low, and no SiC MOSFETs or fan signals are allowed to go high. The different faults (over voltage, over current, over temperature, and gate driver 1 and 2) are represented on the CMOD-A7 board through an RGB led. The fault register can only be reset manually through the control variable register. The control variables in this system include system enable, global reset, DUT and secondary MOSFET states, and primary and secondary fan states. To communicate all the sensed value and control between the FPGA and user, data RAM packets are sent over the UART transmit (TX) and receive (RX) lines using code which was previously developed for another project at ASPIRE.

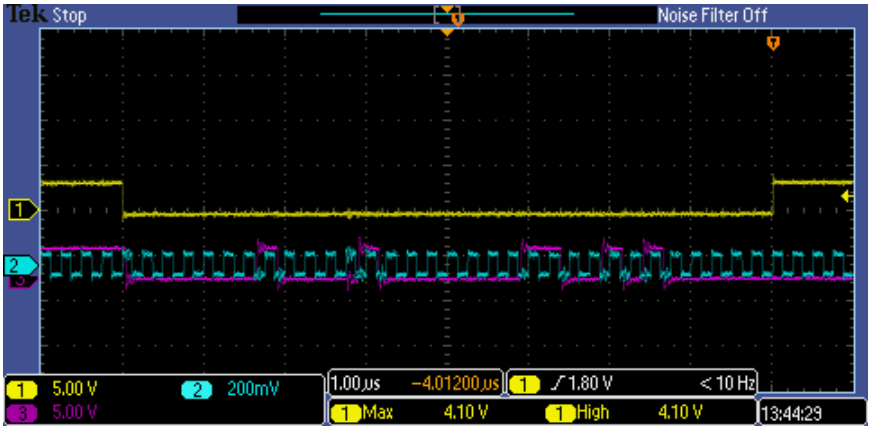


Fig. 3.8: ADC signals on oscilloscope

3.3.2 MATLAB

MATLAB is used to interpret the actions of the FPGA in order to implement the system control, which is to deliver the thermal cycles to the DUT. Figure 3.9 shows the thermal cycle pattern applied to the DUT, where one of the 10 cycles takes the temperature to a lower point than the rest. The purpose of only taking one of the 10 cycles to the lower temperature is to save time for the whole test since the lower temperature takes significantly longer than the other cycles.

The broad actions of the MATLAB script are illustrated as a flowchart in Figure 3.10. This flowchart highlights a continuous loop until the end-of-life threshold of the DUT is reached. In this testing, the end of life threshold is the actual end of life, which happens when the device fails in either an open circuit or a closed circuit. The minimum temperature of the swing is found by checking if the remainder of cycle count divided by 10 is equal to 0, implemented as the modulo operator in code. The MATLAB function continually compares the sensed temperature to the minimum and maximum desired value and switches the states of the DUT and secondary to get the desired functionality. This process is shown in Figure 3.11, where the green plot shows V_{gs} of the DUT, and the red plot shows V_{gs} of the secondary. While the T_j of the DUT is increasing, there is 20 V V_{gs} applied to the device to allow for current conduction. During this period, a -5 V V_{gs} is applied to the secondary to ensure it is turned off. In the cooling portion of the cycles, the opposite behavior occurs, where

$-5\ V$ V_{gs} is applied to the DUT and $20\ V$ V_{gs} is applied to the secondary. Additionally, the software implementation provides a small overlap time between the gate signals of the DUT and secondary to avoid creating an open circuit.

In addition to this main MATLAB process, there are two separate timer functions, called "ADC Read" and "ADC Save", running in the background. The ADC Read timer is set to run at a rate of 5 samples per second. This timer reads the ADC results from the FPGA in binary form, and translates them to the actual voltage, current, and temperature. The purpose of the ADC Save timer is to save the sensed data from the other timer function. To get rid of some minimal noise in the sensed values, this timer averages every five sensed values. With the averaged values, R_{DS_on} is calculated, and all values are saved once per second. The data is sent to a .csv file where the columns are voltage, current, temperature, resistance, and cycle count. To avoid problems with overloading .cvs files, this timer also implements counters to start saving to a new file once the current file has saved a large number of results. This timer also displays calculated results every second in the command

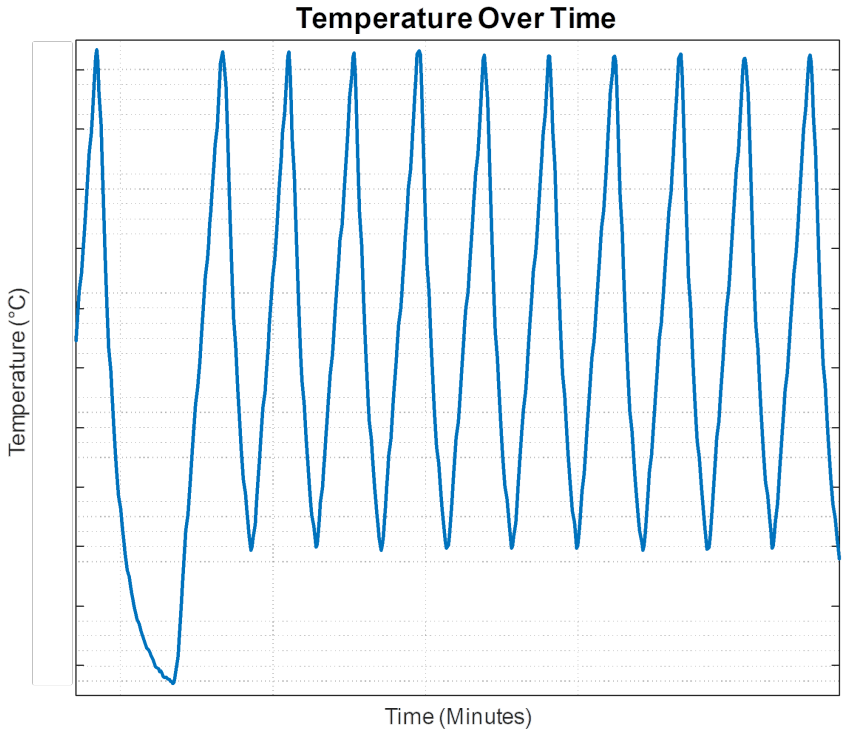


Fig. 3.9: Thermal cycles to the DUT

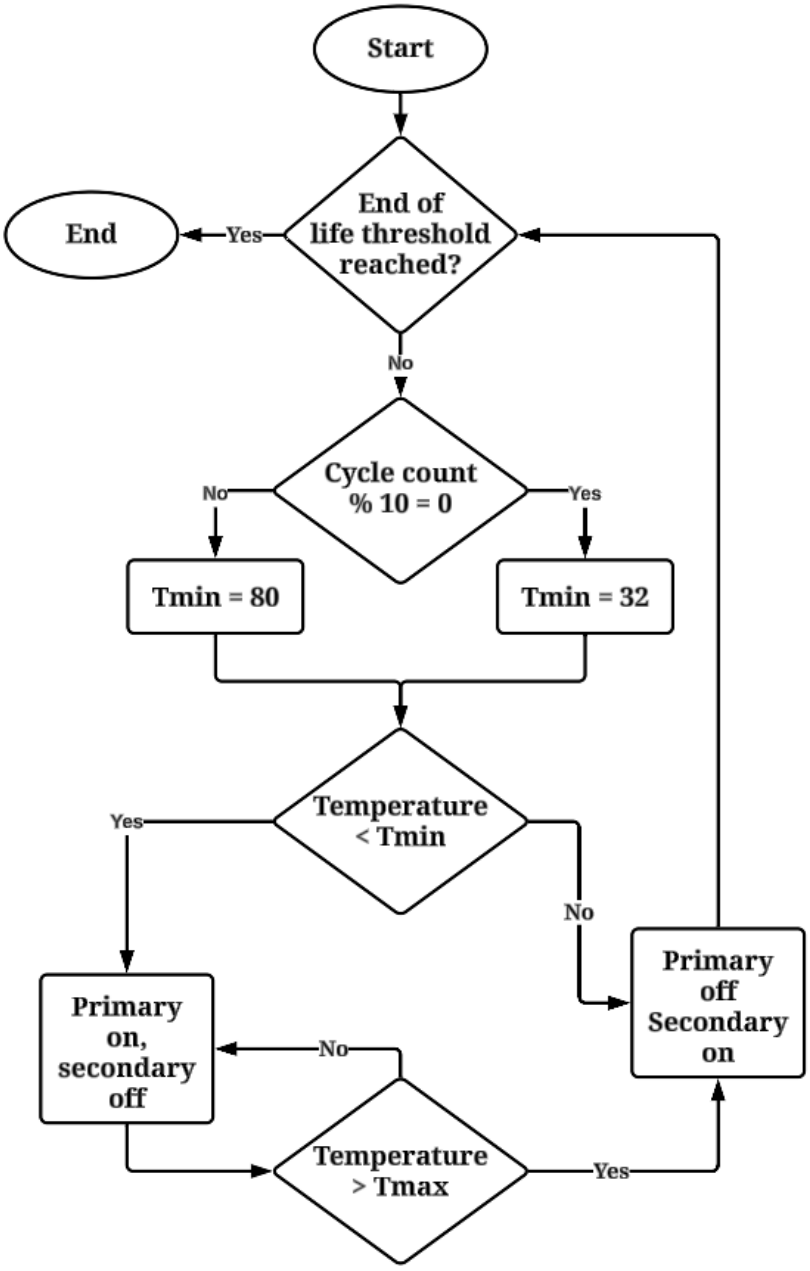


Fig. 3.10: MATLAB Script Flowchart

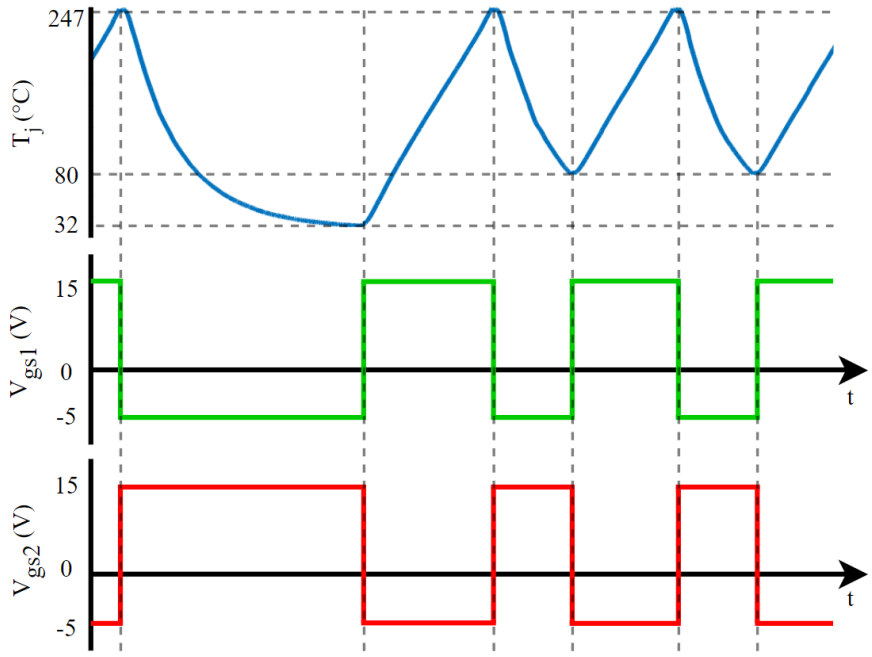


Fig. 3.11: Thermal cycles controlling the gate signals

window of MATLAB to give context as to what is happening during the test.

3.4 Whole System

Figure 3.12 shows the whole system including MATLAB, DC current and auxiliary power supplies, and the thermal cycling platform.

3.5 Lessons Learned

Though the preliminary and power cycling test results are discussed in Chapter 5 of this thesis, this section provides some key takeaways which are used to validate the first revision, allowing for the design of a second revision. In summary, these takeaways are:

- **Results are valid.** The results from power cycling ALT on revision one are as expected and will be useful in remaining useful lifetime modeling.
- **Power cycling takes a long time.** Though duration varies greatly between the tests, end-of-life may take several weeks of continuous testing.

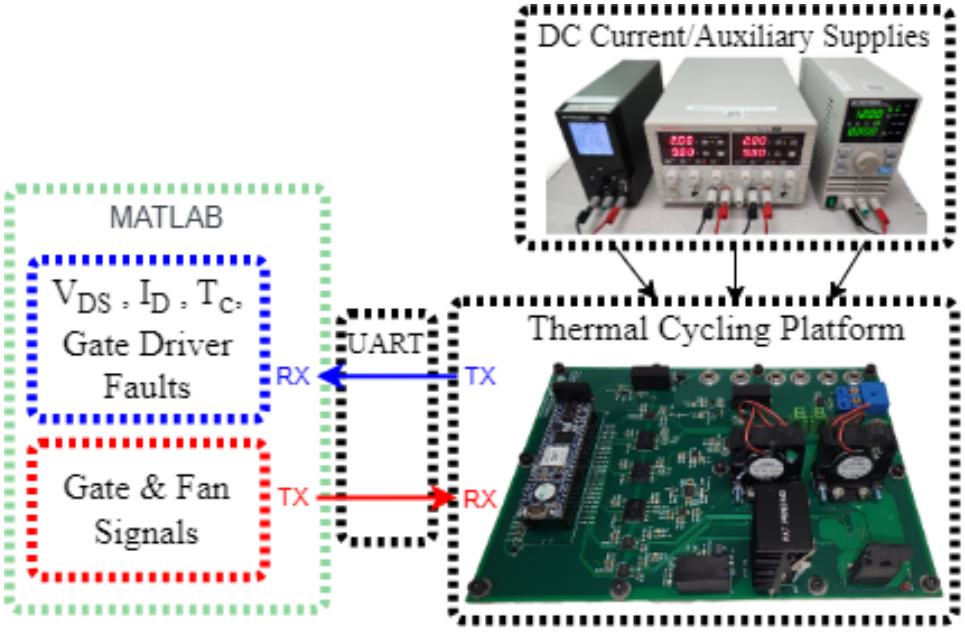


Fig. 3.12: System Diagram for SiC MOSFET ALT

- **Testing is destructive to PCBs.** The high temperature applied to the DUT has undesirable effects on the health of surrounding components, including sensing noise and gate driver faults.

- **Heating and cooling periods need to be short.** To speed up the process of testing and provide a higher level of shock, cycles should be delivered quickly. Using higher currents and bigger fans are ways to help this.

CHAPTER 4
REVISION TWO

4.1 System Design

As a result of the successful testing on revision one, it was decided that a scaled-up version was necessary to obtain data in a quicker way. Using a novel circuit design, shown in Figure 4.1, the dc power cycling test is scaled up to perform the lifetime testing on six SiC MOSFETs at a time. This circuit consists of six modules of parallel SiC MOSFETs in series to allow for easier delivery of constant current while only increasing the input voltage requirements. The driving reason for the creation of this system is to obtain more data at a quicker pace. However, this design also addresses issues with revision one presented as slow thermal cycles, PCB breakdown, and sensing signal integrity. The desire for this system is for it to not only be much more robust, but also easily replaceable in the parts of the hardware that will undergo high temperatures.

4.2 Hardware Design

Overall, this system uses nearly identical circuits to the revision one circuits. However, changes exist in voltage sensing, current sensing, high current paths, power terminals, cooling capabilities, and additional temperature sensing circuits. In this design, three separate PCBs are designed to carry out the dc power cycling. Figure 4.2 shows the system breakdown with each PCB including any intermediate connections. The three PCBs in the system include a main board, a gate driver board, and a DUT board, which will all be individually broken down and explained in the coming sections.

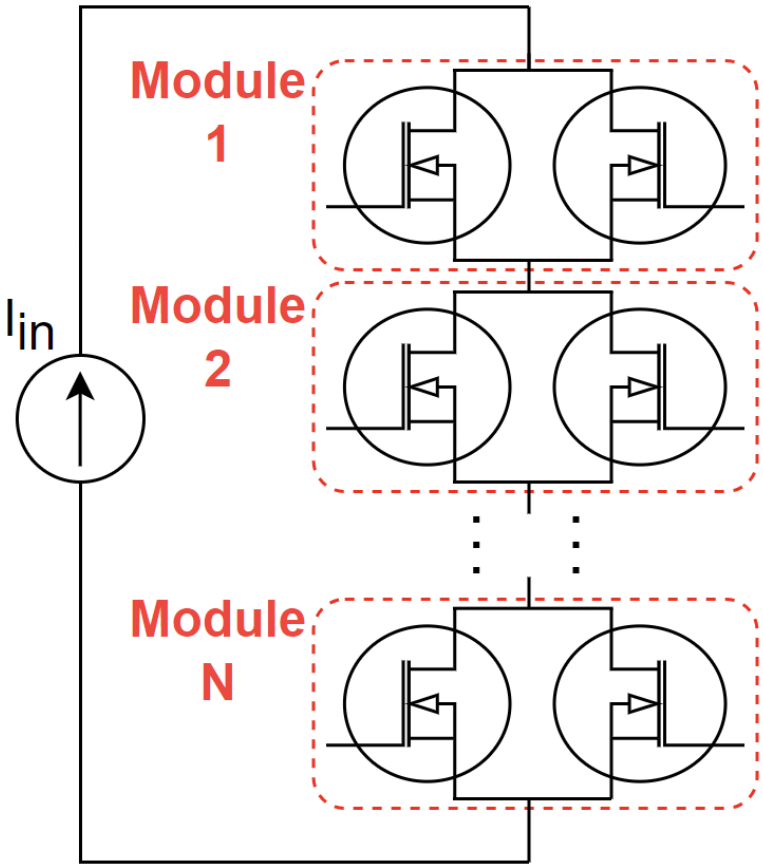


Fig. 4.1: Novel circuit topology for dc power cycling ALT.

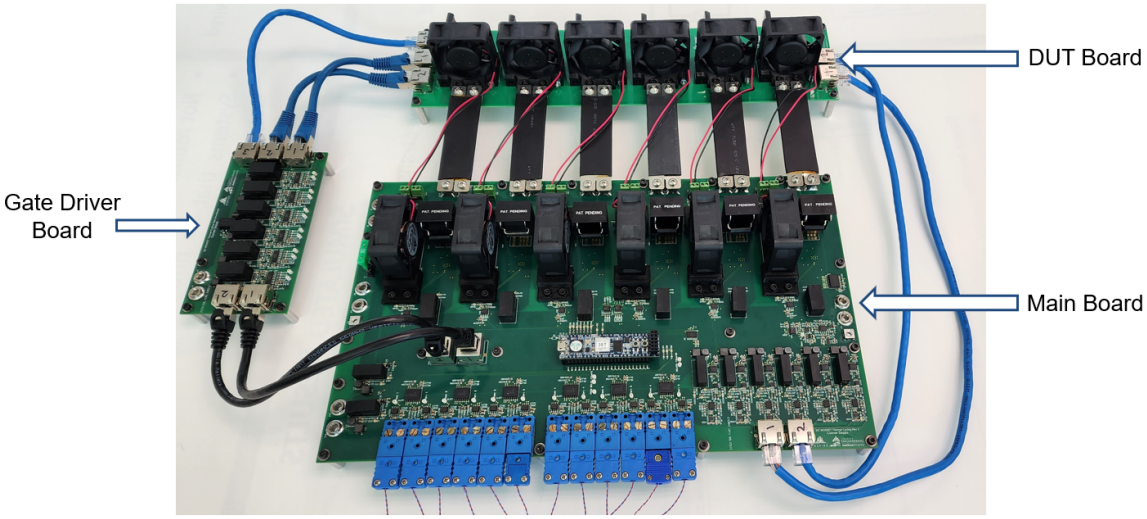


Fig. 4.2: Revision two system with three separate PCBs

4.2.1 Main Board

The main board houses the majority of components in this system including 12 temperature sensing circuits, 6 voltage sensing circuits, 1 current sensing circuit, 6 secondary SiC MOSFET and gate drivers, 4 Ethernet connectors, 1 fault multiplexer, primary and secondary fan control and wire terminals, and the CMOD-A7 FPGA for system control.

Temperature Sensing

Temperature sensing circuits remain the same as in revision one, where the type-T thermocouple voltage is read by the cold-junction compensated ADC and sent to the FPGA. The difference in this system is that the temperature of both the DUT and secondary devices in each module are sensed and saved by the FPGA. Over time, the secondary devices will also experience less severe thermal cycling during the periods of time when the DUT is in the cooling phase of the cycle.

Voltage Sensing

To sense voltage across each module of parallel SiC MOSFETs in this system, isolated circuits are used. If voltages were to be sensed across each device with non-isolated sensing, the modules closest to the input power supply would have larger voltages seen at the drain and source nodes, since the total voltage from the supply will be $6 * V_{ds}$. Isolated circuits are necessary to avoid the need for higher voltage rated circuits, which are commonly known to have errors at lower voltages. The fundamental use of a fully differential amplifier with a differential ADC remains the same. However, each voltage supply necessary to the circuit is powered by isolated supplies instead of one common supply, so there is an increase in total power supplies. Each voltage sensing circuit is fed the drain and source voltages of the primary MOSFETs housed on the DUT board to eliminate the voltage drop across the intermediate board connections. This signal is sent over an Ethernet cable using the drain and sources as twisted pairs to help with signal integrity.

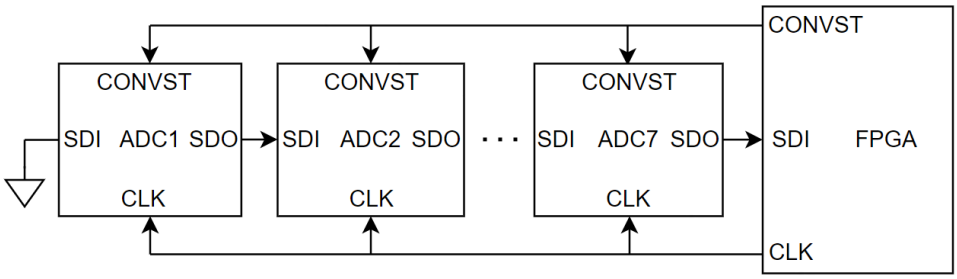


Fig. 4.3: Voltage and Current Sensing ADCs in daisy chain configuration

Current Sensing

The main change made to the current sensing circuit is the use of a new hall effect sensor with a current rating up to 30 A instead of the previous 20 A sensor in revision one. Due to this, the passive sensing components all changed to compensate for the new hall effect voltage output range.

Differential ADCs

In this design, the previous voltage and current sensing differential ADCs are replaced with new 16-bit ADCs, capable of daisy chained communication to save controller pin space. These ADCs utilize a conversion start signal ($CONVST$), clock signal (CLK), serial data in signal (SDI), and serial data out signal (SDO) to interface with a controller in read-only SPI communication.

A condensed circuit diagram of the daisy chained ADCs is provided in Figure 4.3. The chain starts with the first ADC SDI pin connected to ground, then connects the SDO pin of each ADC to the next ADC SDI pin until the seventh ADC connects the final SDO pin to the FPGA. Since there are seven 16-bit signals, the resulting final SDO signal is a 112-bit signal that needs to be interpreted in the FPGA. To interpret the data sent on the final SDO line to the FPGA, signals following the timing diagram shown in Figure 4.4 are implemented. Once the $CONVST$ signal goes high, each ADC needs time to complete the conversion. After the conversion is complete, it takes 112 clock cycles to save each bit of data, one by one.

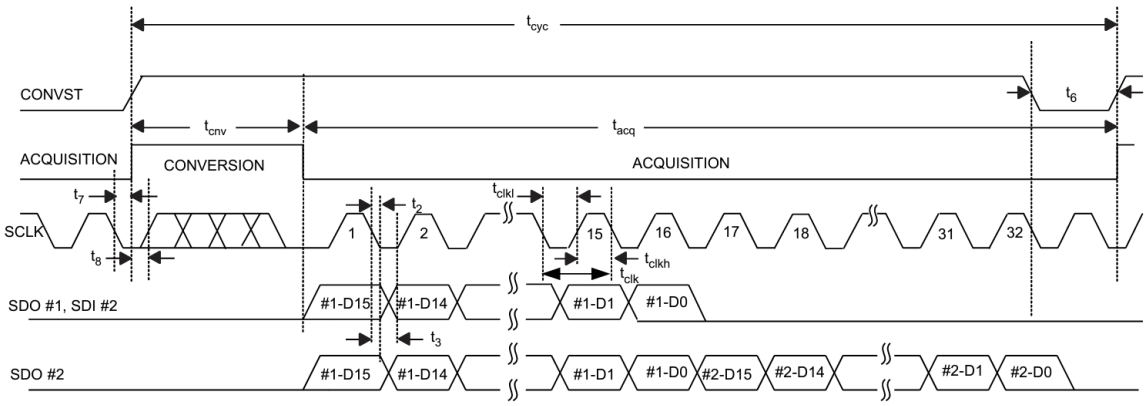


Fig. 4.4: Timing diagram for SPI communication with daisy chained ADCs

Cooling

In an effort to keep components off the DUT board, all cooling control circuits and wire terminal blocks are included on this main board. A similar cooling method is used for this board as was used in revision one. The fan control circuit diagram is included in Figure 4.5. All of the secondary fans are mounted to this PCB using 3d printed mounts. The secondary fans are all controlled through the use of a single N-channel MOSFET with a low gate voltage threshold which can be turned on by the FPGA output instead of a gate driving circuit. However, each primary fan uses a separate control circuit and signal to allow for individual module control. In this design, all the secondary fans face the same direction to create a stream of air to assist in cooling all secondary SiC MOSFETs at the same time. On this board, the DUT/primary fan control circuits and wire terminals are placed at the edge of the board closest to where the DUT board will be, so the actual fans remain on that board. Once again, all fans are powered using a separate supply than the rest of the board is using to avoid interference and noise.

Fault Multiplexing

To limit required pin usage of the FPGA, a 16:1 multiplexer is used to condense the 12 gate driver fault outputs to a single signal. Instead of 12 FPGA pins, operating this circuit only takes 5: 4 for the select signals and 1 for the multiplexer output signal. To observe fault signals, the select signals are used as a four-bit signal that counts from 0-15. Since the

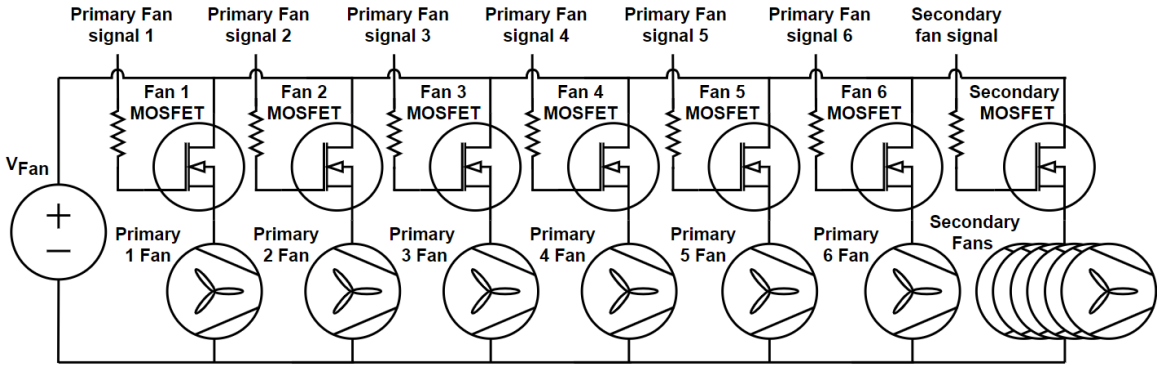


Fig. 4.5: Cooling Circuit

gate driver fault signals are active low signals, the extra four pins on the fault multiplexer are tied to +3.3 V. The FPGA model to interpret the fault signals is described in Section 4.3.

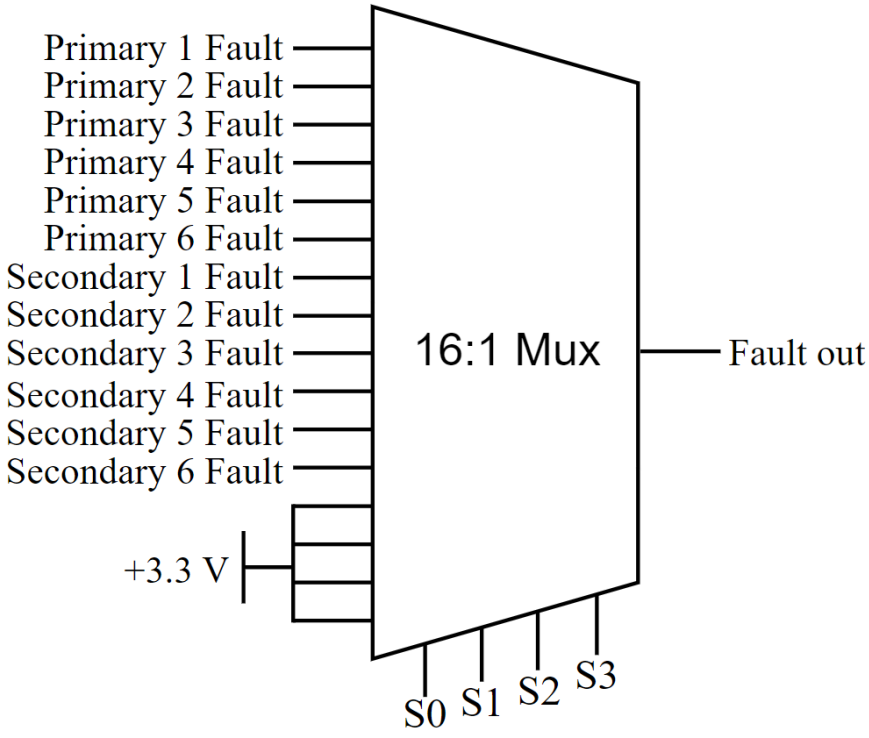


Fig. 4.6: Fault multiplexer inputs and outputs

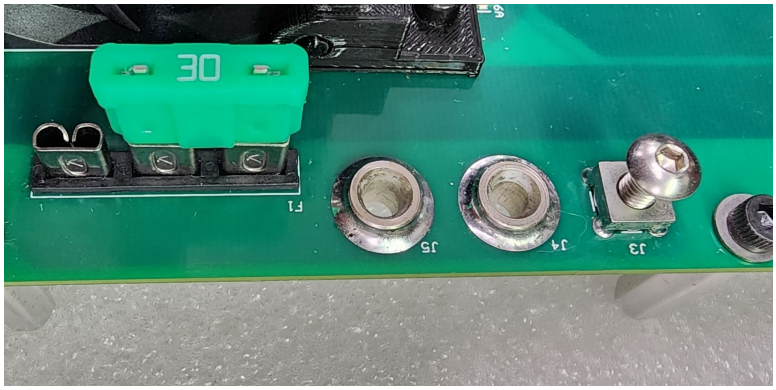


Fig. 4.7: Input power connectors

Input Current

In this new design, the input current connectors include two banana cable ports, each rated at 15 A, and one M4 screw terminal rated at 50 A. In addition to input ports, the input fuse is now included as a part of the PCB to avoid the use of inline fuses, but keep the extra level of protection. Both of these are shown below in Figure 4.7.

Finalized Main Board PCB

The finished PCB which includes all hardware described in previous sections and more is shown in figure 4.8. At the top of the board, between the fan power and control circuits, are the terminals for the bus bars which connect to the DUT board to connect the DUT and secondary devices in parallel. Below the terminals and cooling circuits, the secondary SiC MOSFETs and fans are all in line for a single path of airflow. The other part of the board is used for sensing, communication between boards, and for housing the FPGA system controller.

4.2.2 Gate Driver Board

The purpose of the gate driver board is to interface between the main board and all six SiC MOSFETs on the DUT board. The same driver and surrounding components are used as were in the first revision. This board contains six repeated, isolated gate driver circuits, input power terminals, and five Ethernet ports for communication described in

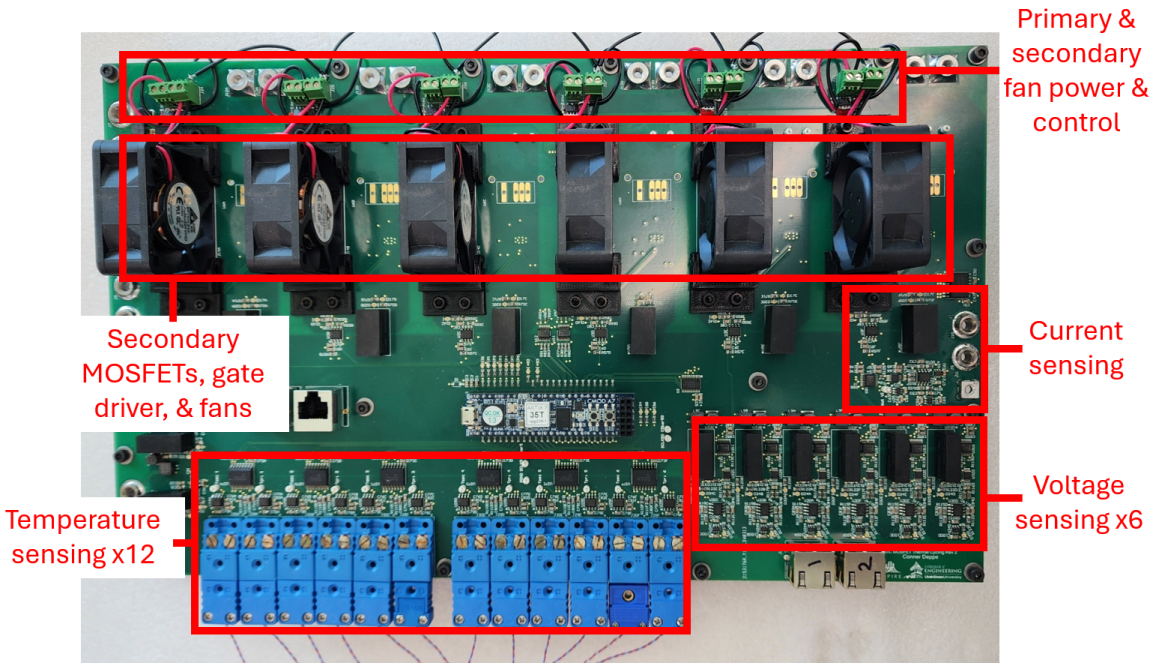


Fig. 4.8: Main PCB

Section 4.2.4. The finalized PCB is included in Figure 4.9.

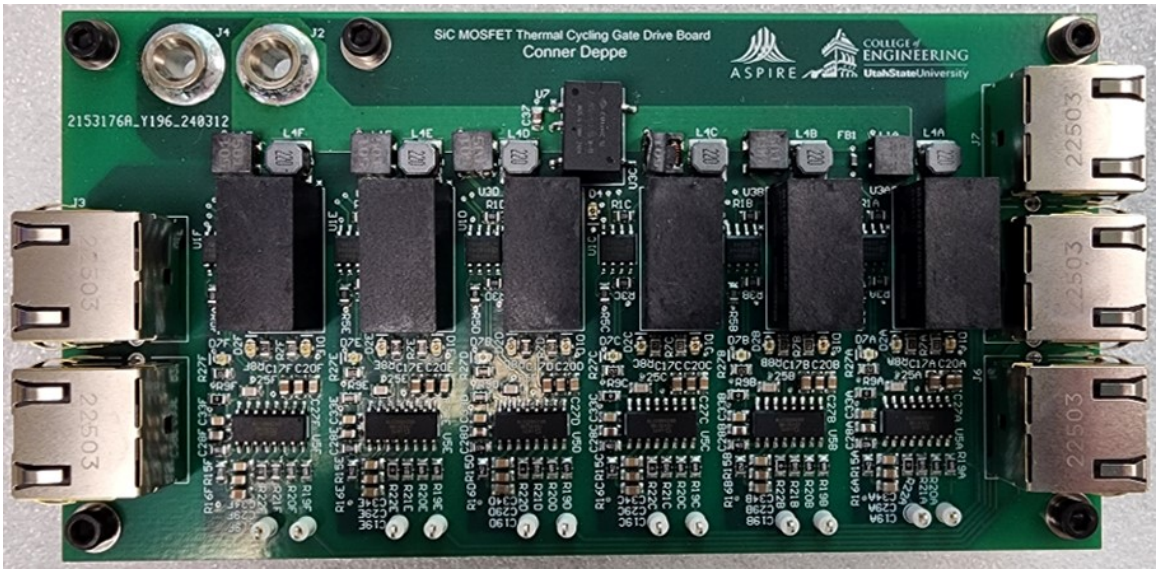


Fig. 4.9: Gate Driver PCB

4.2.3 DUT Board

The DUT board is designed to be robust, but low cost at the same time due to the expected deterioration caused by the high temperatures. This PCB is shown in Figure 4.10. The components housed on this PCB include 5 Ethernet ports, 12 soldered screw terminals for the bus bars, 12 diodes and 6 resistors for turn on/off of each DUT, and the DUTs themselves. The fans are mounted to this PCB using 3D printed mounts, but as stated before, the controls and wire terminals to power the fans are on the main board. Each DUT on this board has a separate fan, and each fan is pointed in the same direction placed next to each other to avoid interference with the other DUT and fans. Each DUT module on this board has 5 footprints as shown in the close-up image in Figure 4.11. These footprints have been slightly adjusted as compared to the previous revision. Each hole for the SiC MOSFET pins has been extended vertically to provide more space for heat to disperse to, as well as more space to apply solder.

4.2.4 PCB Connections

In this system, there are various connections between boards and the PC. The connection to the PC remains as a USB cable plugged directly into the FPGA using a UART line for communication. Since the modules of parallel SiC MOSFETs have the DUTs and secondary device housed on separate boards, custom bus bars are used to make the drain-to-drain and source-to-source connections between them. These 110 mm long bus bars are

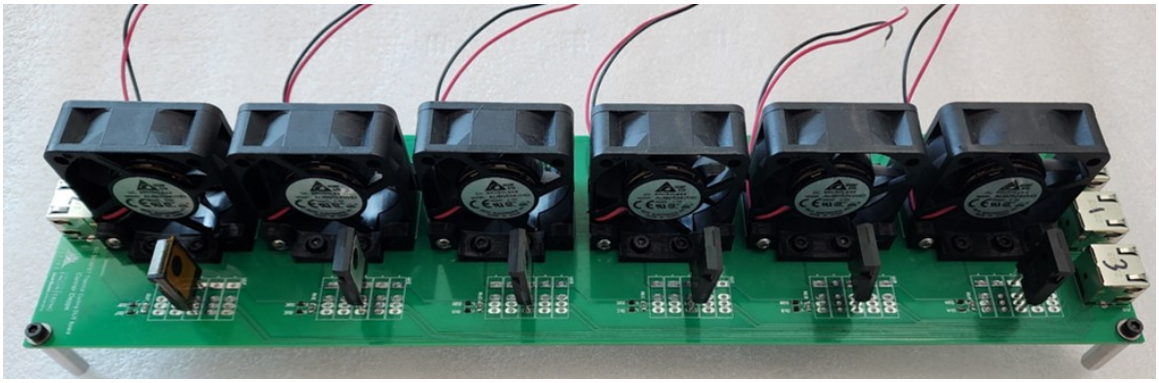


Fig. 4.10: DUT PCB

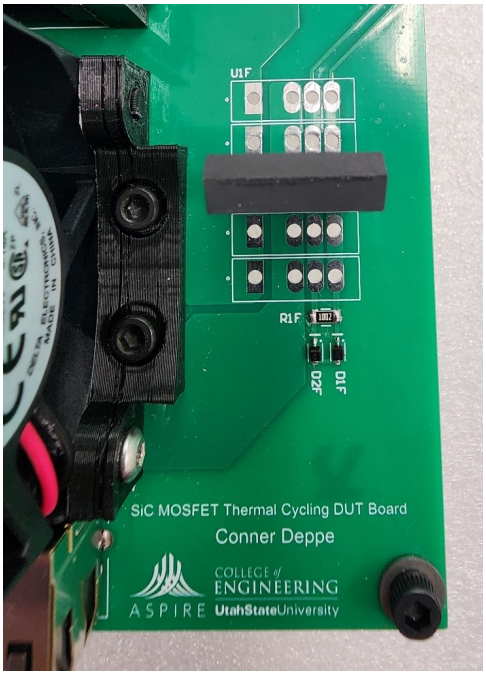


Fig. 4.11: Single DUT module with footprints

Fig. 4.12: Custom bus bars

shown in Figure 4.12. The length of these bus bars is useful to give separation of boards and allow for the fans on the DUT board to pull air through the fans that is not coming off the main board.

The rest of the inter-board connections are made through 7 total Ethernet cable connections. The main board has 4 ports, the gate driver board has 5 ports, and the DUT board has 5 ports. The communicated signals between the boards is illustrated in Figure 4.13, where the blue connections represent shielded cables and the red represent unshielded cables. The main board houses the FPGA, so two Ethernet ports are utilized to interface with the gate driver board to send gate signals and receive fault signals. These two ports

are shielded because the PCBs share a common ground. On the gate driver board, there is an isolation barrier between the input signals and each gate driver module. The output voltages ($+20\ V$ or $-5\ V$) are sent to the DUT across an unshielded Ethernet cable, since each module is held at a different potential. Each gate voltage is wound as a twisted pair with the return path from the same module. These signals take two Ethernet ports, and the remaining port is used to receive the 6 drain voltages which are used in the gate driver circuits for fault detection. For voltage sensing, the DUT board sends drain and source voltages over 2 Ethernet ports to the main board, which does all the signal conversion.

4.3 Software Design

The software design approach for this system is similar to the design in revision one, but this needs to be scaled to run six separate tests. In this software system, MATLAB remains the source of control for all modules, and the Verilog model written in Vivado is used to carry out nearly the same functionality.

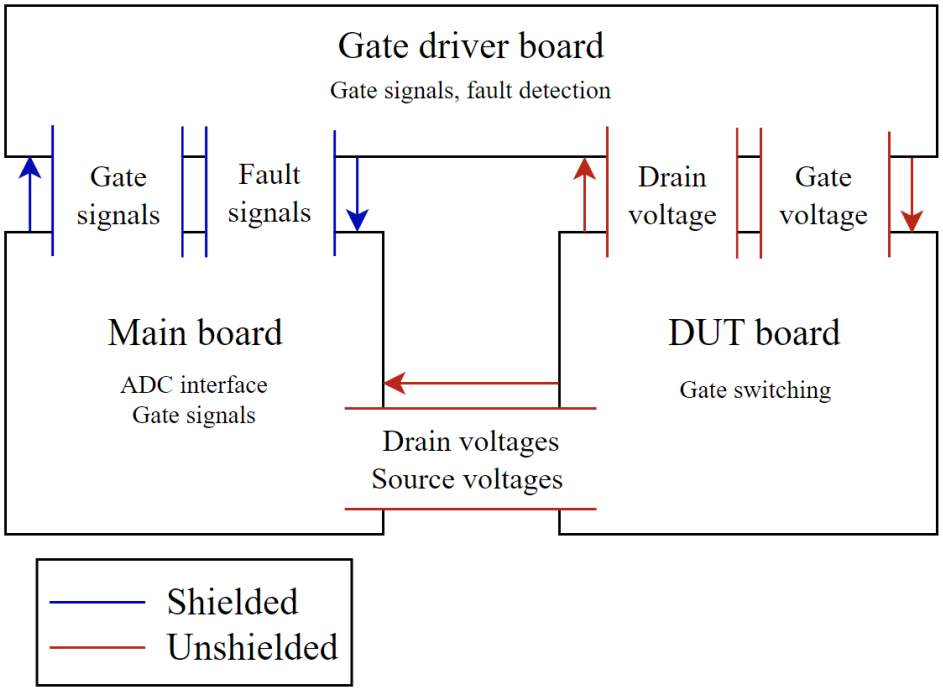


Fig. 4.13: Ethernet connections between PCBs

4.3.1 Vivado

The Verilog model in this system includes two separate types of ADC modules, clock generation, UART communication and parameter wrapping, and fault multiplexer interpretation.

Each of the 12 temperature ADCs has their own instances of an ADC interpretation module, which works exactly the same as in revision one. Since the voltage and current sensing ADC are in the daisy chain configuration, there is a single ADC interpretation module inside the Verilog model. To interface with these ADCs, the timing diagram represented in Figure 4.4 must be met. There are two main special considerations when interfacing with these daisy chained ADCs. First, it is necessary that the $SCLK$ signals must be low at the rising edge of the $CONVST$ signal, which is used to tell the ADCs to start the conversion. Second, there must be at least 1400 ns conversion time (t_{cnv}) before data is able to be transmitted. To interface with these ADCs, a 10 MHz clock signal is used, which means there needs to be 14 clock periods before data begins to be transferred. At the end of the conversion period, data begins to be transferred through the chain, starting with the ADC in the part of the chain farthest from the FPGA. Each ADC requires 16 clock cycles before transmission is complete, so this data transmission takes a total of 112 clock cycles, and the whole period of the $CONVST$ signal is 126 clock periods. Once the data transmission is complete, the 112-bit register is broken down by 16-bit pieces for each sensed value, which is then saved to the register which is transmitted to MATLAB across the UART.

In this new system, the UART and parameter wrapping modules are adjusted to fit 16-bit ADC data inside a RAM block, instead of the previous 14-bit data. The data transferred over UART now has 1 control register, 3 fault registers, 19 ADC signals, and 12 SiC MOSFET control signals. The control register includes a system enable, global reset, six fan signals for DUT fans, one fan signal for the secondary fans, and a fault multiplexer enable control.

To interpret the fault signals using the multiplexer, a cyclic Verilog module is written to loop through the select bits continuously to monitor all fault signals. Using a 50 Hz clock,

S3	S2	S1	S0	Output
0	0	0	0	In 1
0	0	0	1	In 2
0	0	1	0	In 3
0	0	1	1	In 4
0	1	0	0	In 5
0	1	0	1	In 6
0	1	1	0	In 7
0	1	1	1	In 8
1	0	0	0	In 9
1	0	0	1	In 10
1	0	1	0	In 11
1	0	1	1	In 12
1	1	0	0	In 13
1	1	0	1	In 14
1	1	1	0	In 15
1	1	1	1	In 16

Table 4.1: Multiplexer functionality

the select bits are incremented in order, as given by Table 4.1, where each possible sequence of select bits represents one fault signal input to the multiplexer. In the hardware, there are only twelve signals, so when select bits represent the unused fault multiplexer inputs, no data is saved or recognized. The resulting fault signals are then recognized in the main Verilog module, which recognizes them as active low signals.

The three fault registers in this system include one for the 12 temperature sensors, one for the 7 voltage and current sensors, and one for the 12 gate driver faults. For the voltage, current, and temperature faults, predefined limits are used. When one of the values goes above the limit, that gets recognized by the system. However, a fault is only ever recorded in the respective fault registers when there are four consecutive high readings, in an effort to ignore false high readings. The gate driver faults are recognized similarly, where the results are only saved in the fault register when there are four consecutive bad signals (faults are active low in this case). In this system, the only faults that can disable the whole system on their own include the voltage, current and temperature fault signals. Other than these, there are cases where if both the primary and secondary gate drivers of any module in the system have faults, the whole system will shut down. As in the previous system, each type

of fault is represented by a different color on the CMOD-A7 RGB led.

4.3.2 MATLAB

Due to the increased complexity of this system, the MATLAB code needs to be carefully designed to ensure timing needs of control are met. The MATLAB code is designed to run several things in parallel, including individual module control, sensing interpretation, and saving data. The main portion of the MATLAB code exists in one while-loop which runs until every module in the system has finished testing. Inside this while loop, logic including setting the minimum temperature threshold, reading gate driver faults, and SiC MOSFET state control, are each run six times (one time for each module). Though the ADC sampling frequency is controlled by the FPGA in the Verilog model, each time the while loops is executed, a parallel function named "processControlVals" is called to process the sensed values. This is chosen to operate in parallel due to the potential long duration of calculations, since this function reads all 19 ADC values and scales them individually based on the calibrated values. There also exists a timer function running in parallel at a constant rate of 5 Hz. In this timer function, all the data logging is performed. To keep data easily understood, each SiC MOSFET has its own series of .csv files that data will be saved to. At every occurrence of the timer function, the data interpreted by the "processControlVals" function is saved into individual arrays of data. After five timer executions, each ADC data array is average, and the results are saved to the respective .csv files for later use. This timer also implements counters for each file that will start a new file every time a user specified number of rows of data is saved.

CHAPTER 5

HARDWARE RESULTS

5.1 Revision 1 Results

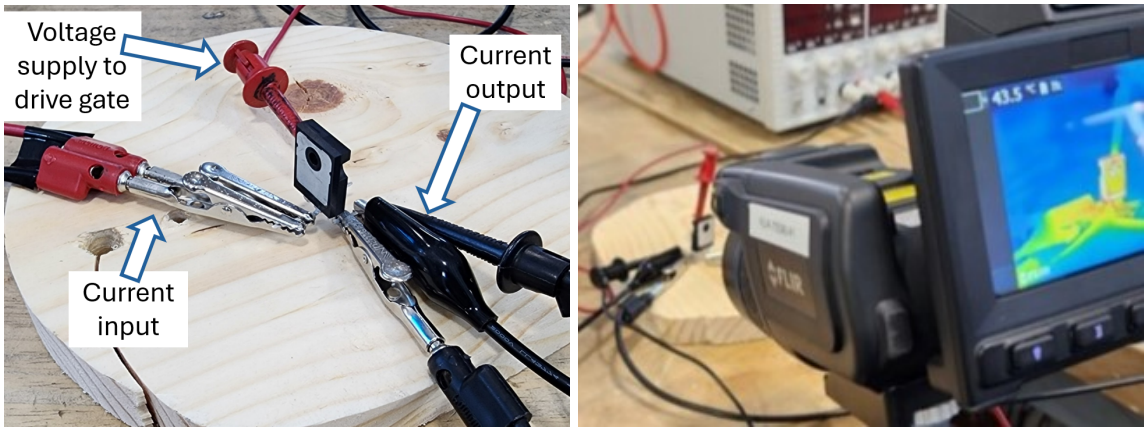
5.1.1 Initial Validation

As part of the initial testing of this system, off board temperature swing testing took place to obtain estimated on cycle time based on different current levels. This test uses a simple setup, shown in Figure 5.1. The setup uses two power supplies: one for the main current supply and one to apply the gate-to-source voltage to turn the device on. In Table 5.1, results are shown for three different current levels. It is clear that due to the high current rating of the device, a high current is necessary in testing to decrease cycle time and increase shock to the device.

Following preliminary testing, initial on-board testing is necessary. The first task for on-board testing was to calibrate the voltage, current, and temperature sensing circuits in conjunction with the ADC model on the FPGA. To calibrate the voltage sensing circuit, a known voltage is applied across the drain-to-source of the DUT, then the resulting ADC value recorded by the FPGA is obtained. This process is repeated over the expected range of voltage. Similarly, this process is applied to the current sensing circuit by turning on the DUT and running known currents through the device over the full range of the current sensor. The raw results from the voltage and current calibration are shown in Figure 5.2.

Current (A)	Temperature (° C)	Time (min)
10	24 – 155° C	8.5
12	24 – 155° C	3
15	24 – 155° C	1.5

Table 5.1: Preliminary temperature swing testing results



(a) (b)

Fig. 5.1: Off-board preliminary temperature swing testing

On the left side of the table, there are two ranges of current sensing calibration. In the current sensing circuit, the use of V_{bias}, V_{OCM}, and the ratio from R_f to R_g are selected to utilize the full positive and negative range of the differential ADC (from V_{ref} to $-V_{ref}$). This is possible because there is a symmetrical, even range for the voltage outputs of the hall effect sensor. However, this is not possible for the voltage sensing circuit since the range for the voltage is not symmetrical and will vary widely over time of testing as R_{DS_on} increases. The voltage sensing circuit still utilizes the full positive range of the differential ADC (0 to V_{ref}).

With the final raw values from ADC calibration, the slopes and offsets are extracted from the data by plotting the values and finding the linear line of best fit. The plots for voltage and current are shown in Figures 5.3 and 5.4 respectively. With these lines of best fit, math is implemented in the MATLAB code to interpret the FPGA output, given in unsigned decimal, and translate it to either a voltage or current value. As evident in Figure 5.4, there are two different lines of best fit, due to the utilization of the full range of the differential ADC. To implement these two lines in code, the unsigned decimal value is checked first to determine which range it fits into, then converted to the real current.

Little calibration was needed for the temperature sensing circuit, since there is a given resolution by the thermocouple ADC. This calibration setup is shown in Figure 5.5, which

Current ADC			Voltage ADC		
Input	Unsigned decimal	Slope	Input	Unsigned decimal	Slope
0.996	11162		0.3352	1304	
1.493	11369	416.499	0.3423	1327	3239.437
1.992	11669	601.2024	0.3597	1382	3160.92
2.985	12258	593.1521	0.3677	1408	3250
3.98	12858	603.0151	0.3789	1442	3035.714
4.975	13450	594.9749	0.3901	1478	3214.286
5.97	14040	592.9648	0.4003	1510	3137.255
6.965	14625	587.9397	0.4178	1566	3200
7.96	15228	606.0302	0.44	1635	3108.108
8.95	15815	592.9293	0.4589	1694	3121.693
	Average slope:	591.4606	0.4802	1758	3004.695
	Offset:	10511	0.4939	1801	3138.686
9.949	39		0.5007	1822	3088.235
10.943	622	586.5191	0.5107	1853	3100
11.937	1210	591.5493	0.5176	1874	3043.478
12.93	1800	594.1591	0.5293	1910	3076.923
13.925	2395	597.9899	0.536	1931	3134.328
14.918	2982	591.138	0.5426	1951	3030.303
15.913	3580	601.005	0.5501	1974	3066.667
16.907	4170	593.5614	0.5579	1996	2820.513
17.9	4760	594.1591	0.5636	2014	3157.895
	Average slope:	594.4397		**Average slope:**	3107.352
	Offset:	-5882		**Offset:**	265.29

Fig. 5.2: Raw values from voltage and current ADC calibration

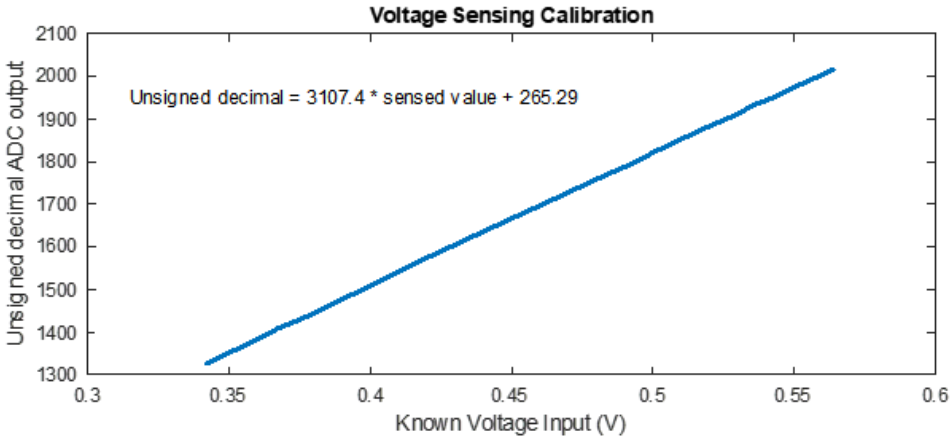


Fig. 5.3: Voltage calibration line of best fit

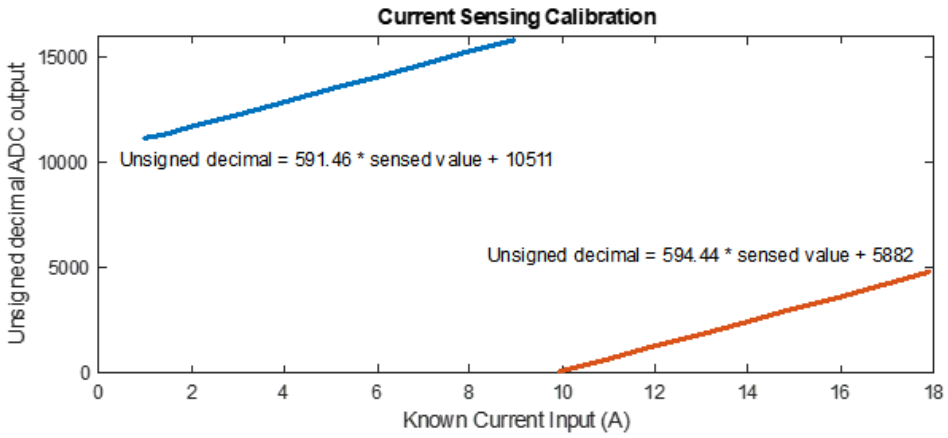


Fig. 5.4: Current calibration lines of best fit

shows an external thermometer with a type-T thermocouple to sense temperature. Also, a thermal camera is used for comparison. The single bit precision for each circuit are as follows: voltage is 0.36 mV, current is 1.65 mA, and temperature is 0.25° C.

To validate the sensing circuits, results of a brand-new device are compared to the device datasheet. The results of this validation process are shown in Figure 5.6, where the blue line is the datasheet extracted data and the red line is real data acquired in system operation. To obtain the data, a constant current is fed through the device to heat it from 25° C to 175° C, while collecting V_{ds} and I_D. As seen in the plot, the data matches nicely to the datasheet values. Though there are small discrepancies, these can be attributed to potential differences in manufacturing and small errors at low voltages in the sensing circuit.

One of the final steps before running power cycling tests is to analyze the on-board temperature swing under different current levels. This testing was extensive but is summarized in Figure 5.7. Current levels ranging from 12 A to 16 A were found to be insufficient for the desired temperature range capabilities. Testing at 18 A brought positive results, but there were still a few issues seen with both heating and cooling times and capabilities. Due to the secondary fan state being on during the full temperature swing, the airflow escaping from the desired path caused the heating time of the DUT to increase. The lack of directed airflow also slowed down the cooling portion of the cycle. To fix these issues, 3D printed airways, shown in Figure 5.8, were designed and attached to the fans. The results

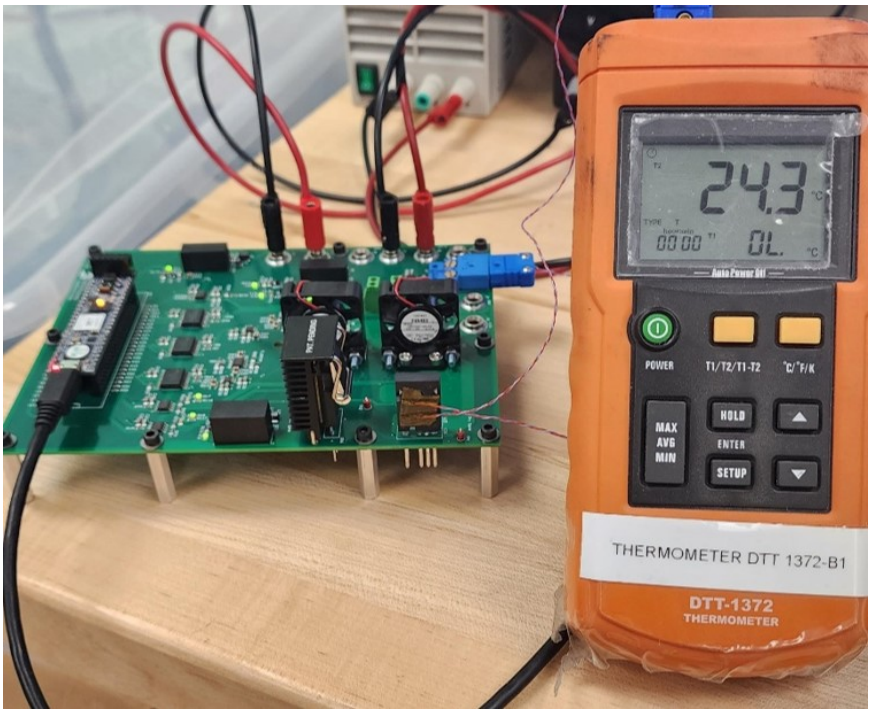


Fig. 5.5: Temperature calibration test setup

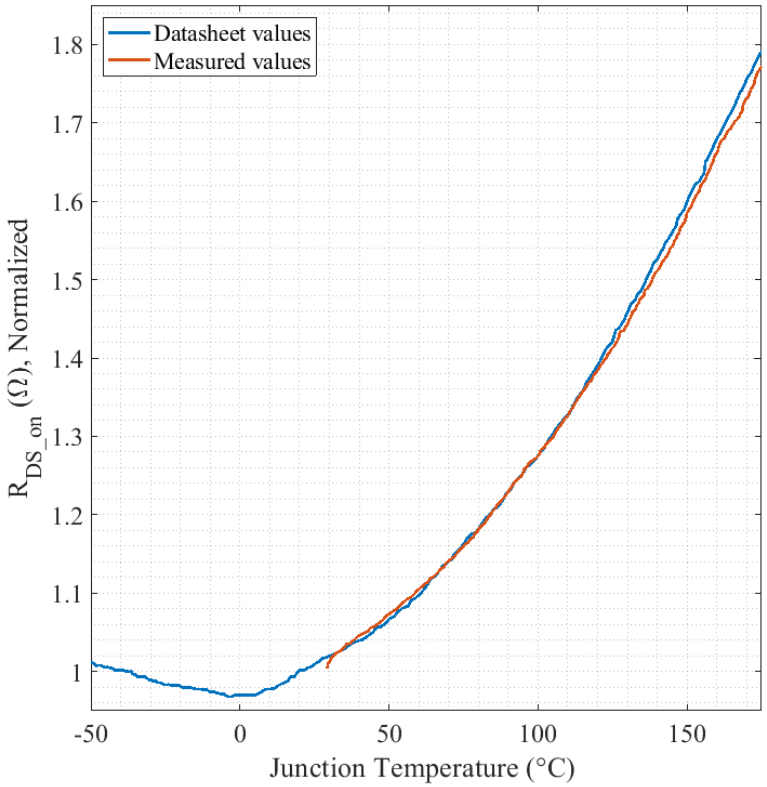


Fig. 5.6: Voltage, current, and temperature datasheet comparison

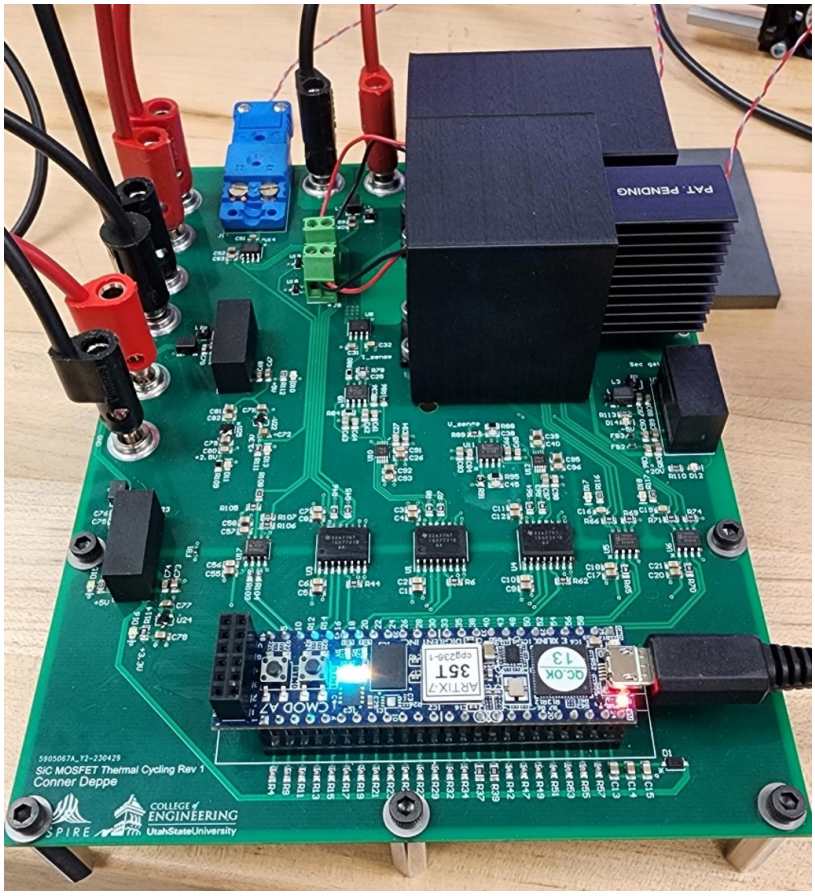
Hardware state	Temperature range (° C)	Time (mm:ss)	Notes
Initial (12 A)	40 to 80	5:00	Need higher current
Initial (14 A)	50 to 90	7:30	Need higher current
Initial (15 A)	45 to 150	10:30	Need higher current
Initial (16 A)	30 to 130	8:45	Need higher current
Initial (18 A)	30 to 185	4:45	Heating is too slow Can't cool enough
	185 to 50	5:30	
	30 to 185	4:52	
	185 to 60	3:00	
Added airways (18 A)	30 to 185	4:14	Can't cool enough
	185 to 50	5:45	
	50 to 185	3:30	
	185 to 60	3:01	
New return path (18 A)	80 to 220	3:26	Heating and cooling times are sufficient
	220 to 80	1:53	
	80 to 220	3:21	
	220 to 35	4:36	

Heating	
Cooling	

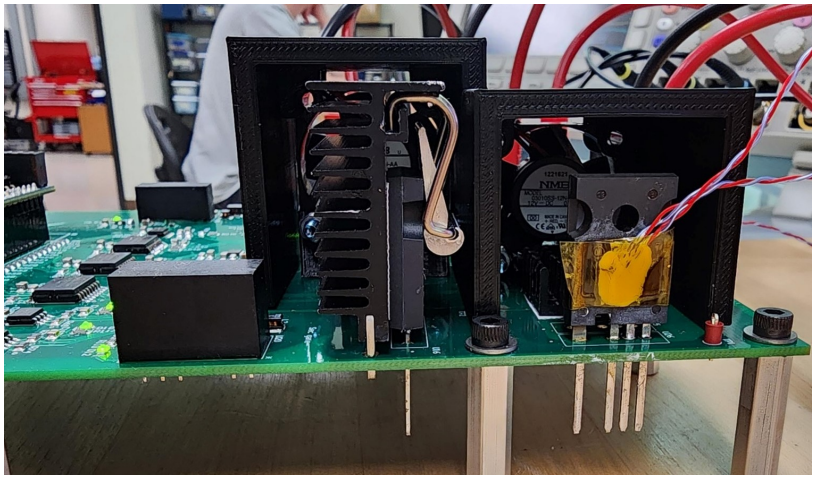
Fig. 5.7: On-board temperature swing testing with hardware changes

of this hardware addition shows decreased heating and cooling times. However, the system was still only capable of bringing the temperature of the DUT down to 50° C. After this realization, more investigation found a design flaw in the secondary current return path on the PCB. This path needed to be able to carry current up to the rated value of the current sensor, but it was too small. The results showed extreme temperatures around that part of the PCB, which was right next to the DUT. This was determined to be the reason for incapable cooling, so a bypass wire was soldered to the bottom of the PCB, as shown in Figure 5.9, to prevent the PCB from overheating. With the addition of this bypass wire, the system was now able to heat and cool the DUT sufficiently.

Before running continuous power cycling testing on the board, external protection was implemented in the form of in-line fuses for the input current lines. To test the inline fuses, a constant current was run through the wires, which resulted in large enough temperatures causing the fuse to blow. This setup is shown in Figure 5.10, where Figure 5.10a is a real image and Figure 5.10b is a snapshot from an infrared camera showing extreme temperature. Though the current supplied was under the limit of the wires, fuse holder, and fuse, this initial product was not viable. After replacing this inline fuse setup with a higher rated



(a)



(b)

Fig. 5.8: Fan airways

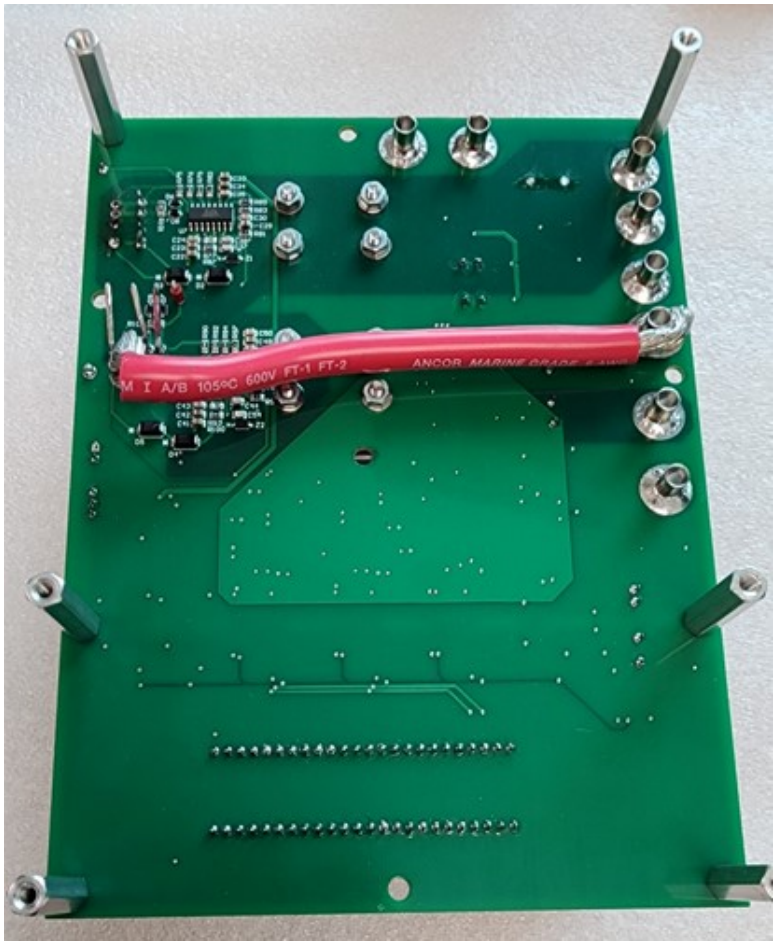
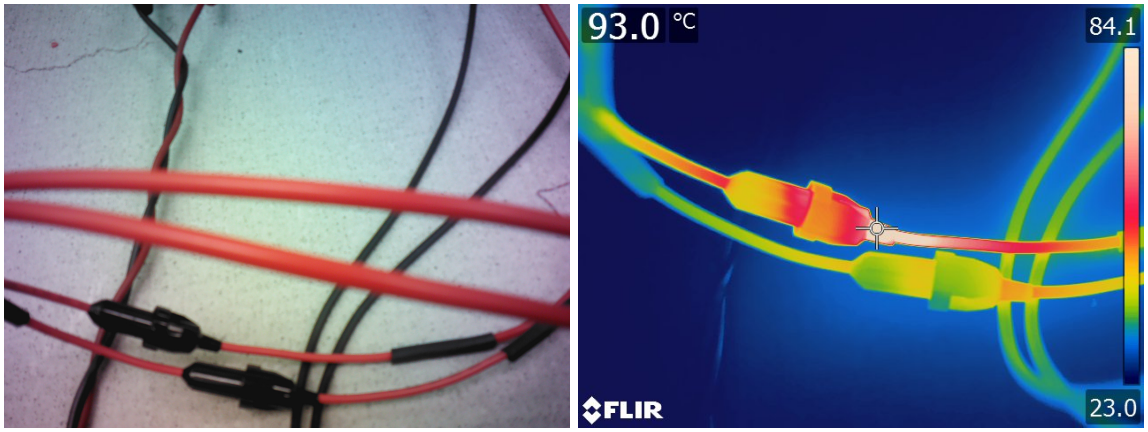


Fig. 5.9: Bypass wire for secondary SiC MOSFET return path



(a) (b)

Fig. 5.10: Inline fuses overheating

wire, preliminary testing is now complete, and autonomous dc power cycling testing can be run.

5.1.2 Power Cycling Results

To run the power cycling using the PCB designed in Chapter 3, the hardware test setup shown in Figure 5.11 is used. This setup includes the thermal cycling platform, which is connected to three power supplies: one for auxiliary power, another for main current, and a third for fan power. Additionally, it features a USB connection to the PC for user interfacing. A summary of the power cycling test results is shown in Table 5.2, where testing is split into three phases with different test parameters. The test results include 7 successful devices tested, 27,598 total cycles, and 2045 total hours. The first phase of testing represents the piloting phase of the PCB, the second phase introduced an increased sampling rate, and the third phase introduced a new temperature range for thermal cycles.

Phase One

Phase one of testing was used to perform validation of system parameters. The data collection occurred at a sampling rate of 0.2 Hz, and the thermal cycling values are given as $T_{j\_min} = 80^\circ\ C$, $\Delta T_j = 165^\circ\ C$, $T_{j\_max} = 245^\circ\ C$. During this testing, permission was not

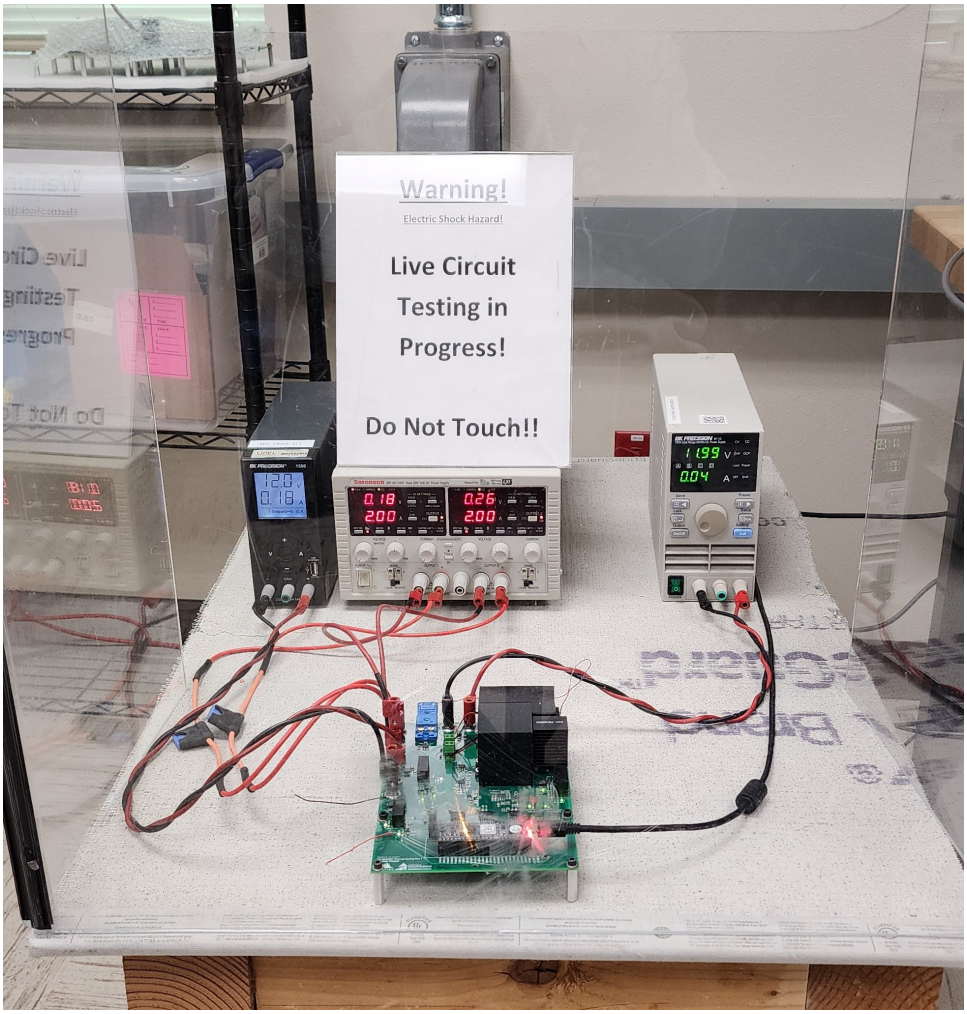


Fig. 5.11: Hardware test setup

Phase	Device	Cycles	Hours	Sampling rate	Temperature
1	1	630	52	0.2 S/s	$T_{j\_min} = 80° \ C$
2	2	1562	131	1 S/s	$\Delta T_j = 165° \ C$
	3	1841	159		$T_{j\_max} = 245° \ C$
3	8	8940	683		$T_{j\_min} = 80° \ C$
	9	1537	127		$\Delta T_j = 147° \ C$
	10	2430	197		$T_{j\_max} = 227° \ C$
	11	10658	696		

Table 5.2: Successful test results

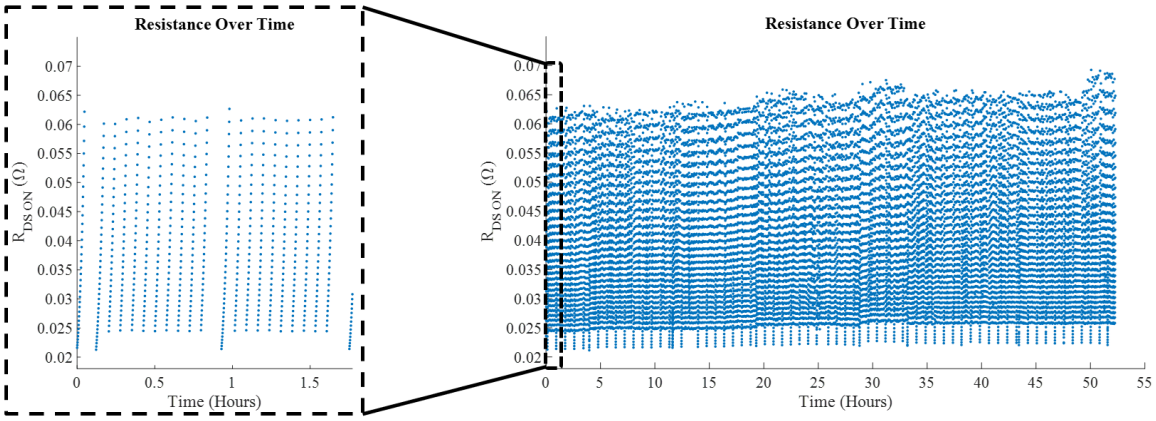


Fig. 5.12: R_{DS_on} data results for device 1 with expanded portion

given yet to run the testing overnight, so testing was only run during work hours. The only device of phase one testing lasted 52 hours, which was 630 cycles. The whole test results for R_{DS_on} are shown in Figure 5.12 on the right. On the left side, a zoomed in portion of the R_{DS_on} of the first 20 cycles is shown. It is clear to see the increase in R_{DS_on} over the whole change in temperature. To better analyze the R_{DS_on} data, Figures 5.13 and 5.14 are used. In these figures, R_{DS_on} data is extracted at various temperatures along the full range. Figure 5.13 shows the real R_{DS_on} values for each temperature range. In this plot, lines of best fit are calculated and displayed for each different range. The trends across all ranges of temperature are linear. The scaled resistance plot shown in Figure 5.14 is made using the same data as in Figure 5.13, but each temperature range is scaled to the initial sensed value. This plot shows that over the temperature ranges, the increase in resistance is fairly consistent.

The results from this testing allow for several conclusions and therefore changes to the testing profile and code. First, after observing the data, the are several significant gaps which can be up to 10 hours long. From this, it was determined to increase the sampling rate for the next phase of testing. Second, the discontinuous testing caused some jumps in the sensed values, which is undesired. To overcome this, the next phase of testing did not start until the final approval for overnight testing came through. Lastly, there is a somewhat frequent occurrence of sensing noise mostly in the current sensing results. To fix

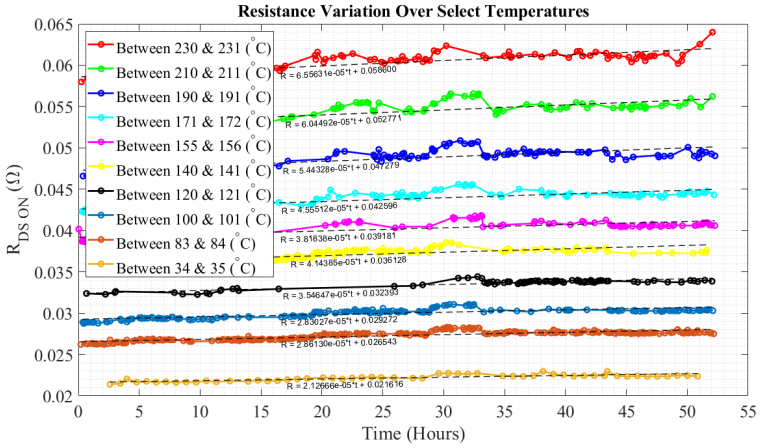


Fig. 5.13: R_{DS_on} over selected temperature ranges for device 1

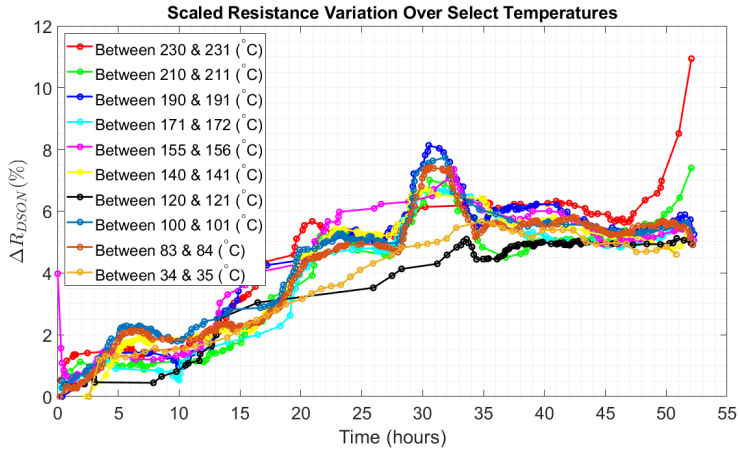


Fig. 5.14: Normalized R_{DS_on} over selected temperature ranges for device 1

this issue, sampling rate was increased by 5 times, but the MATLAB code now takes the average of every 5 sensed values.

Phase Two

In phase two, the only part of the testing profile that changed is the sampling time, which is now 1 Hz. This frequency is the frequency at which the data sample is saved, but the MATLAB script implements a sampling rate of 5 Hz then averages and saves every 5 values. Two more SiC MOSFETs were tested under these new conditions, and results were very similar to the first phase of results. The actual R_{DS_on} sensing results are shown in Figures 5.15 and 5.16, which show significant increases in R_{DS_on} over time. Device 2 lasted through 131 hours of testing, which was 1562 cycles. Device 3 lasted through 159 hours of testing, which was 1841 cycles. Both of these devices successfully underwent continuous testing to failure with minimal pauses.

The plots for R_{DS_on} over time divided into select temperature ranges are shown in Figures 5.17 and 5.18. These results show a much higher resolution over time as compared to phase one. For both of these devices, a linear variation of R_{DS_on} is seen just as in phase one of testing. However, as seen in Figures 5.19 and 5.20, the results for scaled resistance variation are slightly different than those seen in phase one. These results show a less uniform increase in R_{DS_on} over the temperature ranges.

Following the conclusion of testing on device 3, it was seen that this first thermal cycling PCB was too worn out to perform further testing. The extended thermal cycles had caused issues with solder re-flow and PCB footprint detachment. Figure 5.21 shows an image after device 3 testing was finished with a drop of solder at the end of the drain pin of the DUT. Upon removal of device 3, the PCB footprints are shown in Figure 5.22 before and after cleaning them. On this first PCB, tests on devices 1 and 2 were carried out using the footprint called U26, and device 3 testing was carried out on U15.

Due to the broken-down footprints, this board was deemed to no longer be viable, and testing was set to move forward on board 2, which was quickly populated with all new components. Overall, this board brought nothing but issues from the start. This

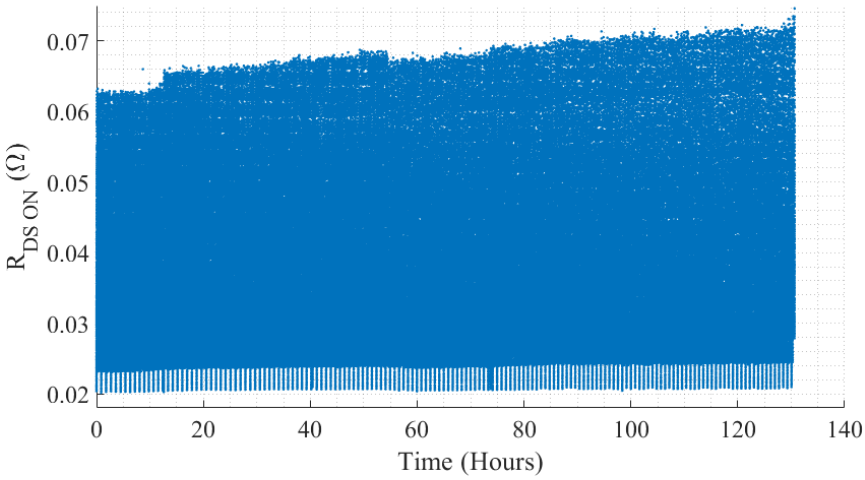


Fig. 5.15: R_{DS_on} data results for device 2

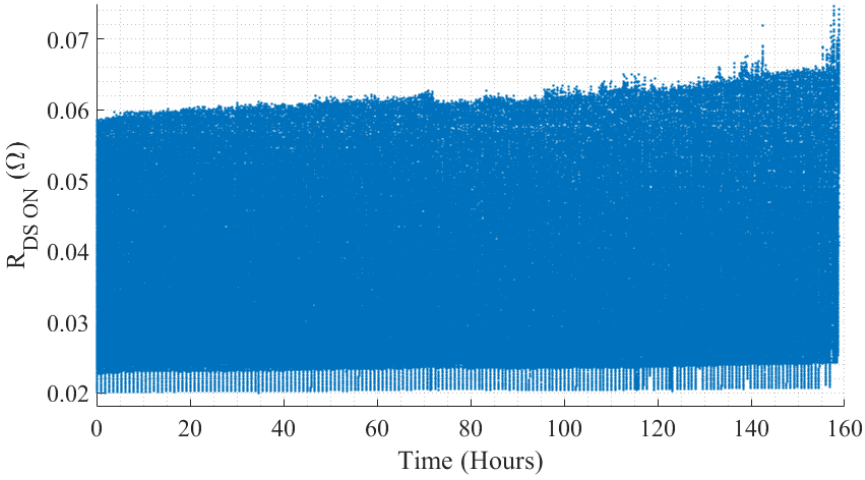


Fig. 5.16: R_{DS_on} data results for device 3

board ran testing on 4 separate devices, each of which were unsuccessful. The testing is summarized in Table 5.3. The first test, on device 4, was running smoothly for about a day and a half when at a point in the middle of the night, MATLAB froze in the middle of a heating portion of the cycle. This resulted in an extreme temperature of the junction of the SiC MOSFET, which caused complete failure of the device. As a result of this testing, the temperature limits implemented in the FPGA code were significantly lowered. Though device 4 lasted 35 hours, or 427 cycles, the results did not show significant change

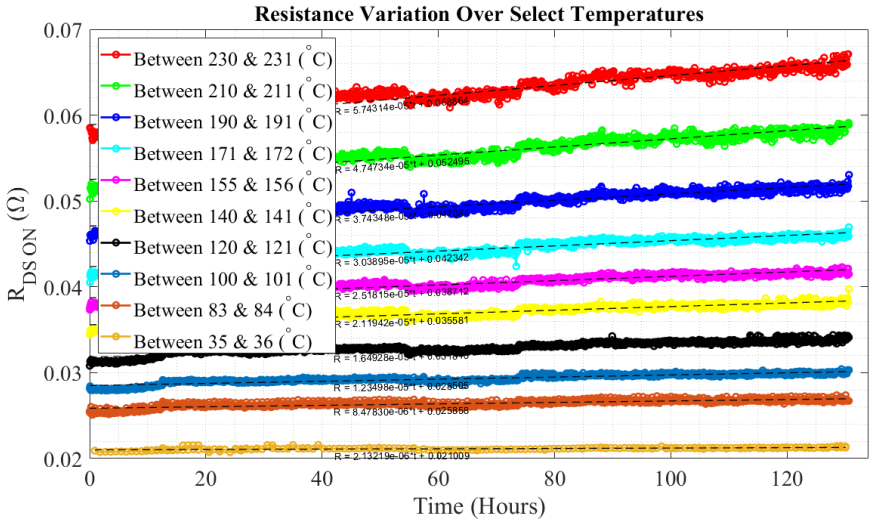


Fig. 5.17: R_{DS_on} over selected temperature ranges for device 2

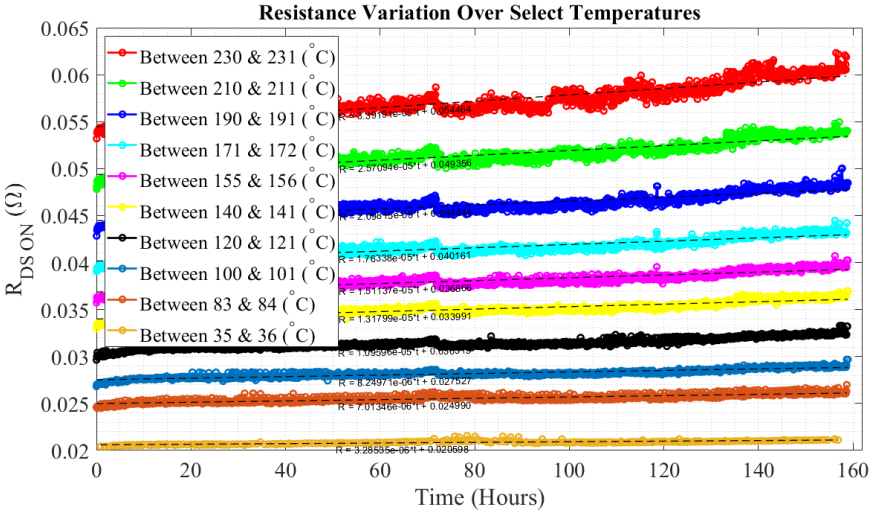


Fig. 5.18: R_{DS_on} over selected temperature ranges for device 3

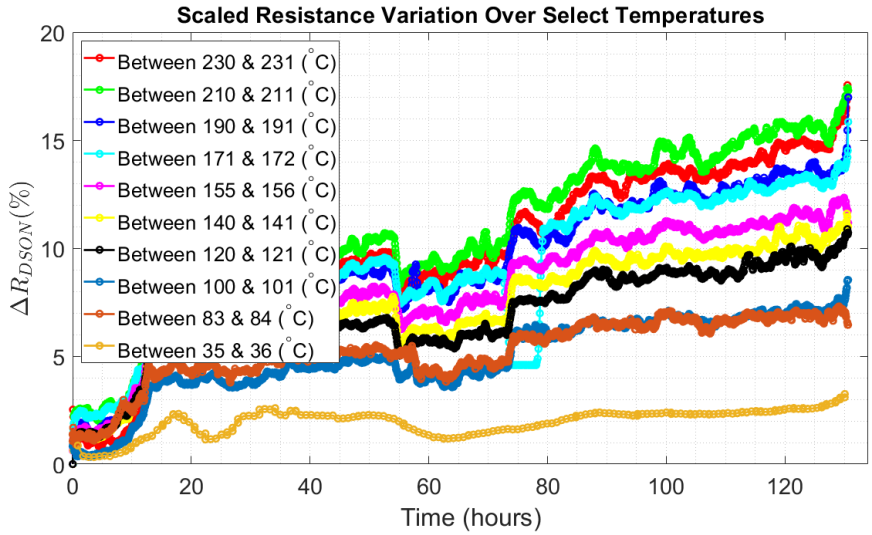


Fig. 5.19: Normalized R_{DS_on} over selected temperature ranges for device 2

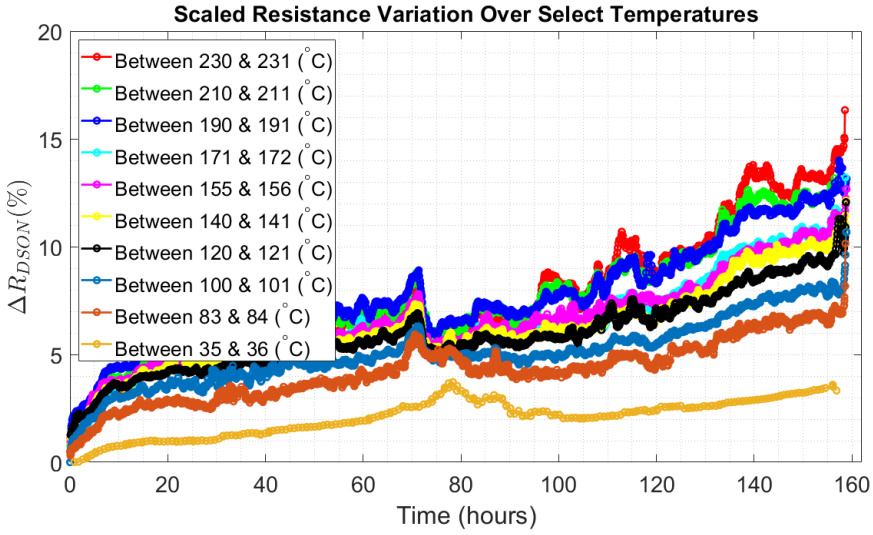


Fig. 5.20: Normalized R_{DS_on} over selected temperature ranges for device 3

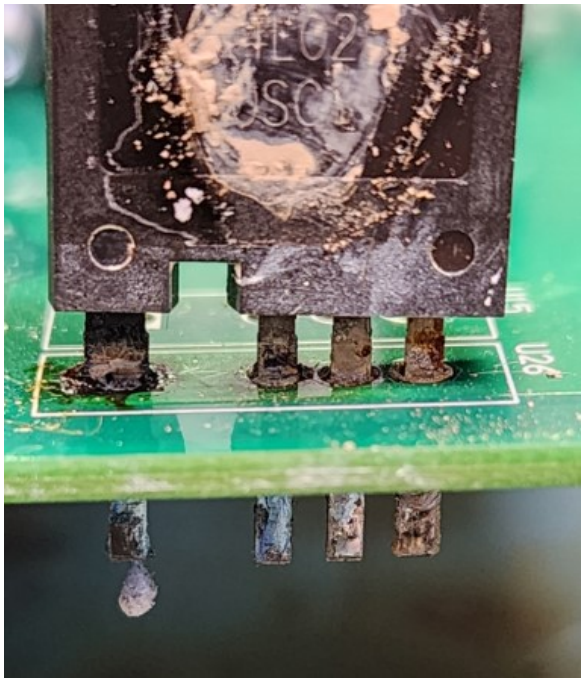
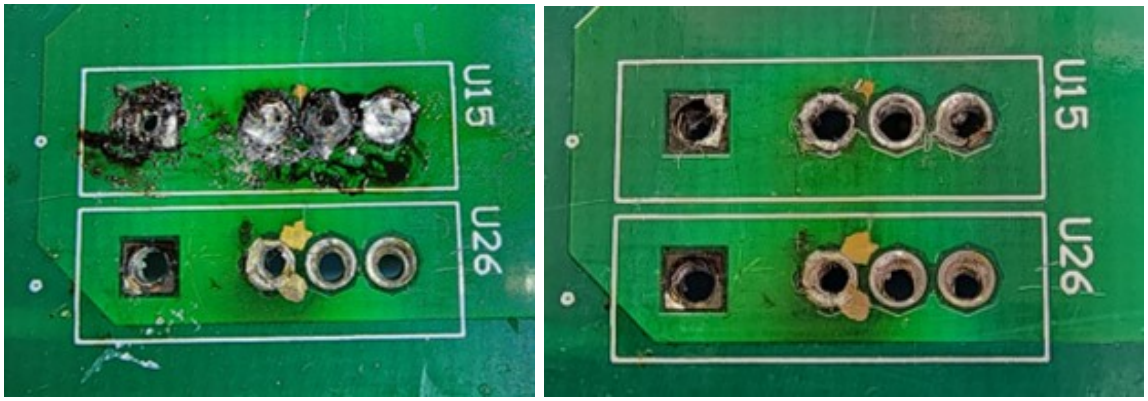


Fig. 5.21: Solder dripping from device 3



(a) Before cleaning (b) After cleaning

Fig. 5.22: Board 1 broken footprints

Device	Cycles	Hours	Cause of failure
4	427	35	MATLAB froze
5	695	59	Gate driver faults
6	470	44	Over voltage faults
7	171	18	Over voltage faults

Table 5.3: Failed test results

in R_{DS_on}, so they are not presented here. Next, testing on device 5 started. This testing was frequently, randomly interrupted due to gate driver faults. After each fault, the whole system would need to reset, causing major delays in testing. Device 5 lasted 59 hours, or 695 cycles of intermittent testing. Again, this device did not see significant variation in R_{DS_on}, so results are not presented. After device 5 testing, the entire gate driving circuit was replaced, and testing on device 6 began. Testing was frequently, randomly interrupted again, but this time by faults due to over voltage sensing errors. After 44 hours, or 470 cycles of intermittent testing, device 6 failed. As a final attempt to get board 2 working, the entire voltage sensing circuit was replaced and testing on device 7 began. After a short period of time, over voltage faults occurred, and board 2 was put to rest.

Phase Three

In phase 3, a new temperature profile is introduced the system to help avoid the breakdown of the PCB and circuits close to the DUT. The new temperature profile is given as $T_{j\_min} = 80^\circ\ C$, $\Delta T_j = 147^\circ\ C$, $T_{j\_max} = 227^\circ\ C$. In this phase, successful tests were run on 4 different devices, which ran over 20,000 total cycles. Testing in this phase shows much more promising results than the previous phases. The actual resistance results for device 8-11 are shown in Figures 5.23, 5.24, 5.25, and 5.26. In each of these, the change in R_{DS_on} shows a different pattern than phases one and two. The resistance variation over select temperature ranges are shown in Figures 5.27, 5.28, 5.29, and 5.30. In each of these, the MATLAB calculated linear lines of best fit are shown to highlight the fact that the slopes of each plot are no longer linear. To compare these results, the scaled R_{DS_on} plots are given in Figures 5.31, 5.32, 5.33, and 5.34. Over most of these results, the scaled resistances

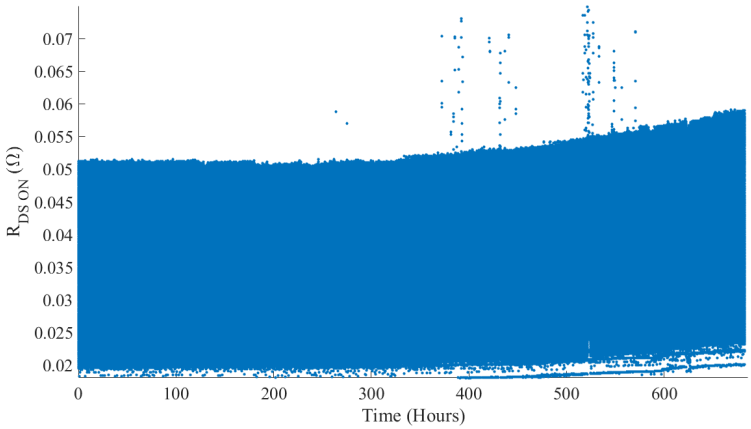


Fig. 5.23: R_{DS_on} data results for device 8

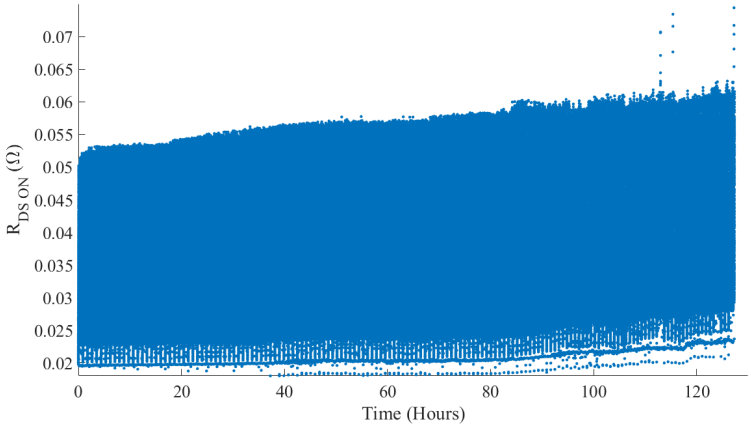


Fig. 5.24: R_{DS_on} data results for device 9

across the temperature ranges are very consistent among each other. These plots also show a much larger percent change in resistance over the duration of testing.

Several conclusions can be drawn from the final phase of testing on revision one. First, the same part number gives different values and changes in R_{DS_on}, but the trends are quite similar among each other. Second, with the common trends in several data sets, a potential end-of-life threshold can be developed based on R_{DS_on} variation. Third, since the trends resemble an exponential increase, there is no need for complex machine learning model development. Finally, in the future, when applying the models developed through the use of this data, R_{DS_on} should be measured at consistent temperatures to get accurate

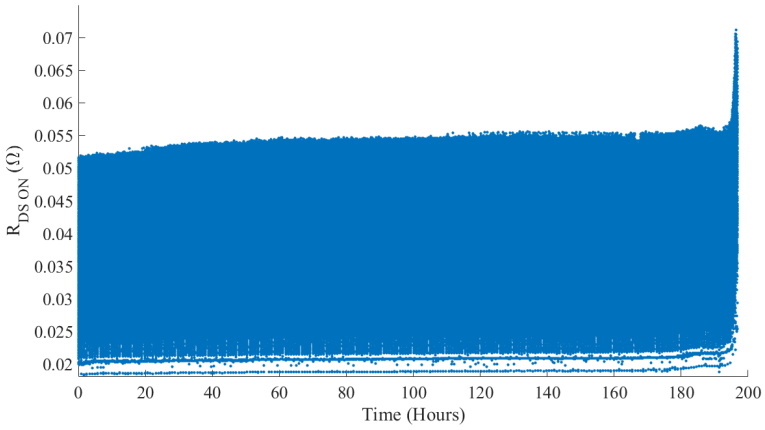


Fig. 5.25: R_{DS_on} data results for device 10

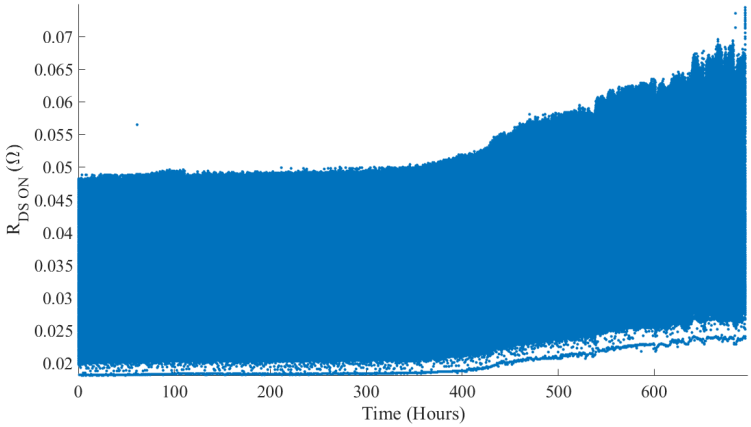


Fig. 5.26: R_{DS_on} data results for device 11

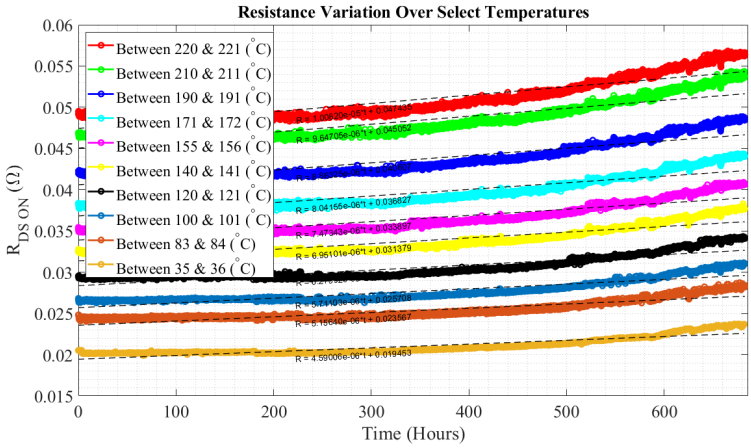


Fig. 5.27: R_{DS_on} over selected temperature ranges for device 8

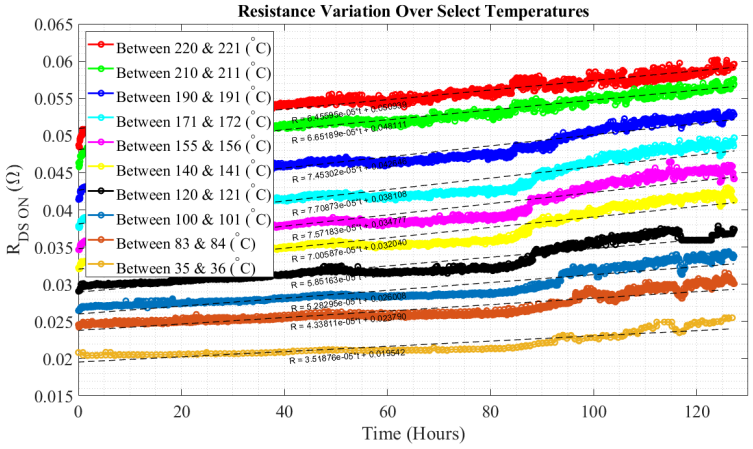


Fig. 5.28: R_{DS_on} over selected temperature ranges for device 9

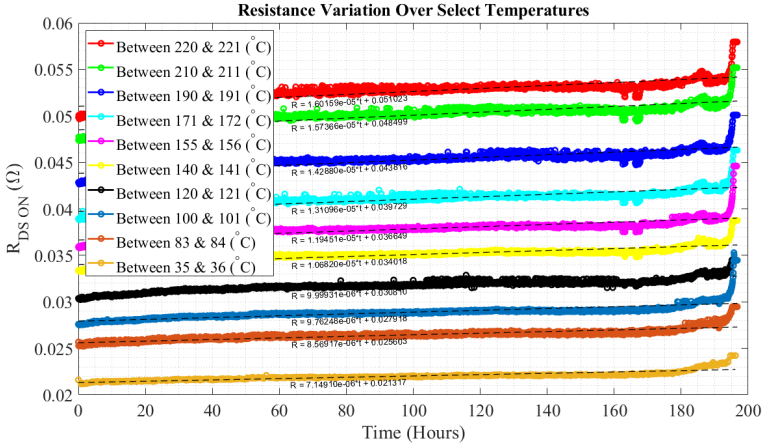


Fig. 5.29: R_{DS_on} over selected temperature ranges for device 10

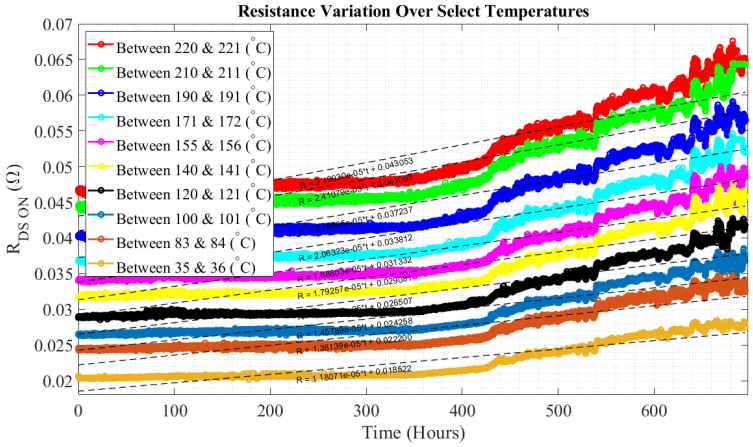


Fig. 5.30: R_{DS_on} over selected temperature ranges for device 11

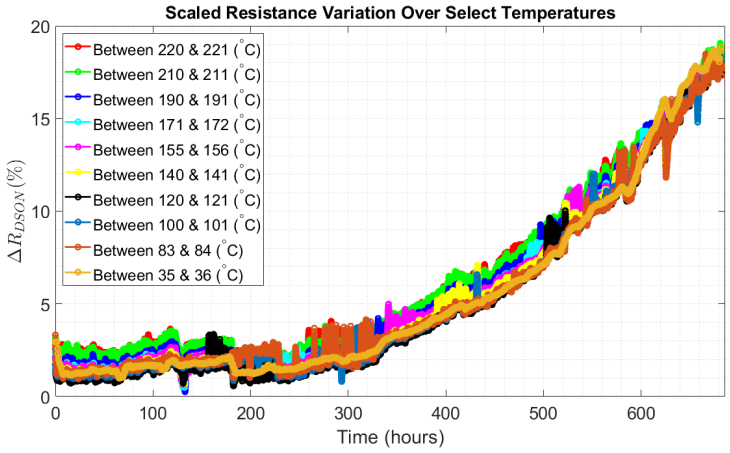


Fig. 5.31: Normalized R_{DS_on} over selected temperature ranges for device 8

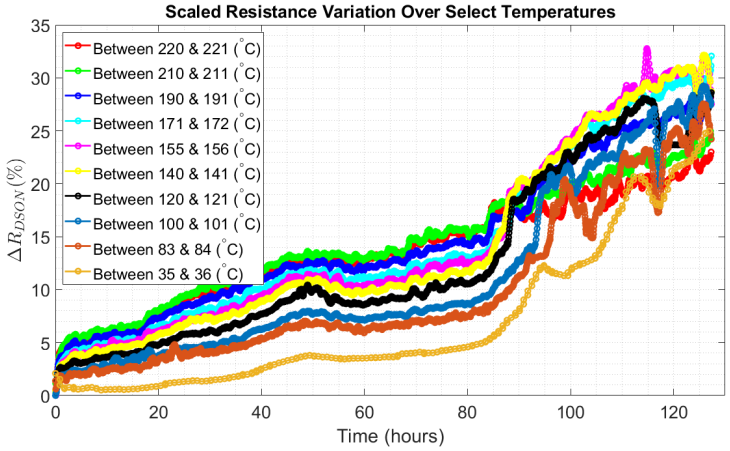


Fig. 5.32: Normalized R_{DS_on} over selected temperature ranges for device 9

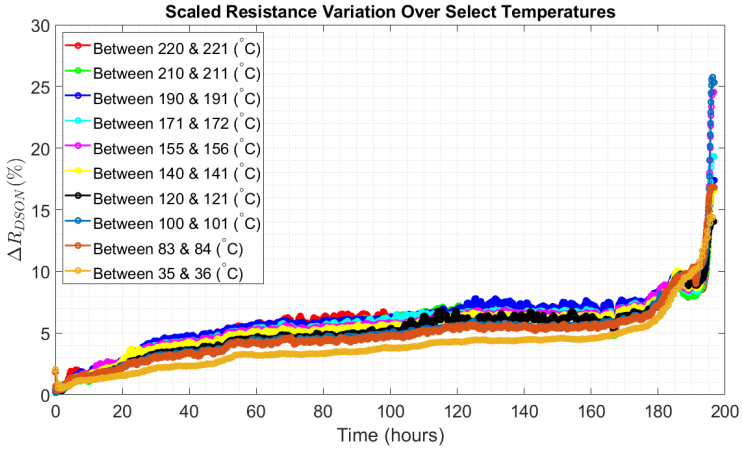


Fig. 5.33: Normalized R_{DS_on} over selected temperature ranges for device 10

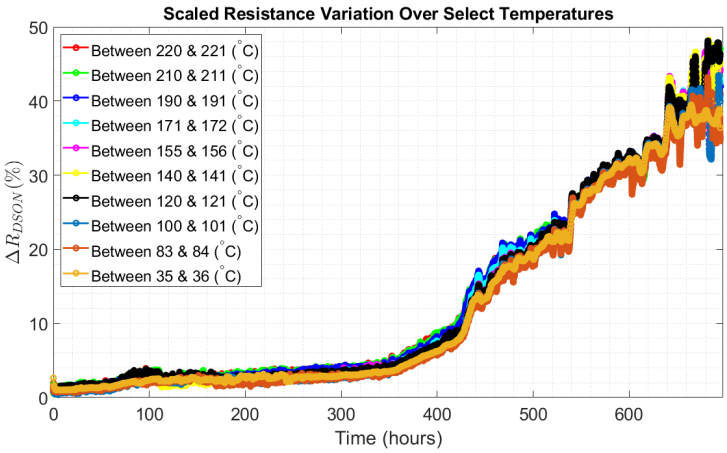


Fig. 5.34: Normalized R_{DS_on} over selected temperature ranges for device 11

estimates for online monitoring.

5.2 Revision 2 Results

At this point in time, revision two is still in the early stages of testing. Over the next few months, this project and testing on revision two will be taken over by another student.

CHAPTER 6
CONCLUSION AND FUTURE WORK

6.1 Conclusion

This thesis outlines the design and implementation of a dc power cycling test to help understand the aging process for SiC MOSFETs. The dc power cycling test was designed to degrade the bond wires of the SiC MOSFET over time, which was represented by a shift in R_{DS_on}. This test was designed to be suitable for discrete SiC MOSFETs that are used in EV charger applications. In this test, it was necessary to sense I_D, V_{DS}, and T_j to control the system and accurately represent R_{DS_on}.

The dc power cycling test was then implemented in hardware which was capable of testing one SiC MOSFET at a time. This hardware was designed to autonomously collect data autonomously from the start of the test to the end-of-life of the device. Everything including control, fault detection, end-of-life detection, and data collection is achieved autonomously through the interfacing of an FPGA connected through USB to MATLAB.

Data collection was successful for a total of 7 devices, which lasted 2045 hours and 27,598 cycles. This data collection not only validated the functionality of the developed hardware, but of the designed dc power cycling test. In the last phase of hardware testing on this revision of the hardware, temperature range and sampling time were fine-tuned to give the best possible data, which can be used in later work.

With the ensured validity of the first revision of hardware, a second revision was then designed to scale up the dc power cycling test. In the new hardware, dc power cycling of 6 different SiC MOSFETs can occur independently in a novel circuit topology, all while using the same bench-top power supplies as in revision one. This new system was designed to be much more robust and directly address the issues seen in heating and cooling times, PCB breakdown, and sensing integrity on revision one hardware.

6.2 Future Work

The future work of this research starts with further implementation of revision two hardware. With this hardware, a significant amount of data can be produced to help with the later modeling of these SiC MOSFETs. The future work of this whole topic of research is outlined in Figure 6.1. As discussed in this thesis, the boxes titled Failure Modes, Accelerated Lifetime Tests, and Failure Indicators are explored. In the future, the data provided on the failure indicators will be used to develop component-level models. After that, system-level models can be obtained through the combination of different component level models.

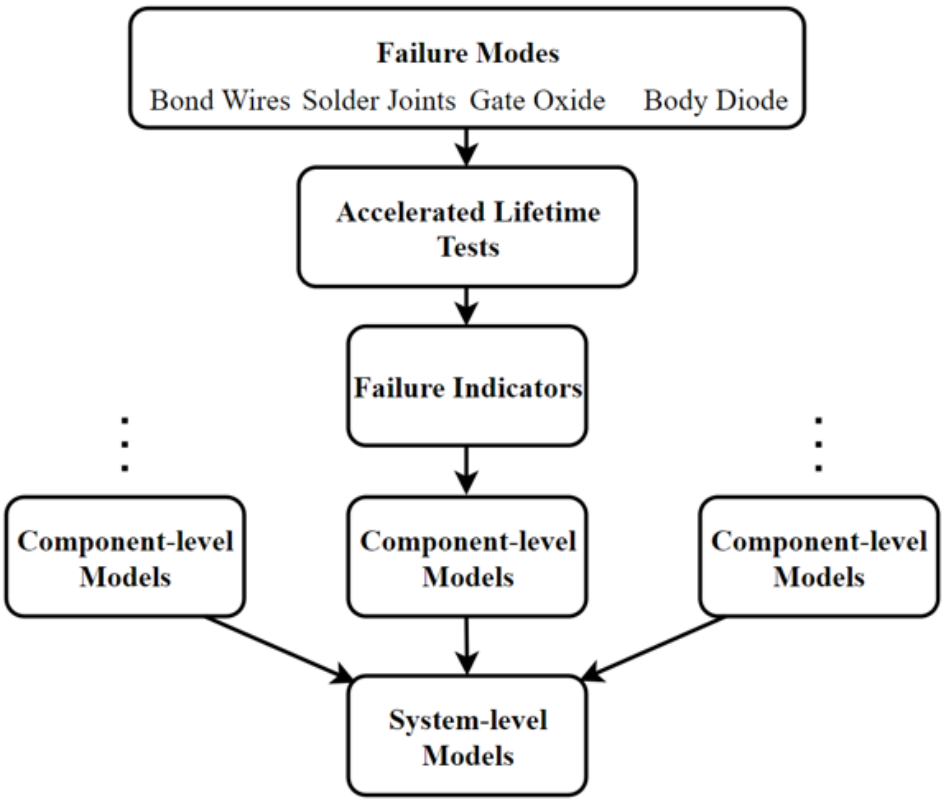


Fig. 6.1: Breakdown of process to achieve system level lifetime estimation models

REFERENCES

[1] "Electric vehicles and hybrids surpass 16% of total 2023 u.s. light-duty vehicle sales - u.s. energy information administration (eia)." [Online]. Available: https://www.eia.gov/todayinenergy/detail.php?id=61344

[2] Z. Ni, X. Lyu, O. P. Yadav, B. N. Singh, S. Zheng, and D. Cao, "Overview of real-time lifetime prediction and extension for sic power converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 8, pp. 7765–7794, 2020.

[3] B. T. Vankayalapati, F. Yang, S. Pu, M. Farhadi, and B. Akin, "A highly scalable, modular test bench architecture for large-scale dc power cycling of sic mosfets: Towards data enabled reliability," *IEEE Power Electronics Magazine*, vol. 8, no. 1, pp. 39–48, 2021.

[4] "Public charging issues may short-circuit ev growth, j.d. power finds." [Online]. Available: https://www.jdpower.com/business/press-releases/2023-us-electric-vehicle-experience-evx-public-charging-study

[5] D. B. Yelaverthi, R. Hatch, M. Mansour, H. Wang, and R. Zane, "3-level asymmetric full-bridge soft-switched pwm converter for 3-phase unfolding based battery charger topology," in *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2019, pp. 2737–2743.

[6] A. Zade, C. R. Teeneti, M. Mansour, S. Gurudiwan, B. Hesterman, H. Wang, and R. Zane, "A 21-kw unfolding-based single-stage ac–dc converter for wireless charging applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 12, no. 1, pp. 8–27, 2024.

[7] S. Inoue, C. R. Teeneti, D. Goodrich, J. Larsen, A. Kamineni, and R. Zane, "High-power field-focusing circuit for dynamic wireless power transfer systems," in *2022 Wireless Power Week (WPW)*, 2022, pp. 699–704.

[8] J. Zhu, H. Kim, H. Chen, R. Erickson, and D. Maksimović, "High efficiency sic traction inverter for electric vehicle applications," in *2018 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2018, pp. 1428–1433.

[9] Z. Tang, Y. Yang, and F. Blaabjerg, "Power electronics: The enabling technology for renewable energy integration," *CSEE Journal of Power and Energy Systems*, vol. 8, no. 1, pp. 39–52, 2022.

[10] S. Dusmez, H. Duran, and B. Akin, "Remaining useful lifetime estimation for thermally stressed power mosfets based on on-state resistance variation," *IEEE Transactions on Industry Applications*, vol. 52, no. 3, pp. 2554–2563, 2016.

[11] J. R. Celaya, A. Saxena, C. S. Kulkarni, S. Saha, and K. Goebel, "Prognostics approach for power mosfet under thermal-stress aging," in *2012 Proceedings Annual Reliability and Maintainability Symposium*, 2012, pp. 1–6.

[12] E. Ugur and B. Akin, "Aging assessment of discrete sic mosfets under high temperature cycling tests," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2017, pp. 3496–3501.

[13] M. Farhadi, B. T. Vankayalapati, and B. Akin, "Reliability evaluation of sic mosfets under realistic power cycling tests," *IEEE Power Electronics Magazine*, vol. 10, no. 2, pp. 49–56, 2023.

[14] G.-J. Su, "Comparison of si, sic, and gan based isolation converters for onboard charger applications," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, 2018, pp. 1233–1239.

[15] S. Li, S. Lu, and C. C. Mi, "Revolution of electric vehicle charging technologies accelerated by wide bandgap devices," *Proceedings of the IEEE*, vol. 109, no. 6, pp. 985–1003, 2021.

[16] C. Tang, Q. Xu, R. Han, P. Guo, R. Liu, and Z. Qing, "Comparison and evaluation of the thermal performance between sic-mosfet and si-igbt," in *2022 IEEE Transportation Electrification Conference and Expo, Asia-Pacific (ITEC Asia-Pacific)*, 2022, pp. 1–5.

[17] M. V. Kjær, H. Wang, and F. Blaabjerg, "End-of-life detection of power electronic converters by exploiting an application-level health precursor," *IEEE Open Journal of Power Electronics*, vol. 3, pp. 549–559, 2022.

[18] L. Saidi, A. Ismail, M. Sayadi, and M. Benbouzid, "Phm of power electronic converters in renewable energy systems: A short review with some applications," in *2022 IEEE International Conference on Electrical Sciences and Technologies in Maghreb (CISTEM)*, vol. 4, 2022, pp. 1–6.

[19] K. Sivalingam, M. Sepulveda, M. Spring, and P. Davies, "A review and methodology development for remaining useful life prediction of offshore fixed and floating wind turbine power converter with digital twin technology perspective," in *2018 2nd International Conference on Green Energy and Applications (ICGEA)*, 2018, pp. 197–204.

[20] Y. Shen, Z. He, Y. Shi, H. Niu, Y. Chen, C. Liu, Y. Chen, Z. Cai, G. Lu, and X. Dai, "Time-dependent degradation mechanism of 1.2 kv sic mosfet under long-term high-temperature gate bias stress," *IEEE Transactions on Electron Devices*, vol. 70, no. 3, pp. 1162–1167, 2023.

[21] S. A. Ikpe, J.-M. Lauenstein, G. A. Carr, D. Hunter, L. L. Ludwig, W. Wood, L. Y. Del Castillo, M. M. Mojarradi, F. Fitzpatrick, and Y. Chen, "Silicon-carbide power mosfet performance in high efficiency boost power processing unit for extreme environments," *in Proceeding for Internation Conference on High Temperature Electronics*, pp. 184–189, 2016.

[22] H. Miyazaki, M. C. Ngo, K. Hirao, and M. Fukushima, "Effect of thermal cycle temperature gap on thermal fatigue of metallized silicon nitride substrates for sic power modules," in *2023 International Conference on Electronics Packaging (ICEP)*, 2023, pp. 95–96.

[23] P. Ghimire, S. Beczkowski, S. Munk-Nielsen, B. Rannestad, and P. B. Thøgersen, "A review on real time physical measurement techniques and their attempt to predict wear-out status of igbt," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1–10.

[24] S. Dusmez and B. Akin, "An accelerated thermal aging platform to monitor fault precursor on-state resistance," in *2015 IEEE International Electric Machines Drives Conference (IEMDC)*, 2015, pp. 1352–1358.

[25] G. Sonnenfeld, K. Goebel, and J. R. Celaya, "An agile accelerated aging, characterization and scenario simulation system for gate controlled power transistors," in *2008 IEEE AUTOTESTCON*, 2008, pp. 208–215.

[26] J. R. Celaya, A. Saxena, S. Saha, and K. F. Goebel, "Prognostics of power mosfets under thermal stress accelerated aging using data-driven and model-based methodologies," *in the Proceedings of the Annual Conference of the Prognostics and Health Management Society*, 2011.

[27] N. Baker, S. Munk-Nielsen, and S. Beczkowski, "Test setup for long term reliability investigation of silicon carbide mosfets," in *2013 15th European Conference on Power Electronics and Applications (EPE)*, 2013, pp. 1–9.