Solar Array Arcing Mitigation for LEO Spacecraft

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What’s the worst that could happen?

- ESD in orbit is not well understood by many in the smallsat community
- Key differences between LEO and GEO mechanisms
- LEO arcing prevention can be catastrophic, and demands different design approaches

Figure 1: Sustained Arc Damage from the ESA EURECA Mission
Background

- PV-battery systems prevalent in smallsats
- 28VDC bus designs common
  - Desire to leverage standards and practices from aircraft industry
- Consequence: high-voltage (>50V) systems uncommon
  - Until recently...
- Increasing demands on EPS drive systems towards higher voltages
  - Decreased Ohmic losses, higher voltage payloads
- But with high-voltage comes the risk of arcing...
Background (cont’d)

• Unfortunately, high voltages in LEO (200-1000km) introduce arcing risks

• Arcing risk in LEO is directly related to power system voltage

• Arcing, power drain, destruction of spacecraft coatings can be detrimental or catastrophic!

• Many aren’t aware of the risks…
The LEO Environment

• When energized conductors are exposed to plasma, positive surfaces collect electrons and negative surfaces collect ions

• When spacecraft interact with a plasma environment, several things can happen:
  – Floating potential shifts
  – Parasitic power drain
  – Sputtering
  – Arcing
GEO Arcing

- ESD first identified as an issue for GEO spacecraft

- GEO characterized by electron interactions at >1keV
  - During quiet conditions, electron current < photoelectron current
  - During storm conditions, electron currents > photoelectron current

- If electron current is high and spacecraft surfaces are insulated, differential charging occurs, and arcing can result
  - Insulators such as solar array coverglass can accumulated >1kV potential!
LEO Arcing

- ESD in LEO is completely different!
  - Not a well-understood mechanism until (relatively) recently
  - ESD in LEO directly related to system voltage

- Plasma environment relatively low-energy, but dense

- Surfaces exposed to plasma will charge to whatever potential is needed for net current flow to be zero

- A current loop can form that uses part of the ionosphere as a conducting medium
LEO Arcing (cont’d)

- Electrons are highly mobile, and are easily collected by positively-charged surfaces
- Ions are not mobile, and are not easily collected by negatively charged surfaces
- Consequently, high potentials can develop quickly on spacecraft with high operating voltages
  - Solar arrays with exposed interconnects, cell edges, or power traces will collect negative charge and are subject to arcing
Illustration

• For LEO spacecraft with negatively-grounded power systems, the entire vehicle can float negative with respect to ionosphere

• A spacecraft with a +100V array can see its structure float almost -100V with respect to ionosphere
  – Practically, 90% of the array voltage magnitude

• An illustration:
Illustration – Neutral Environment

~ +50V

100V Battery

~ -50V
Positive surface collects mobile charge carriers

~ 10V

100V Battery

~ -90V

Negative surface cannot collect immobile charge carriers
Solar Array Arcing

- Array arcing results from strong local electric fields
  - Common sites are exposed interconnects

- Serious issues at “triple points”
  - Insulator, conductor, plasma meet to complete a circuit
  - Triple-point arcs can occur as low as 75V

- Trigger arcs
  - Brief discharge

- Sustained arcs
  - Continuous, catastrophic discharge

- This is not a fully-understood phenomenon!
Structural Arcing

- **Two forms:** triple-point and dielectric breakdown

- **Dielectric breakdown** is direct discharge through a dielectric when electric field exceeds dielectric strength
  - An insulating surface will equilibrate to plasma potential
  - If that surface covers a conductor at different potential, dielectric breakdown can occur
  - A risk for thermal coatings, anodized aluminum, etc.

- **Dielectric breakdown** observed for structural voltages as low as 55V!
Mitigation Strategies

• Past designers have applied GEO techniques to LEO spacecraft... this doesn’t work!

• Common mitigation strategies include:
  – Avoid total string voltages > 55V
  – Avoid adjacent string voltages > 40V
  – For string voltages > 75V, trigger arcs can be completely prevented by encapsulation
  – For string voltages > 75V, sustained arcs can be prevented with RTV grouting between adjacent cells
  – Reduce string currents < 0.5A
  – Avoid the problem.
Case Study: M3MSat

- Solar array arcing was an early risk identified for M3MSat
  - Maritime Monitoring and Messaging Microsatellite
  - Mission: AIS detection from space
  - CSA, DRDC, Com Dev (prime), SFL

- Power system topology uses series-PPT
  - High-voltage array stepped down to +28VDC bus
The M3MSat Approach

• Initial solar array designed to maximize number of cells on each panel
  – Variable string lengths
  – Maximum peak voltages $\sim +100V$

• Recognized at early stages that arcing would be a risk in baseline design

• Difficult problem!
  – At microsat scale, where budget and schedule are aggressive, it is difficult to validate/test a mitigation approach!
  – We must rely on best practice alone to address this risk!
Mitigation Options

• Place the structure at most positive potential (positive grounding)
  – Known to reduce risk without changing array design
  – Change to power electronics front-end (PPT)

• Force structure to ground (plasma contacting)
  – Way beyond scope for this sort of mission!
  – Good enough for ISS...

• Prevent plasma exposure to high-voltage surfaces
  – Array encapsulation
The Solution

*Clever people solve problems...*

*...wise people avoid them.*
The Solution

- Array layout redesigned to limit maximum string length (19 cells)
  - Power budget and thermal considerations
  - Optimal string length for maximum power within arcing risk bounds

- Maximum system voltage reduced below 75V

- Maximum voltage of 63V open-circuit
  - Maximum structure potential at WCC-BOL of ~56V
  - Insufficient current for sustained arcing at open-circuit

Table 1: Worst-Case Solar Array Characteristics

<table>
<thead>
<tr>
<th>Solar Array Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum String Temperature</td>
<td>-77 C</td>
</tr>
<tr>
<td>Maximum Open-Circuit Voltage, $V_{oc}$</td>
<td>63.1 V</td>
</tr>
<tr>
<td>Maximum Peak Power Voltage, $V_{mpp}$</td>
<td>56.8 V</td>
</tr>
<tr>
<td>Maximum String Current, $I_{sc}$</td>
<td>506 mA</td>
</tr>
<tr>
<td>Maximum Structure Potential</td>
<td>56.7 V</td>
</tr>
</tbody>
</table>
Conclusions

• Underlying mechanisms for ESD in LEO need to be recognized at system level, early!

• This is a counterintuitive issue that will be encountered more often with higher-performance microsats

• From cost and QA standpoint, may be best to avoid the problem!