

THE ADPMS READY FOR FLIGHT

AN ADVANCED DATA & POWER MANAGEMENT SYSTEM FOR SMALL SATELLITES & MISSIONS

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ABSTRACT

In a contract for ESA, Verhaert Space developed a state-of-the-art control unit for small satellites. Built on the experience gained with the PROBA-I satellite that has been in daily use since its launch in 2001. This next generation avionics has been developed and will have its first in-orbit demonstration in 2009 as the satellite control unit for PROBA-II. The objective of this paper is to explain the benefit of this avionics and its architecture towards small satellite integrators.

The ADPMS presented in this paper is designed for rapid adaptation to a diversity of next generation satellites. It provides the fundamental bus-elements and allows the addition of third-party cards thanks to its open 'plug and play' architecture, resulting in a more optimal spacecraft design and a reduced software effort with a consequent reduction in recurrent development costs and a much shorter production cycle.

BACKGROUND

The need for a performant, easily adapted and configured satellite control unit has been identified as crucial to succeed in the system design of small satellites with high autonomy demands. The European Space Agency initiated different programs to demonstrate the concept and feasibility of small satellites with high performances in terms of:

- Autonomy
- On board processing capabilities
- Payload management

There are some limitations that exist in today's Data Handling Systems, Payload Processing Units and Power Conditioning Systems in terms of:

- Power consumption
- Mass and Volume
- Design complexity due to a lack of uniformity
- Proprietary 'closed' architecture (blackbox design)
- Limited computing and data-handling performance
- Modularity
- Scalability

- Testability

A detailed look at the above top-level requirements identifies however some contradictions:

- Low power consumption versus high computing performance
- Low mass and volume versus modularity
- Highly integrated system versus testability

This paper describes how the ADPMS design has provided an answer to all above criteria without penalising one of them.

SMALL SATELLITE REQUIREMENTS

Earth Observation Specific

1 Image = 1 command from ground

Complex maneuvering capability (multiple target imaging, image panning, ...)

Onboard Autonomy Features

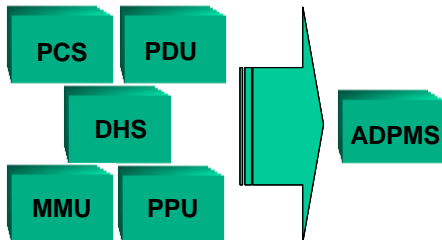
- Autonomy in planning / scheduling
- Autonomy in attitude control system
- Autonomous target prediction and trajectory generation
- High level payload management

- Powerful automated on-board functions
- Ground Segment Automation
- Internet access for payload activity requests
 - Internet access for payload data distribution
 - “Light-out” ground segment

SYSTEM DESIGN

It is clear that, in order to fulfil the top-level requirements listed above, some drastic changes were needed. Therefore the following five essential satellite bus elements have been incorporated into one system:

- S/C Power Conditioning System (PCS)
- S/C Power Distribution Unit (PDU)
- S/C Data Handling System (DHS)
- S/C Mass Memory Unit (MMU)
- S/C Payload Processing Unit (PPU)



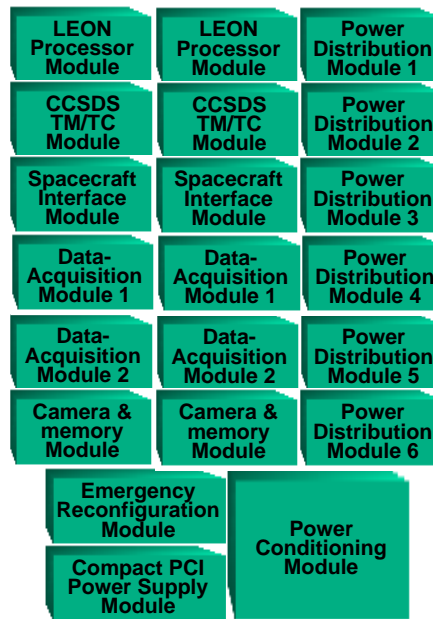
A very effective power, mass and volume reduction could be achieved by the integration of these elements. Resulting at Satellite level in a:

- centralisation of all data handling, storage and processing
- centralisation of all analogue- and temperature sensor acquisition
- elimination of the harness that interconnected the formerly separate units
- reduction of the mechanics because of the integration into one physical enclosure.

ARCHITECTURAL

Overview of the system

The next generation data handling system presented in this paper is partitioned into sub-modules in the form of 3U Compact-PCI boards. The main modules consist of a processor board with memory, a TM/TC board, a spacecraft interface board, one or more data-acquisition boards, a camera board with mass memory and a reconfiguration board. Furthermore the integrated power system consists of a power conditioning module, several power distribution modules and a Compact-PCI power supply module.



All digital functions are implemented using custom logic in form of FPGA's. The computer boards communicate with each other via a high speed PCI backplane while communication to the power boards occurs via direct commanding. The processor that has been selected is the LEON2-FT (AT697 from Atmel). The integrated power system is designed around a Li-ion battery and supplies a battery-regulated bus. The system provides 24 protected output stages to power the payloads and the remaining bus-units located on the spacecraft.

Re-use of industrial standards

The design complexity and testability of the ADPMS have been significantly reduced by the implementation of some well-proven industrial specifications resulting in a higher uniformity of the FPGA and board designs.

For the inter-board connections the Compact PCI standard was selected because of the following key-features:

- It is an open specification (coordinated by PCISIG and PICMG)
- It is currently the most widely accepted and implemented expansion standard in the world, which has resulted in a very properly defined standard reviewed by a large user community.
- The standard includes all aspects needed to achieve a 100% compatibility between plug-in boards of different suppliers. (protocol-, electrical-, mechanical- and configuration-aspects)
- The standard includes a lot of guidelines based on real measurements and extensive simulation to achieve a reliable product-design. (electrical- and pcb-layout-guidelines)

- The mechanical form-factor is suited for rugged environments.
- The electrical definition is suited for applications requiring low power consumption because it's based on a reflected wave-switching topology instead of fixed bus terminations.
- The standard allows the usage of commercial off-the-shelf test-equipment.
- The standard is designed for high throughput communication between the different plug-in cards.
- A high performance connector technology (shielded high-density connector)
- The standard allows for an easy expandability of the ADPMS computer
- Its multi-processor support.

Also the utilization of this industrial specification allowed for the use of commercial off-the-shelf racks, backplanes and processors to support independent board level testing before unit integration.

Modularity and testability have been the key drivers for the selection of the AMBA™ AHB bus for the various System-On-A-Chip designs that were developed during this project. This bus selection allowed for the development of generic IP-blocks that improved the uniformity of the various FPGA designs and as such provided higher flexibility towards late design changes and seriously simplified validation activities.

Peripheral DMA engines

In many existing systems, communication between modules with unequal data rates or large data latencies creates blocking of the shared buses, such as the PCI bus or on-chip AMBA buses. For instance, if a processor wants to send a telemetry packet to the ground station it could either program its internal DMA to transfer the packet via PCI to the telemetry board, or perform direct software writes. In this case the telemetry chain would have to generate a significant amount of waitstates on the bus. This would significantly reduce the throughput for other transfers. Also a 'try-again-later' response would still block the bus due to the processor continuously issuing retries until the transfer is completed. Using interrupts is also no option because the resulting interrupt rate would be not possible to handle by any available kernel for SPARC.

This data latency problem has been solved by the implementation of a local DMA engine on all (rather slow) communication I/F's, like the telecommand, telemetry and the payload communication interfaces. These DMA engines know exactly (because they are part of the peripheral) when the interface has the possibility to transfer more data and therefore only collect the data over the PCI bus at that point in time.

The implementation of local DMA engines on every communication interface has also eliminated the need for FIFO-buffers that are traditionally present in slow target modules. The in- and outgoing data are now directly written into the EDAC-protected processor memory. This results in less power consumption (SRAM memories eliminated), less components (less board space) and because of that a higher reliability. The system is now also very robust against data bottlenecks and is only limited by the throughput of the external interfaces. All major data traffic is done with little or no involvement of the processor and with negligible performance impact. Even if additional interfaces would be added or if the throughput of existing interfaces would be increased, this would still only represent a small bandwidth amount of the PCI and AMBA buses and the system could maintain operation without software or hardware modifications.

Redundancy approach

The ADPMS architecture defines a standard two-lane system with a switchover redundancy scheme. The nominal lane is fully powered and controls the platform, while the redundant lane is powered off.

Compared with the PROBA-I DHS that had at all time two hot-redundant TM/TC modules powered to provide the necessary commanding redundancy. The ADPMS system has a slightly other redundancy concept in order to eliminate the separate power-switch relays for the TM/TC module and to avoid the need for back-biasing protection in the un-powered modules (plugged onto the backplane-bus). Considering that the TM/TC module is connected to the PCI bus where no additional buffers are used, it might be difficult to prevent potentially destructive back biasing of the processor PCI interface. In addition, a future integration of for instance the processor and TM/TC system or the complete lane into one System-On-A-Chip would also be difficult. Having parts of the redundant lane powered also requires that the power supplies are continuously switched on, increasing the failure rate and the overall power consumption. Therefore the ADPMS implements 2 cold redundant nominal TC-decoders and compensates for the fact that they are cold redundant by the addition of a reconfigure and emergency command unit (called RECU).

The main reason to have a separate RECU is to be able to power-down the complete redundant lane and still tolerate one failure anywhere in the system. Being able to power-down a complete lane will save power and lower the failure rate, and allow a future integration of the system into a single SoC device. Since the RECU will be powered continuously, it is logical to group it with the time manager and context memory, which also needs to be maintained during reconfigurations. The RECU TC decoder does not need to implement the full

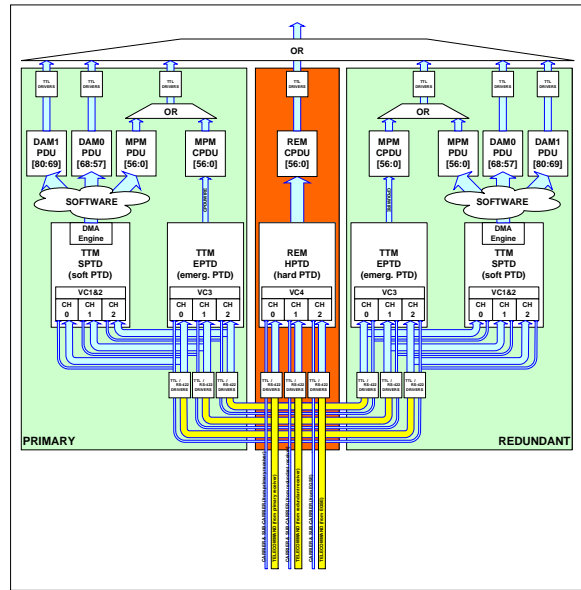
TC standard since it will only be used for reconfiguration in case of nominal TC decoder failure. The decoder only accepts MAP0 CPDU commands - no other MAPs are needed. The RECU CPDU only implements the most critical commands to allow a recovery of the system, further configuration of the system are performed by the (new) nominal lane through software or from ground using the nominal TC decoder.

It can be noted that even if the RECU is not redundant on its own, it poses no single-point failure since it is not used for nominal operation. An error in the RECU leading to an incorrect (unnecessary) lane-switch is not fatal since the second lane will resume operation.

Software packet telecommand decoder

Having a H/W recovery TC decoder in the RECU, the need for a full-blown hardware TC decoder in the nominal and redundant lanes might not be so strong. The argument for hardware TC decoders has been that they are always powered ('hot'), and will work regardless of software errors. Since the recovery TC decoder is 'hot' and since the nominal and redundant lanes have a limited emergency TC-decoder in hardware, this requirement is no longer needed for the nominal TC decoder. Therefore this nominal TC decoder can be implemented in software.

The benefits of a software decoder are several; the protocol can be changed to future versions without hardware redesign, the (hardware) failure rate decreases since less logic is needed, and most of all, the power consumption is reduced. A full-blown hardware TC decoder would consume one large FPGA, a bipolar PROM and a radiation-hard static RAM. These components would have an average power consumption of 0.3 - 1.0 Watt, depending on used device types. A software TC uses virtually no extra power since the performance needed for its operation is estimated to less than 10 KIPS. The only required hardware in this case is a sync-pattern detector (EB90) and a simple state machine to lock a channel. In order to support higher bit rates also a BCH decoder and a DMA channel are implemented. The necessary logic remains within the order of a few kgates, which allows it to be implemented together with all other TM/TC functions in one FPGA. Note that also the PDU function (including TC packet decoding and execution) is implemented in software in case of a software decoder, with only the pulse address decoders and a pulse timer remaining in hardware.



A new processor

A trade-off was made between LEON2 and LEON3 in both FPGA and ASIC implementation. Where the LEON3 (implemented in an ACTEL RTAX2000 FPGA) gives slightly better performance than the former ERC-32. For this project there was a need to demonstrate high computing performance. Therefore the LEON2-FT (AT697 from ATMEL) has been selected.

It has a superior performance with respect to its successor the ERC-32. Also the on-chip PCI host bridge for connection to a high throughput PCI backplane and the availability of a powerful debug support unit made it very suitable for this application. The LEON furthermore supports via its PCI-target interface direct read and write access from/to the main memory, which makes the utilization of the peripheral DMA engines (as described earlier) very straight forward. Because of that the onboard software can concentrate on its processing tasks while all data movement is done with a minimum of software interaction. It is clear that not only the higher clock frequency but also the 7-stage pipeline in combination with the data- and instruction cache make this processor very powerful for a very little power consumption. In addition the LEON allows the utilization of SDRAM memory devices instead of or in combination with SRAM devices. This results in a significantly increased memory capacity for less board space and less power consumption.

A battery regulated bus

The power-bus topology that has been selected for the ADPMS is a battery regulated bus built around the effective utilisation of a Li-Ion battery.

- Compared with traditionally used Ni-Cd cells; the new Li-Ion cell is reducing considerably the difference between the maximum EOC and the minimum battery voltage for the same DOD.
- Typically small satellite bus-units and payload requirements in terms of supply bus regulation are not very stringent, the actual regulation is locally realised by their manufacturers with built-in DC/DC converters.

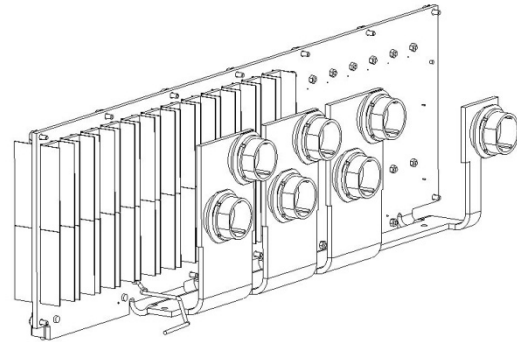
These facts reduce or eliminate the need for a complex and bulky PCS. The advantages being that the complexity of the electronics and the number of components decrease. Which has an immediate effect on the amount of testing involved and increases the reliability significantly. The Power Conditioning Module designed for ADPMS takes advantage of the above elements and is therefore more suited for small satellite application in terms of mass, volume and cost.

Backplane design

The backplane has been designed to significantly ease the S/C integration by the provision of mixed-signal connectors customised for the external units and payloads. It should be noted that this approach integrates the traditionally very complex and bulky S/C harness inside the unit without the need for internal harnessing. This results in easy to integrate one-to-one cables towards the various units, routing both data and power lines (thanks to the integrated power system).

All signals are however still available through the provision of an additional connector per type of interface (the traditional approach). These connectors are now not used anymore in flight configuration but facilitate the S/C integration and testing thanks to the ability to spy on all interfaces (even after full S/C integration) without having to disconnect the flight-harness.

This has been realised by the use of multi-layered flex-rigid PCB's for compact design, good signal integrity and low EMC noise. The backplane also provides the crosscoupling between the primary and redundant chain.



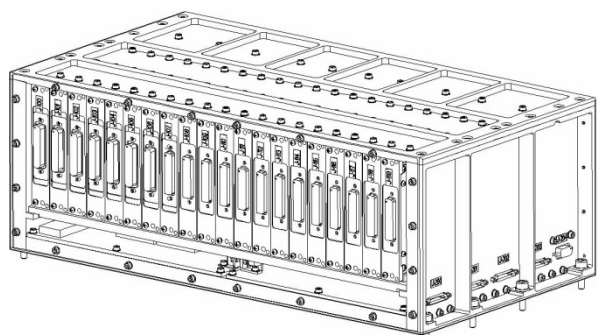
Mechanical improvements

Thanks to the small form factor of the electronic boards the ADPMS housing has a limited height and the possibility to expand in the length while maintaining the same height. This makes this unit very suitable for small satellites with a high level of integration or a large payload to accommodate. The availability of test spy connectors on the opposite side of the box compared to the real flight connectors allows the box to be mounted on the satellite in a way that easy test access is guaranteed even after full spacecraft integration. The thermal control of the box is fully passive and the box has been designed for vibration levels compliant with a wide range of launchers facilitating the selection of a piggyback launch. Detailed 3D modelling and multiple design iterations have been performed to achieve an optimal highly integrated housing design.

Flight connector side



Test spy connector side



NEW TECHNOLOGIES

The ADPMS has benefited from today's rapid evolution of electronics, by the usage of low power, low voltage components. The selection of lightweight connectors and the extensive utilization of surface mount technology. Furthermore the recent availability of large, radiation tolerant FPGA's made it possible to replace several smaller FPGA's and ASIC's by highly integrated System-On-A-Chip designs.

PAYLOAD SPECIFIC ELEMENTS

Payload specific electronics that are typically developed for every new satellite are traditionally hosted in a separate unit (per company involved), to facilitate the interface management and testability. This results in a less optimal spacecraft design (with respect to volume, mass and power) and in more software development in most cases. Thanks to the open architecture of the presented avionics different suppliers and developers can now supply subsystem cards, developed according to the well-defined industrial Compact-PCI standard, for integration into the central processing unit.

In the frame of the Proba-II project some payload specific electronics have been developed by the payload provider and without problem integrated as a plug-and-play extension board into the Verhaert Space onboard computer

CENTRALISED VERSUS DISTRIBUTED

There is a tendency to use mature off-the-shelf flight equipment onboard small satellites. Leading to the need for a flexible satellite architecture. Therefore the ADPMS satellite control unit supports centralized and distributed computing.

In addition to that, small satellites tend to be highly integrated and their shape is highly depending on the payload they carry, and the piggyback launch opportunities they have. To facilitate these accommodation constraints the ADPMS satellite control unit supports centralized and distributed I/O.

The satellite computing can be done in a centralized way thanks to the high throughput backplane and the possibility to plug-in additional co-processors if needed. On the contrary also distributed computing is supported thanks to the provision of several serial communication interfaces to interconnect the different computing units, and the provision of two high-speed CCSDS encoded direct downlink channels for external usage.

To allow flexibility in the satellite accommodation, the ADPMS can be connected to the other satellite units, sensors and actuators in a centralized or distributed way. This is realized in practice by the capability to plug the I/O-cards directly onto the backplane or to operate them as RTU's. And allows the satellite

provider to trade-off several small boxes versus one large box and the harness related to that. This in the frame of optimal spacecraft design and easy access during AIT activities.

'PLUG & PLAY' = RAPID ADAPTATION

Rapid adaptation to any satellite need is really the key feature of ADPMS. It is clear that most small satellite missions require optimal solutions both from a technical and financial point of view. This requires a flexible and modular approach at the spacecraft controller level to avoid redesign as much as possible and on the other hand to allow geographical distribution of the development. The ADPMS can be seen as an open framework that can host any combination of existing or newly developed modules. The baseline configuration for Proba-II consists of various different sub-modules like: processing, TM/TC, spacecraft communication, data-acquisition and reconfiguration. But without any problem the ADPMS could also host a set of identical memory modules + a processor module resulting in a high capacity mass memory with built-in data processing capabilities like video recognition or other. Another example could be to plug several identical processor modules in the ADPMS resulting in a 800Mips computer unit.

QUALIFICATION

Several new technologies like the AT697E from ATMEL and the RTAX2000 from ACTEL have been incorporated into the ADPMS and will have their first in-orbit results end of this year thanks to the Proba-II mission. In order to use these new technologies in a reliable way, the following qualifications have been achieved for this project. A reflow qualification for the soldering of high pin count, small pitch column grid array packages like the 624-pin CCGA and the 349-pin MCGA. A manufacturing qualification for 26 layers flex-rigid printed circuit boards and a new via-filling process to support the layout of small pitch column grid array packages without the need for blind vias (reducing cost, time and risk). A qualification for the use of press-fit connectors providing increased reliability for higher vibration levels.

THE RESULT

The ADPMS configured for the Proba-II satellite offers the following functionality for the following budgets:

Functionality

- Backplane data traffic up to 1,6 GBps
- Multi processor support
- Processor board
 - o designed for 100MHz operation with tunable clock frequency.
 - o 64 Mbyte SDRAM / 4 Mbyte SRAM
 - o 4 Mbyte Flash / 256 kByte Prom

- Telecommand
 - o 2 Mbps uplink capability (RS422)
 - o Four virtual channels or more
 - o Configurable amount of MAP-IDs
 - o 56 CPDU channels
- Telemetry
 - o 100 Mbps downlink (LVDS/RS422)
 - o Five virtual channels
 - o 2 packetwire inputs (LVDS/RS422)
 - o full encoding
- Mass memory of 4 GBit (with EDAC)
- Context memory of 128 kByte (with EDAC)
- Communication Interfaces
 - o Up to 25 UART channels (RS422)
 - o Up to 6 TTC-B-01 channels (RS422)
 - o Camera interface with frame grabber
- Analog interfaces
 - o Up to 80 analog inputs
 - o Up to 32 temperature inputs
- Power conditioning
 - o Max satellite peak power 300W
 - o Up to 6 solar sections
- Power distribution
 - o 24 outputs of 28V / 50W
 - o current protected with auto restart
 - o switchable or non-switchable
 - o Battery undervoltage protected with auto switch off
- H/W generated emergency telemetry
- Centralized time synchronization

Budgets

- Mass: 13 kg
- Volume: W=455mmxH=160mmxD=267mm
- Power: 17 W

CONCLUSIONS

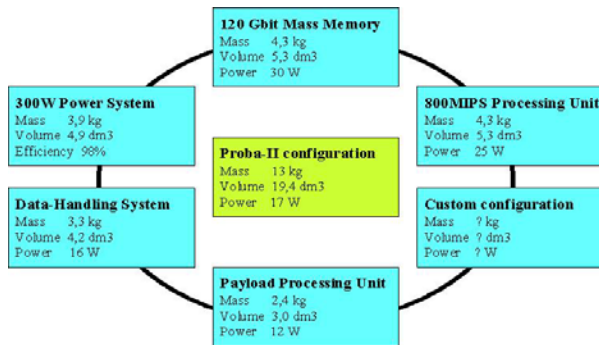
Herewith an overview of the realized design compared to the initial top-level requirements that were outlined at the beginning of this paper.

	Power	Mass	Volume	Design Uniformity	Open architecture	Performance	Modularity	Scalability	Testability
Five bus elements into one system	↘	↘	↘	↗			↗	↗	↘
Compact PCI spec	↘	↘	↘	↗	↗	↗	↗	↗	↗
Small 3U form factor		↗	↘				↗	↗	
SoC designs based on AMBA AHB spec	↘	↘	↘	↗	↗	↗	↗	↗	↗
Peripheral DMA engines	↘	↘	↘			↗		↗	
Soft PTD	↘	↘	↘		↗			↗	↗
Redundancy Approach	↘	↘	↘					↗	↗
LEON2-FT usage	↘	↘	↘	↗	↗	↗	↗	↗	↗
Backplane design		↘	↘	↗	↗		↗	↗	↗
Mechanical concept		↘	↘	↗	↗		↗	↗	↗
New technologies	↘	↘	↘			↗			
Overall result	↘	↘	↘	↗	↗	↗	↗	↗	↗

Looking at the result of the previous table one can conclude that the ADPMS is a state-of-the-art control unit specifically designed for small satellites. It allows rapid adaptation to a diversity of next generation satellites and the addition of third-party cards thanks to its open ‘plug and play’ architecture. Resulting in a more optimal spacecraft design, the possibility to outsource design activities and a reduced software effort with a consequent reduction in recurrent development costs and a shorter production cycle.

OTHER CONFIGURATIONS

Thanks to its modularity, the ADPMS can be easily configured for other applications.



KEY FEATURES

High performance

- 100MIPS LEON processor
- 1Gbit/s high throughput backplane
- 4Gbit mass memory (easily expandable)
- 100MBit/s downlink capability

Low power consumption

- low power, low voltage components (3,3V&1,5V)
- utilization of large radiation tolerant FPGA's

Miniaturized avionics (mass & volume)

- Optimal highly integrated housing design
- Qualification of new high pin count CGA-package
- 99% surface mount technology (SMD)

Easy satellite integration

- Easy test access guaranteed after S/C integration
- Open architecture (↔black box design)
- Improved testability
- Thermal control fully passive

Growth potential – High re-use factor

- High throughput backplane
- Multiprocessor support
- Modular & scalable design
- Third-party board integration

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