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MOSFET Audio Amplifier

Jeff Argast

Utah State University

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MOSFET Audio Amplifier

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Logan, Utah

June 1991

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EXECUTIVE SUMMARY

My senior project is an audio amplifier utilizing MOSFETs as the output transistors to drive the speaker. Within this document I cover the details of designing an amplifier, and the methods used to build it.

The most important part of the project is the output stage. In this section I chose MOSFETs over BJTs. Several advantages ensued from this decision, resulting in a simple design.

Further, the transformer must be able to supply the necessary currents for the transistors. Because large musical peaks are possible, resulting in sizable power surges, I had to obtain a large transformer with adequate specifications. It was also quite heavy.

Since it was so weighty, I had a rack-mount chassis, with the appropriate stress requirements, donated. And mounted within is the entire project, from power-on switch to circuit board to speaker terminals.

The schematic layout and simulation of the circuit was done on Workview (TM) and PSPICE respectively. These two application programs provided more than enough processing power to generate the necessary design. A printed circuit board was laid out with Autocad from the schematic and then, as explained in this paper, eventually etched.

With all this preparation and design, however, the amplifier did not work because of inadequate heat dissipation and MOSFET biasing difficulties. In the final two sections I detail what specifically went wrong, the steps needed to alleviate the above dilemmas and what I learned most about the entire project process.

1.0 INTRODUCTION

Music has been a part of society for hundreds of years. Starting with the great composers it has evolved from conducting massive orchestras and symphonies to what we have today -- massive orchestras and symphonies on keyboard. But regardless of whether you like the classics, heavy metal, pop, jazz, rap or many other styles, most everyone wants it to sound awe-inspiring, as if you were right there.

While notes and bars have been around awhile, recording and reproduction of it has only emerged in the last century. And of that, only during the previous 20 years has the quality gone from good to unbelievable. Today we can nearly make a recording sound like the live performance. Many of us, however, cannot afford the equipment necessary.

For the average consumer there exists a plethora of stereos capable of producing distortion and noise free music. It doesn't have the imaging the expensive systems do, but it provides something close for a fraction of the cost.

At the heart of every system is the amplifier. In today's world of digital music, the quality of sound coursing through the right and left channels is practically distortion and noise free. Consequently the amplifier needs to deliver the continuous plus peak demands that music requires without muddling the signal with sixty hertz hum or other noise or adding harmonics that weren't there to begin with. Not only a good design, but also an intelligent layout of the components is needed to satisfy these criteria.

Most designs choose what is commonly called a "cascade" circuit using bipolar

junction transistors. While an excellent choice, since it has been tried and tested for many years, devices and alternate approaches exist to obtain the same thing for less. Less money, less time and less hassle. The following report is a detailed account of such an alternative, from the initial conception to the final product.

2.0 BACKGROUND

When BJTs became popular, the design most often used (and still used) consisted of four stages as shown in figure 1 -- buffer, gain, pre-driver and driver. Each were cascaded together with coupling capacitors. Feedback was usually in the circuit for linearity and reduction of distortion.

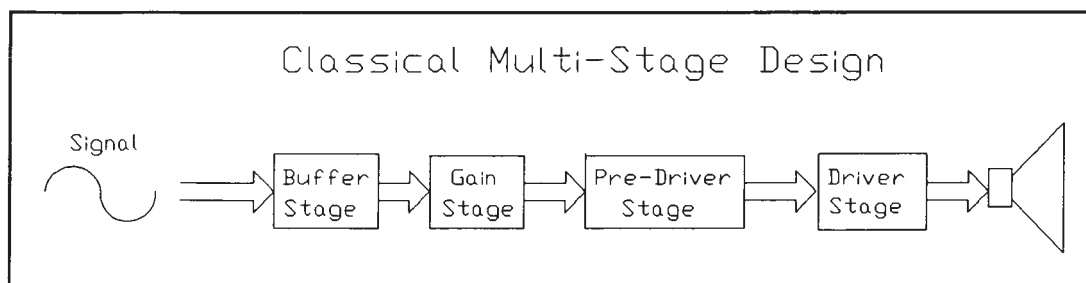


Figure 1

The buffer stage purpose is to isolate the gain from the input, and reduce noise. It also won't affect the frequency characteristics much because its output resistance should be low and the gain is most likely less than or equal to one.

The gain stage is two or three individual BJT amplifiers connected together using capacitors to achieve the desired response. Nominally it is linear and defines the low frequency cut-off of the amplifier.

The pre-driver stage is necessary when using BJTs since the base current can be quite large. This stage has a gain of less than one, usually a voltage follower

configuration, and the BJTs are of the power variety.

Finally, the driver class AB stage to pump the music through the speakers. Depending on the specifications of the amplifier, this stage will provide up to several amps, hence the above mentioned need for pre-drivers. Again, this stage has a gain slightly less than one and the output choke and capacitor define the high-frequency cut-off.

Prevailing for many years, the cascade design has been easy to implement and build. But it is not without serious problems. To begin with, using coupling capacitors can degrade the signal and cause phase shift in the signal. While the human ear cannot detect the phase shifting, it may cause the amplifier to go unstable. Moreover, the capacitors tend to bring the low frequency cutoff up too high. Or they are prohibitively expensive and large if higher value caps are purchased for lower frequency response. Second, BJTs are non-linear in the active region, which may cause distortion in the signal. Last, the circuit is horribly inefficient, because of the multiple biasing currents needed for the various stages and the base current for the output section.

To solve these problems, I have used a different design and output devices. Foremost I am using MOSFETs instead of BJTs for three distinct reasons. First, MOSFETs have a negative temperature coefficient making them stable against thermal runaway. Second, power MOSFETs are very linear in the active region, adding little distortion to the signal. And with some feedback it can very nearly be eliminated. To end with, MOSFETs have almost no gate current. Consequently, they

are more efficient and do not require a pre-driver stage.

Shown in figure 2, the design I used is not the conventional cascade either. It uses two p-channel jfet transistors in an source-coupled pair configuration for the input and two npn transistors for the gain. Advantages are as follows: 1) The use of source-coupled pairs allow direct connection between the input and the output stage. 2) Fewer biasing currents, therefore more efficient. 3) It acts like a huge operational amplifier, with an inverting and non-inverting terminal, making two feedback resistors the gain specifiers -- much easier to design and modify.

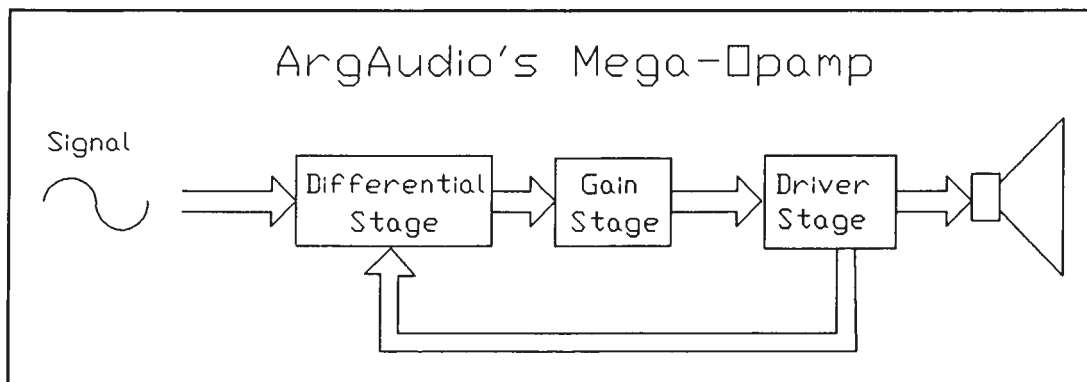


Figure 2

3.0 REQUIREMENTS

Table I shows the requirements established prior to design:

Table I

Power Output into 4 Ohm Speaker:	At least 100W per Channel
Signal to Noise Ratio:	Greater than 80dB
Total Harmonic Distortion:	Less than 1%
Over Current Protection:	Cut-off at 6 amps

100 watts is more than enough to be loud and 80 dB S/N ratio is barely audible. Moreover, you can't hear distortion below 2%, and over current clamping at 6 amps will protect the speakers.

Table II lists components that will be part of the final product:

Table II

<ul style="list-style-type: none">● Fused power supply● Switch to connect speakers after turn-on transients● Rack-mount chassis

4.0 DESIGN

There are five sections to the amplifier, power supply, input, gain, output and protection section. The entire schematic is shown in appendix A1. The first page is the transformer model along with simulation input signal and PSPICE parameters. The next two pages show both left and right channel input/gain stages and the last two pages have the left and right output sections.

4.1 POWER SUPPLY

The power supply consists of a simple bridge rectifier and 4000uF noise capacitors.

The diodes are rated at 6 amps continuous and forty peak, while the transformer can provide

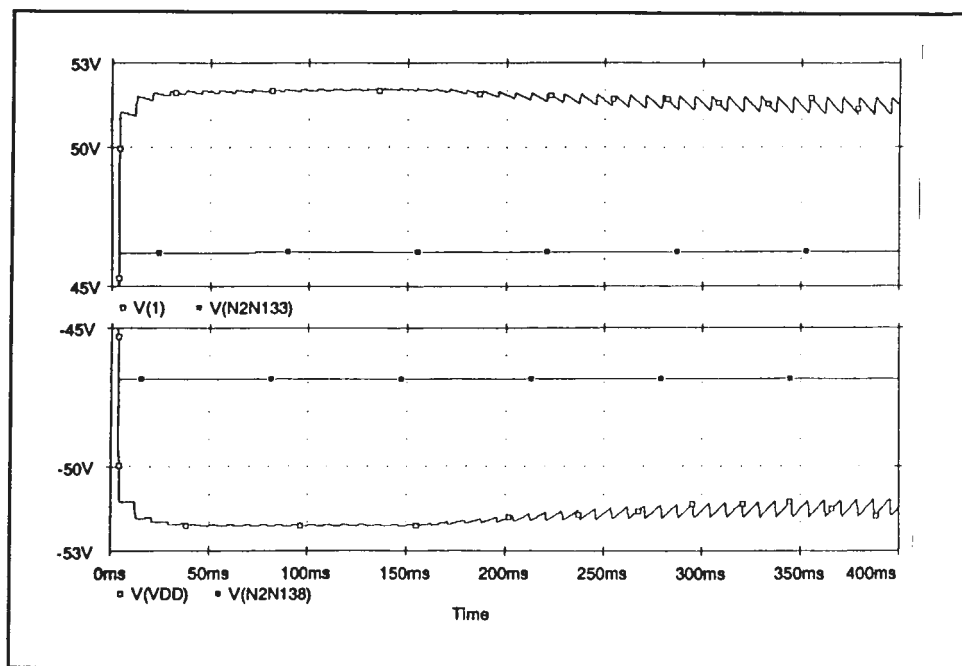


Figure 3

PSPICE Simulated Supply Ripple

ten amps continuous.

At no load conditions, the ripple is less than two volts. The power supply is further

regulated after the output section with a zener-BJT combination, dropping the voltage to 46.3 volts. This supplies the rest of the circuit with power.

To model the transformer in PSPICE, I used a split voltage source design with the center being ground. Each is set to give a 75V RMS line out, comparable to actual

measured values.

Figure 3

shows the

PSPICE

simulated

ripple and

regulated

power

supply

voltages

during no

input signal

condition. Figure 4 exemplifies the current in the noise capacitors during and immediately following initial power up.

4.2 INPUT DIFFERENTIAL PAIR

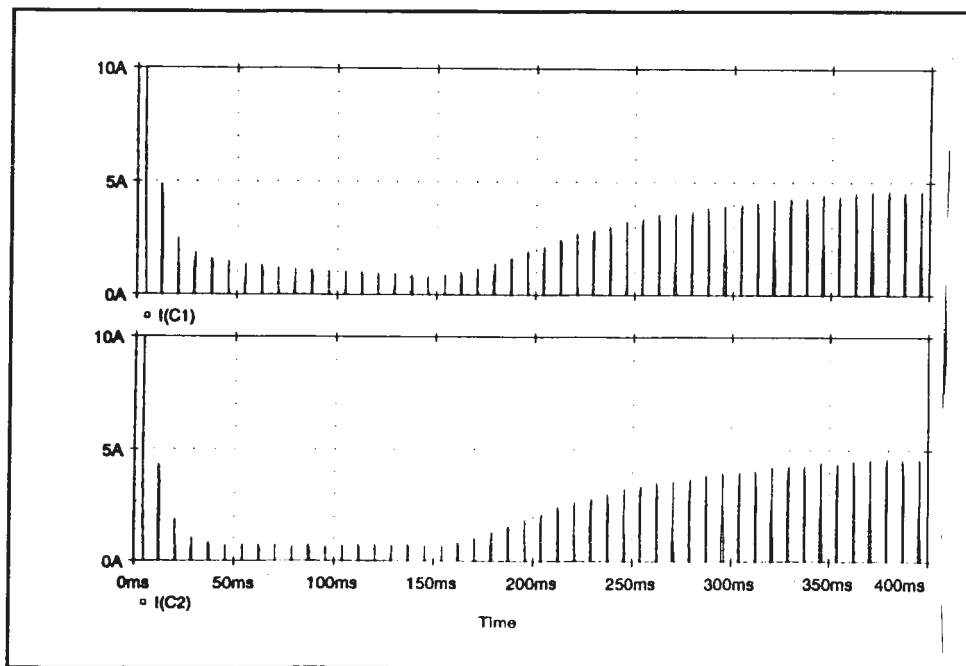


Figure 4

Capacitor Charging Currents

The input section has a p-channel jfet differential pair as a buffer and for feedback. Its gain is -20dB so the noise from external sources is minimized. The bias current is 1mA for each transistor and is supplied through an additional RC network to purge any further noise from the rails. A load resistor of 910 ohms in the drain circuitry is used for biasing the gain section. Two J2N5463 transistors were utilized, and PSPICE had a J2N5462 model in the library, which is the same with a slightly

l o w e r

breakdown

v o l t a g e .

Shown in

figure 5 are

three traces

o f t h e

o u t p u t

w a v e f o r m s

i n e a c h o f

t h e

f o l l o w i n g

c o n d i t i o n s ,

d e m o n s t r a t -

i n g t h e a b i l i t y o f t h e j f e t p a i r t o r e d u c e t h e e f f e c t s o f i n p u t l o a d i n g : F i r s t i s n o s i g n a l r u n n i n g , t h e s e c o n d a l o w i m p e d a n c e s i g n a l s o u r c e o p e r a t i n g a t 1 0 0 m V a n d l a s t , a

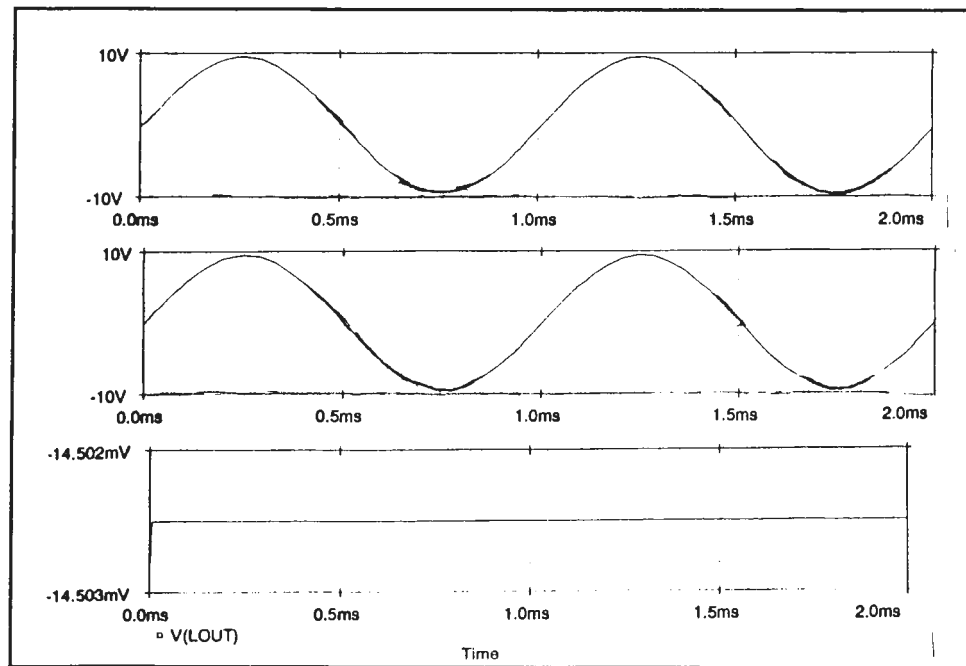


Figure 5

Output Offset Voltage

high impedance source also at 100mV. Specifically, The thing to notice is how each output signal has the same DC offset, set by the biasing network only and not affected by the input source. The nos signal value of -14mV, while not zero, is for all practical purposes not a problem for sound reproduction and speaker handling.

4.3 GAIN STAGE

After the signal is passed through the differential pair, it is boosted by an open loop gain of >2000. The actual gain is specified by the feedback resistor ratio. In effect, the amplifier acts like a massive opamp, wherein the non-inverting terminal is for the input signal and the inverting for feedback. The gain is therefore $1+Rf1/Rf2$. Bias current in the gain stage, using a 2N5550 is 5mA, which after passing through the two 4.3k resistors, leaves a DC voltage of 3.5 resting on the gate of the n-

channel
output
MOSFETs.

A fourth
transistor,

also a
2N5550,

adjusted with a variable resistor in the base circuitry, varies the voltage difference between the n-channel and p-channel devices. After experimentation, the variable

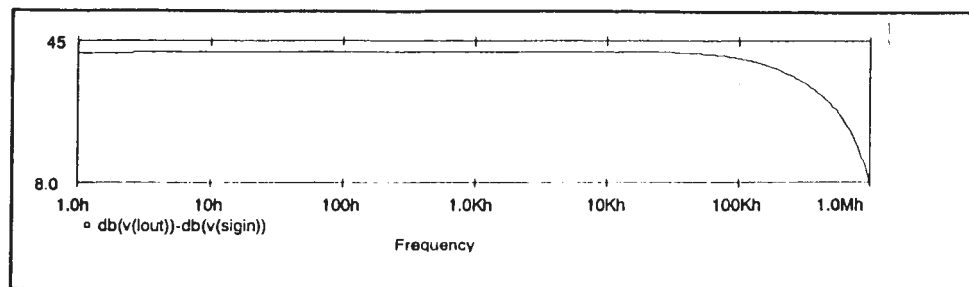


Figure 6

Amplifier Simulated Frequency Response

potentiometer is set so the MOSFETs are barely on. This removes the crossover distortion, characteristic of a solely class B amplifier, from the output.

Figure 6 exemplifies the bode plot of the overall gain within the circuit. The low frequency cut-off is defined by the transistors, while the high frequency is determined from the input RC network and the output RLC network. The response falls off at 100khz to reduce the chance of oscillations in the output stage.

4.4 OUTPUT STAGE

The output section consists of four MOSFETs, two sets of two complementary pairs. A .22 ohm resistor is connected in each source. The speaker can be (and is) directly coupled with the output. The RLC network in the output is needed to limit high-frequency response because with the capacitive effects of the speakers, MOSFETs tend to oscillate under certain conditions. This effectively eliminates that possibility. These MOSFETs can supply up to 10 amps continuous current under ideal conditions, but will only ever need to provide 3 in the amplifier.

The protection circuitry consists of zener diodes on the gates to clamp the output to 35V. BJTs are across the .22 ohm resistors for over-current protection, clamping the output at 6 amps. The combination of both the BJT and zener allows protection against a varying impedance load. A switch will be used to connect the speakers following turn-on, allowing transients to pass through without affecting them. Finally, fuses will be in the power lines in the event of shorting the output to ground. In this case, the amplifier will clamp at six amps and the fuses will blow.

Figure seven shows a distorted output waveform corresponding to one watt, the fourier of a non-distorted waveform and the fourier response of the distorted signal at 1khz.

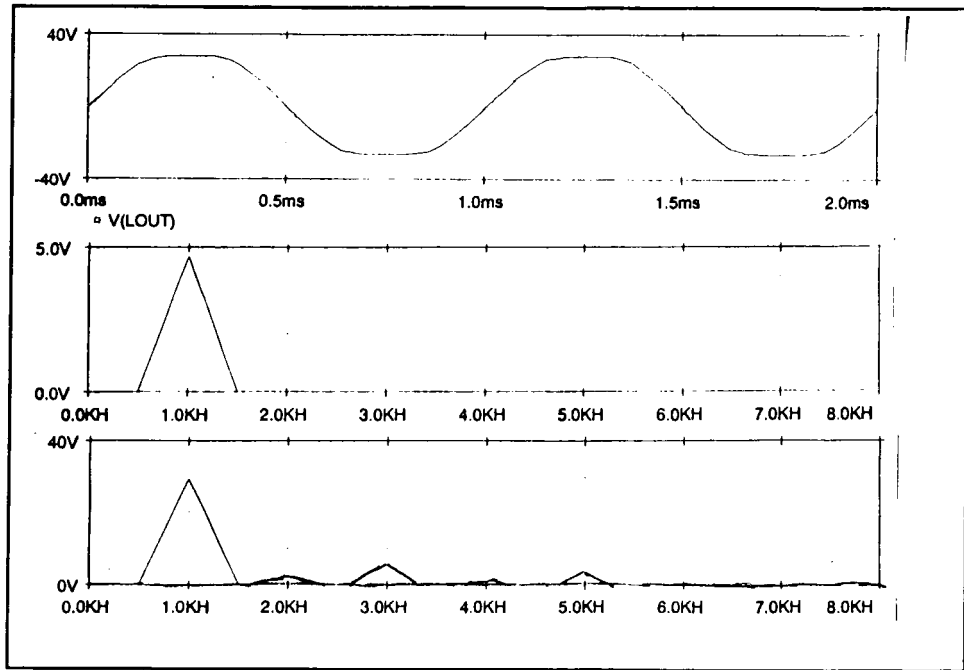


Figure 7

Fourier of Simulated Output

5.0 TEST PLANS

The audio amplifier will be tested on four points:

- Continuous Output Power
- Peak Output Power
- Harmonic Distortion
- How It Sounds

Continuous Output Power

The amplifier will be tested for rated output power by running a 1 khz sine wave input to a 4 ohm load at 3 amps for one hour. The output test will be successful if the amp does not fail.

Peak Output Power

The amplifier will be tested for peak output power by running a 1 khz sine wave modulated into 10ms pulses separated by 1 second with a peak value of 6 amps. The test will be successful if the amp does not fail.

Harmonic Distortion

The amplifier will be tested for total harmonic distortion by piping the output through a fourier analysis oscilloscope, using a 1khz wave at one watt. The test will be successful if the distortion is not over 1%.

How It Sounds

The amplifier will be tested for how it sounds by playing various types of music through it with two 4 ohm speakers hooked up. The test will be successful if I find the sound pleasurable.

6.0 DEVELOPMENT AND CONSTRUCTION

6.1 BOARD LAYOUT

Using Autocad, with the trace and donut commands, I laid out the design for a circuit board, shown in appendix A2. Each trace is a minimum of 0.1" wide and the donuts have an inner diameter of .025" and an outer diameter of .07" for resistors, capacitors and small signal transistors, while for the MOSFETs and power supply regulation transistors the inner is .03" and outer is .08". This allows for the possibility of accidental over-etching and for the traces to handle more current.

6.2 BOARD ETCHING

After completing the layout, it was printed out on a laser printer. Next the layout was taken to a printshop where a PMT was made from the printout, darkening all traces so they were completely black. Third, an acetate was made from the PMT (also done at a printshop) which essentially is the same thing as an overhead photo image, except the traces are 100 times darker. The acetate was then used to mask a pre-sensitized board during ultraviolet light exposure. Areas of the board not covered by traces became susceptible to an etching agent, which the board was placed in following the ten minute exposure. Finally, after etching, the PC board was placed in an etch-resist remover which dissolved any sensitizer left on it. A little steel wool made the copper clean and ready to be soldered to.

Following soldering each component, except the MOSFETs, to the board, it

was tested and calibrated for the proper gate offset voltages. The MOS transistors were then soldered to the board and again it was tested. At this point a problem became evident, which is covered in test results following this section.

6.3 PACKAGING

The transformer, because of its weight, is mounted against the front panel. Each channel circuit board is mounted in the back two corners, with the capacitors next to the front, running power to each board.

Each MOSFET is attached to the heat sink via a 4-40 1/2" screw. A plastic insert and mica sheet isolates the tab from the heat sink. A silicone preparation is used between the MOSFET, mica and heat sink to allow for efficient thermal transfer.

A power switch and ON light were attached to the front panel along with rack mount handles. On the back were placed the speaker terminals and connect switch for both channels. The power cord runs directly into the center bottom of the back panel.

7.0 TEST RESULTS

The amplifier did not function as it should have according to PSPICE simulation. Apparently the problem lies in dealing with the loading effects of the MOSFETs and the betas associated with the Q2N5550 gain stage transistors. As the data listed in table I show, the theoretical gate voltages for the MOSFETs show approximately an eight volt difference between them. During the final pre-testing stages, the gate voltages were measured to be quite close to eight volts. When the MOSFETs were added to the circuit, however, the voltages dropped to the values shown, clearly demonstrating an interaction PSPICE had not taken into account.

7.1 POWER SUPPLY

The test results obtained were excellent concerning the ripple on the rails voltages. Moreover, the regulated supply worked to specifications, albeit the voltage level was slightly high.

7.2 JFET DIFFERENTIAL PAIR

The JFET simulation showed a V_{gs} of 1.5 volts, but the zero measured actually corresponds to the value in the data books for this particular configuration. And, the source currents were almost exactly the same.

7.3 GAIN STAGE/OUTPUT SECTION

While the bias level for the gain transistors closely matched that of the

Table III

Theoretical and Experimental Result Comparison

	Theoretical	Experimental
<u>POWER SUPPLY</u>		
Ripple	2V	1.2V
Regulation	46.3V	47.8V
<u>JFETs</u>		
V _{gs}	1.5V	0V
I _d	.9mA	.9mA
<u>GAIN STAGE</u>		
I _c	5mA	5.1mA
<u>MOSFETs</u>		
V _{gs(N)}	3.5V	2.7V
V _{gs(P)}	-3.7V	-2.9V
I _d	60mA	10mA
I _g	50nA	250uA
<u>MEASUREMENTS</u>		
Noise	100dB	>85dB
Distortion	.2%	>50%

simulation, the voltages on the gates of the MOSFETs, labeled RPGATE, RNGATE, LPGATE and LNGATE in the schematics found in appendix A1, from the bias stage did not provide enough offset to turn the transistors on.

7.4 DISTORTION AND NOISE

The noise level transmitting to the output in actual test results was comparable

to another amplifier that has a signal to noise ratio of 85dB. This is not quite as good as the simulation, but given the effects a poor layout or noisy power supply can have (which PSPICE does not simulate), the result was quite acceptable.

7.5 OVERHEATING

The final and most unexpected problem was heat dissipation from the MOSFETs. To achieve low distortion numbers, the output section needed to be biased anywhere from 60-100 mA. This corresponds to about 1 watt of heat dissipation. Upon trial testing of the amplifier, the output section overheated and destroyed the MOSFETs.

8.0 CORRECTIONS

The amplifier did not function as it should have according to simulation. Consequently, I have here a set of proposed changes to alleviate the problems with the project.

8.1 BIASING

The gate currents for the MOSFETs, while small, is not negligible. For both the P- and N-channel devices, the current almost totalled 1mA, more than enough to reduce the gate voltages to below the threshold. To correct this problem, a set of transistors immediately after the gain stage but before the output section, configured with a gain of one, is needed to supply the necessary gate currents. In this way the appropriate offset voltages should be obtainable.

8.2 HEAT SINKING

In order to dissipate enough heat, the transistors need to be mounted flush to an efficient heat sink. The ones I used may have a too high a thermal coefficient to be able to use them. Moreover, I did not have the MOSFETs connected to the heat sinks close enough, owing to less thermal transfer and device failure. To correct this problem, the boards need to be mounted closer to the heat sinks, and verification of effective thermal conductivity must be made of the heat sinks.

9.0 CONCLUSION

Someone once said you can learn more from a mistake than from the right answer. This project was a failure that succeeded in broadening my understanding beyond what I gained from the classroom.

The most important consideration of the entire project is time. Time sneaks up on you without sight nor sound. Many of the processes used to develop the project were alien to me, and I had to learn as I went. I had no idea how to layout the design for a PC board, let alone etch. I assumed, wrongly, it would take only a couple of weeks to learn. Furthermore, finding the proper materials and adequate facilities to process the circuit boards took up considerable time. Consequently, I ended up rushing much of the construction when I finally got to it.

A further ramification of not budgeting my time effectively, is putting off the technical writing associated with the amplifier. I waited until near the end of completion before actually beginning to scribble anything down. This resulted in cluttered and ill-remembered lab notes.

In all, it was an excellent learning experience, and if I had it to do over again, it would be done more efficiently and with better organization. For the future, I now have a more realistic view of how long it takes to make a finished product, from conception to completion.

ACKNOWLEDGEMENTS

My deepest gratitude goes out to Dan Baker, without his help this project would not have come to be. He donated both the rack mount chassis and the massive power transformer.

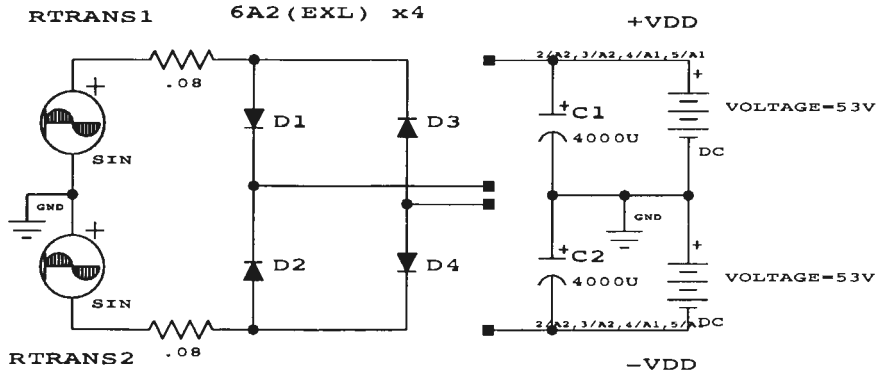
APPENDIX A

Technical Reference Manual

Following is the schematic of the amplifier, containing both the right and left channels along with PSPICE simulation data. The PC board layout is include afterward, and the parts list is at the end.

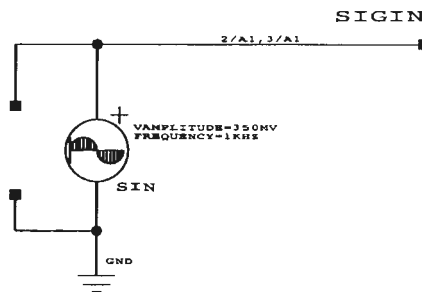
Power Supply

D1-D4:
 MB352(EXL) x1
 OR
 6A2(EXL) x4



Transformer Model

106V Peak



OSCILLOSCOPE

TSTEP=1US
 TFINAL=2MS

CSDF

OPTIONS

ITLS=50000

Title: Distant Thunder

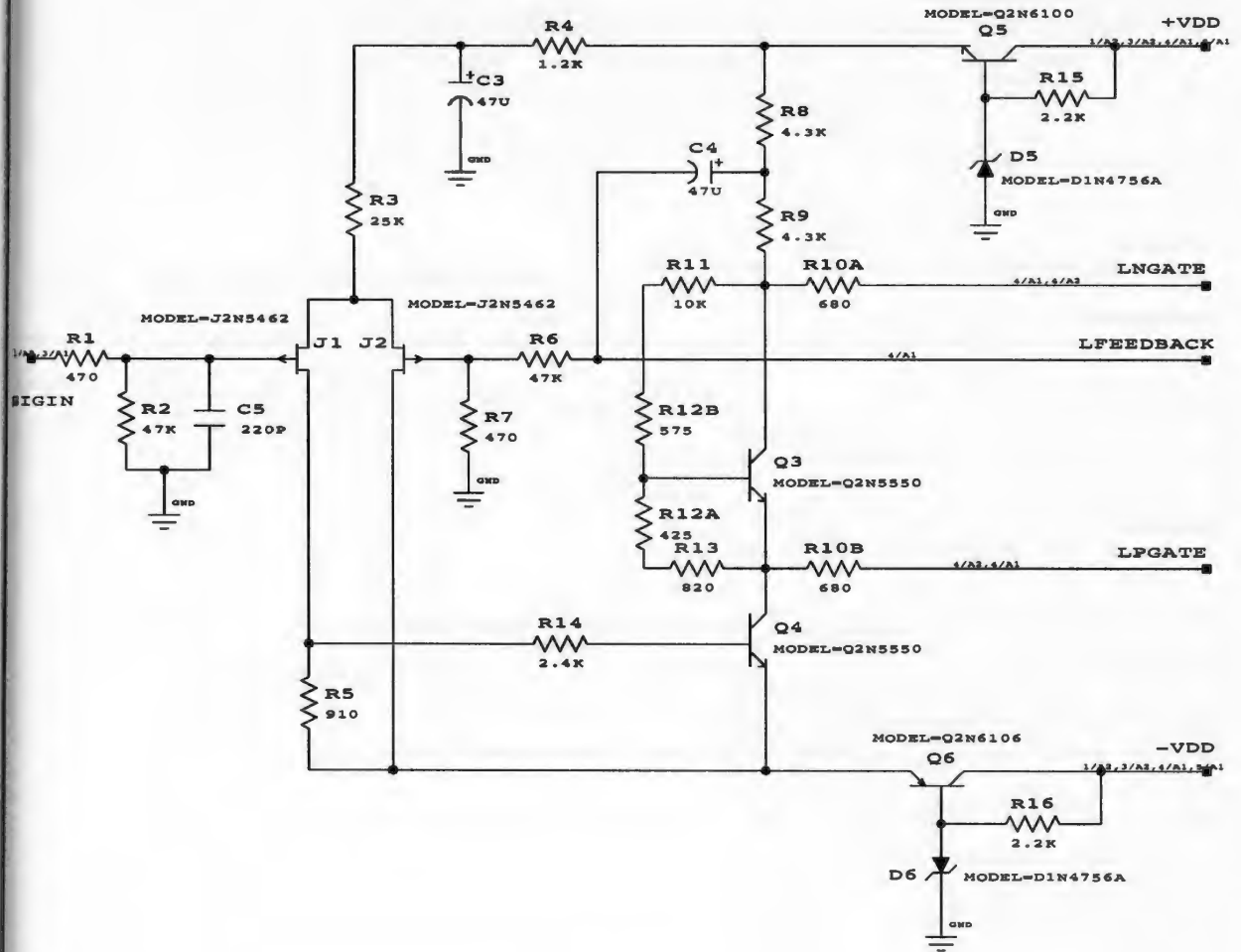
ArgAudio

MOS Power

24

Auth	JDA
Date	05/20/91
Rev	

Left Channel Input Stage



Title: Distant Thunder

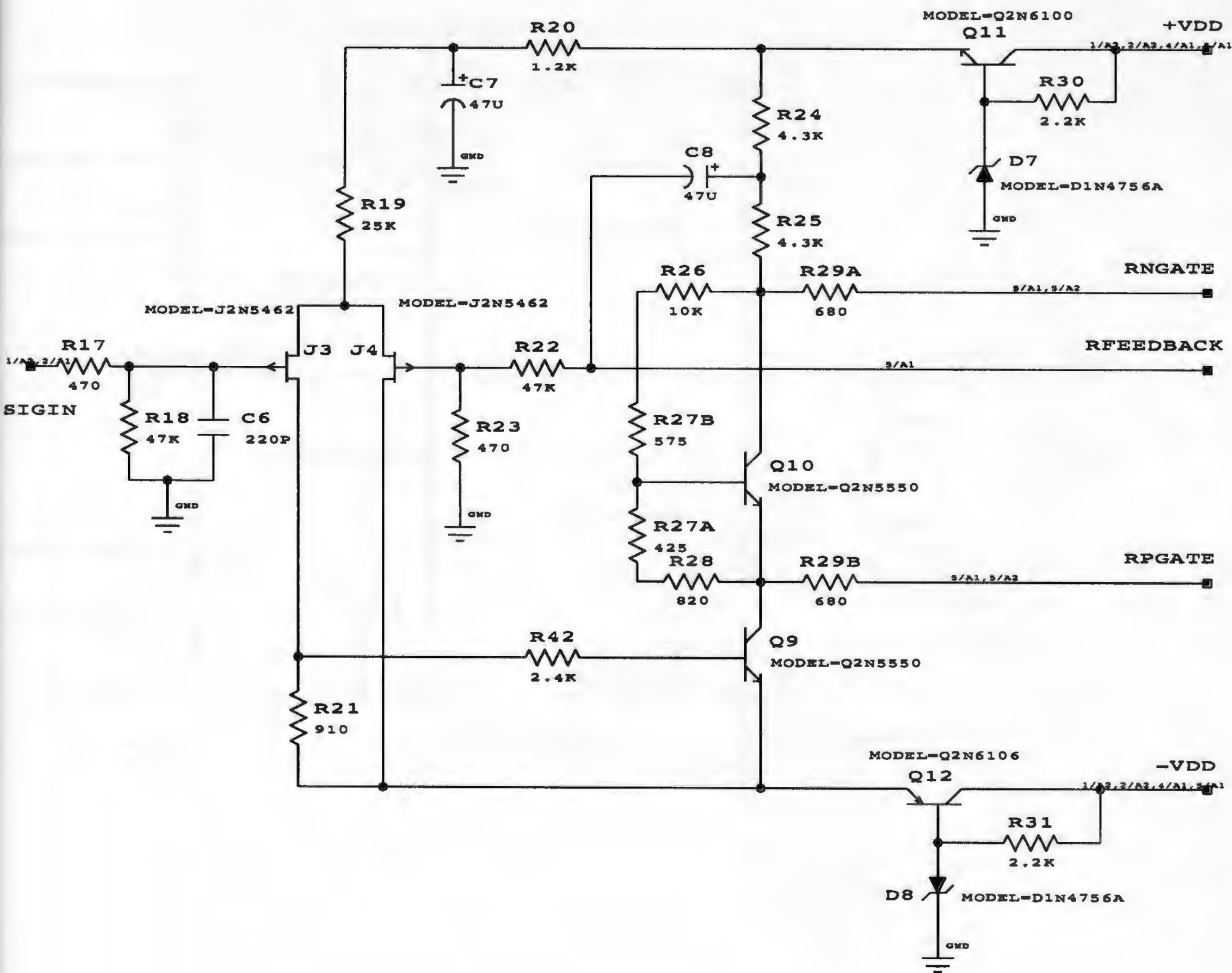


MOS Power

25

Auth	JDA
Date	05/20/91
Rev	

Right Channel Input Stage



Title: Distant Thunder

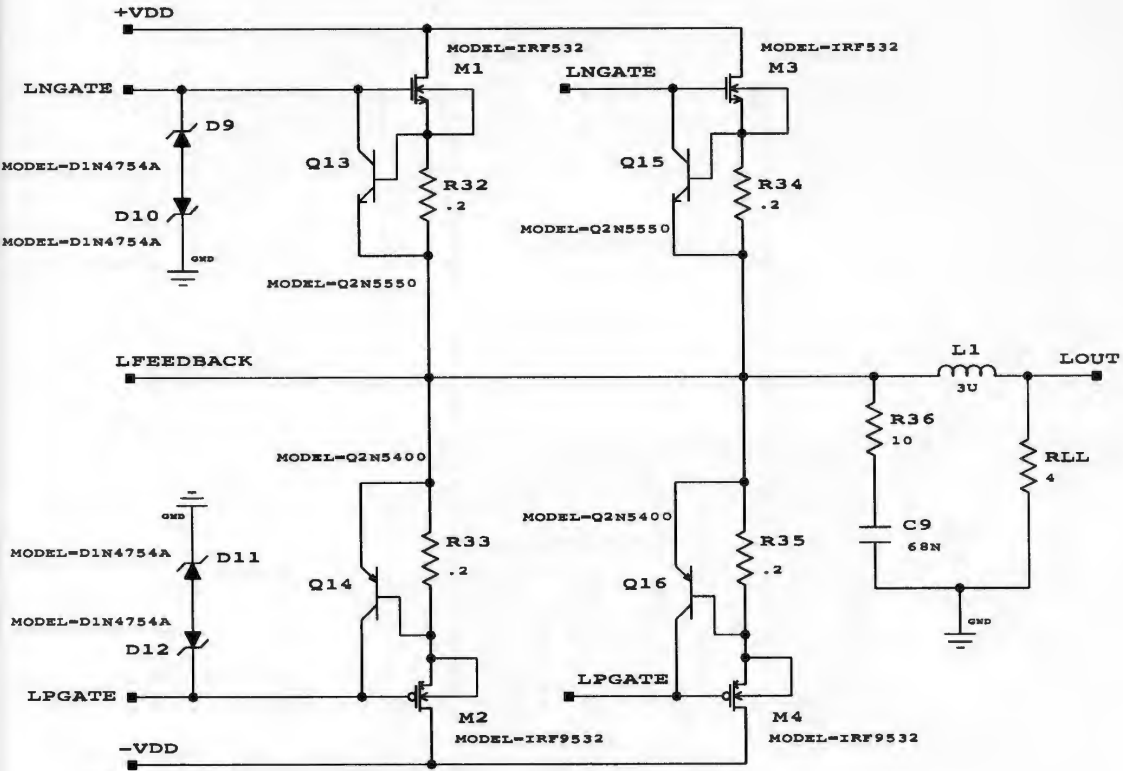
ArgAudio

MOS Power

26

Auth	JDA
Date	05/20/91
Rev	

Left Channel Output Stage



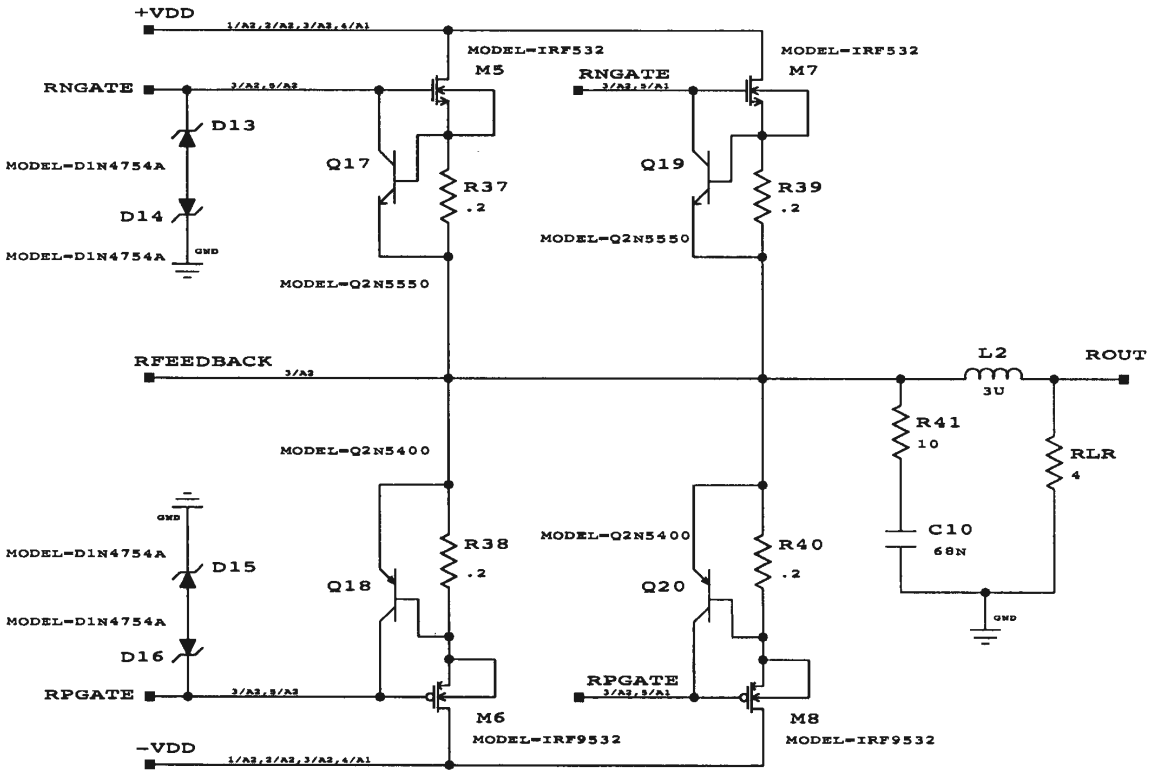
Title: Distant Thunder



27

Auth	JDA
Date	05/20/91
Rev	

Right Channel Output Stage



Title: Distant Thunder

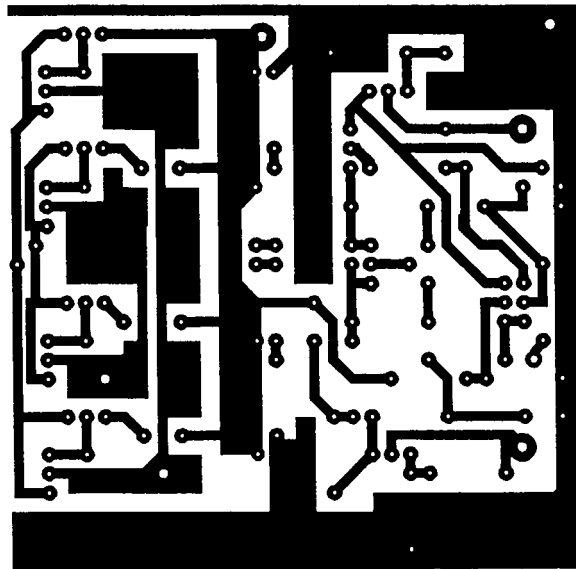


28

Auth	JDA
Date	05/20/91
Rev	

PC Board Layout

Actual Size



Parts List

- 8 - Q2N5550 NPN high voltage transistors
- 4 - Q2N5400 PNP high voltage transistors
- 1 - MB352 35 amp bridge rectifier
- 4 - 470 ohm resistors
- 4 - 47k ohm resistors
- 2 - 220pF capacitors
- 4 - J2N5463 P-channel jfets
- 2 - 910 ohm resistors
- 2 - 25k ohm resistors
- 2 - 1.2k ohm resistors
- 4 - 2.2k ohm resistors
- 2 - 10k ohm resistors
- 4 - 680 ohm resistors
- 2 - 1k variable potentiometer
- 2 - 820 ohm resistors
- 4 - 47uF capacitors
- 4 - 4.3k ohm resistors
- 4 - D1N4756A 47 volt zener diode
- 2 - TIP 120 NPN Power transistor
- 2 - TIP 116 PNP Power transistor
- 8 - D1N4754A 35 volt zener diode

- 2 - 10 ohm/5 watt resistors
- 4 - IRF532 N-channel MOSFETs
- 4 - IRF9532 P-channel MOSFETs
- 8 - .22 ohm/5 watt resistors
- 2 - 68nF/100v capacitors
- 2 - 4000uF/100v capacitors
- 2 - 3uH air-core inductors

APPENDIX B

Project Schedule

1990-1991

	Sept	Oct	Nov	Dec	Jan	Feb	Mar	Apr	May
Design									
Power S.	*****								
Diff Pair		*****							
Gain Stg			*****						
Output Stg				*****					
Simulation									
Power S.		*****							
Diff Pair			*****						
Gain Stg				*****					
Output Stg					*****				
All						*****			
Construction									
Order Parts				*****					
Build PS					*****				
Build Board						*****			
Build Chassis							*****		
Mount All								*****	
Testing									
Power S.							*****		
Diff/Gain								*****	
All									*****
Final Eval									****

APPENDIX C

Project Budget

Parts

Resistor/Caps	\$ 20.00
Small Sig Trans.	\$ 20.00
MOSFETs	\$ 25.00
Transformer	\$ 75.00
Chassis	\$ 100.00

Labor

360 hrs - \$15/hr \$ 5400.00

Total **\$ 5640.00**