Targeting SRAM FPGA Components Using a Two-Photon Absorption Laser

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***Abstract*—State-of-the-art SRAM FPGAs (Field Programmable Gate Arrays) are being increasingly considered for use in space applications, due to their reprogrammability and many dedicated resources that implement many common tasks at high speeds. However, the programmable fabric and resources are susceptible to ionizing radiation common in space, causing the device to fail. The radiation effects of all the components need to be known in order to develop effective mitigation techniques. This information, however, is difficult to obtain through typical broad-beam ion testing, due to low observability rates of the components. This paper present the results of a study to use a laser to study the radiation effects on a FPGA. Specifically, three studies were conducted to show the necessity of laser calibration as well as a case study using this calibration to test a specific component on the FPGA. This calibration technique will be used in the future to test many more components on the FPGA.**

I. Introduction

Field Programmable Gate Arrays (FPGAs) are computational devices (much like a CPU or GPU) that are being considered for many space-based applications. However space is a harsh environment, full of many radioactive particles, and like all electronic devices, FPGAs are sensitive to radiation-induced upsets, referred to as Single Event Effects (SEEs). SEEs can cause incorrect-computations, increased power-consumption and may require the device to be reset. Protecting against such upsets is critical before any device can be used in space.

SRAM FPGAs are particularly vulnerable to Single Event Upset (SEU), a type of SEE. An SEU is a change in the state in a memory structure, such as a bit changing from 0 to 1, or vice-versa, 1 to 0. Such changes in the FPGA state, have the potential to change the underlying circuitry implemented on the device. Many techniques have been specifically created to mitigate against SEU.

It is important to understand the SEE response of a device in order to properly mitigate it against radiation effects. This is typically done by observing the response of the device while operating in ion, proton and/or neutron beam. With each new generation of a device, its SEE response can change and this process has to be redone.

Laser testing is an alternative approach that can be used to supplement radiation testing. Using a laser source, charge can be deposited into the active region of the silicon causing a range of SEEs. Because of the localized nature of the laser, specific components of interest can be selected and quickly tested, aiding in the development of mitigation techniques.

It is tempting to assume that quick SEE studies can be accomplished by simply selecting an interesting region on the device for testing and then varying the energy. However, their are many parameters (such as energy depth) and software settings behind the scene that greatly affect where and how much charge is deposited in the device. If not properly taken into account, these parameters could derail the study.

This work constitutes the development of testing methodology for inducing SEEs in an FPGA in a repeatable and reproducible manner using a laser. Three tests were conducted to create this methodology: (1) Moving the laser up and down the z-axis, (2) changing the user-defined pixel size and (3) varying the energy of the laser. These parameters where then adjusted and used to search for and find a known effect at a specific location in the device. This methodology can then be used in future studies to perform other localized studies.

II. Background

State of the art commercial FPGAs contain many dedicated circuits that allow you to implement high-speed, computationally intensive applications. Examples of such circuitry (and descriptions) are:

- Digital Signal Processors (DSP)- Dedicated circuitry that handles common signal processing tasks, such as multiply, add and subtract. The DSP also contains a multiply-accumulate unit or MAC for these operations.
- Multi-Gigabit Transceivers (MGT) - Fast serial communication ports that can operate with speeds in the range of tens of gigabits per second. These can be used to transfer high amounts of data to on-chip resources (such as the DSPs or other computational units) at speeds that are not possible using the normal single ended or differential I/O pins found on the FPGA.
- Block Random Access Memory (BRAM) - Distributed memory allowing high aggregate internal bandwidth on the FPGA chip. These can be used to buffer data for streaming applications, store intermediate results and even act as caches for soft-processors.
- Mixed-Mode Clock Manager (MMCM) and Phase-Locked Loops (PLL)- Clock management units which provide phase-shifting, clock divide/multiply, inversion and dynamic control. The PLL is a subset of the MMCM which offers phase-shifting and clock multiply/divide.
- Dedicated Microprocessors - SoC (System on Chip) devices contain many processing cores providing massive amounts of computational power to interact with custom hardware cores implemented in the programmable fabric of the device.

Such circuitry is hard to specifically test in radiation testing - as it all interacts with each other. Previous studies on the MGTs on the device attributed over half the errors to FPGA configuration cells [1]. This makes it difficult to develop specific mitigation techniques for this circuitry. These circuits could be specifically targeted by the laser for in-depth SEE response study.

There are several advantages to using laser testing. The user has fine-grain control over many of the parameters - including laser energy, depth of the laser (in the silicon), region of the laser (down to a single pulse), among others. This allows the user to perform localized testing of physical components on the chip and to repeatably observe effects that have low cross-sections in radiation beam (e.g. events that rarely occur).

In Two-Photon Absorption (TPA) laser testing [2], two photons are simultaneously absorbed by the silicon to induce a charge in the active region. TPA offers the advantage of backside excitation, which is needed for now common flip-chip packaging. Backside excitation also allows the laser to access the entire active region of the device, not just the areas that are visible through the metal layers when going through the top side of the chip.

There are, however, some known challenges to backside excitation methods. Through the TPA process, the user has control of the depth of the charge placement in the silicon. The energy deposited by the laser is long (in depth) and cylindrical in nature. If the charge is deposited too close to the metal layers, the charge can reflect and diffract off the metal, causing more charge to be deposited than the user intended, and to be deposited in unintended locations. This variable must be taken into careful consideration in order to perform reproducible experiments [3].

III. Experiments

A. Overview

Each of the devices must be carefully prepared before testing can be done. This process involves delidding the chip (removing the package), thinning the substrate and polishing (to smooth the surface of the chip). Polishing is critical as scratches at the micron level can make imaging through the IR camera difficult and can cause uneven distribution of the laser pulse. All of the devices that were used are flip-chip - meaning that the substrate and active region of the chip is accessible through the top of the device. Figure 1 shows the Virtex-5 FPGA (Xilinx XUPV5-LX110T Development System) after this process.

For this experiment, two FPGAs from Xilinx were tested: a Virtex 5 (XC5VLX110T) and a Kintex 7 (XC7K325T). The V5 is fabricated in 65nm CMOS technology and was thinned to $230\mu m$. The K7 is fabricated in $28nm$ HKMG CMOS technology and was thinned to $100\mu m$.

The laser tests were performed using a TPA pulsed laser at the University of Saskatchewan. The laser generates pulses with $1200nm$ wavelength, with a laser pulse frequency of $10kHz$ and the spot size (e.g. size of the laser) is believed to be around $1.2\mu m$, but its actual size is unknown. A 50x lens

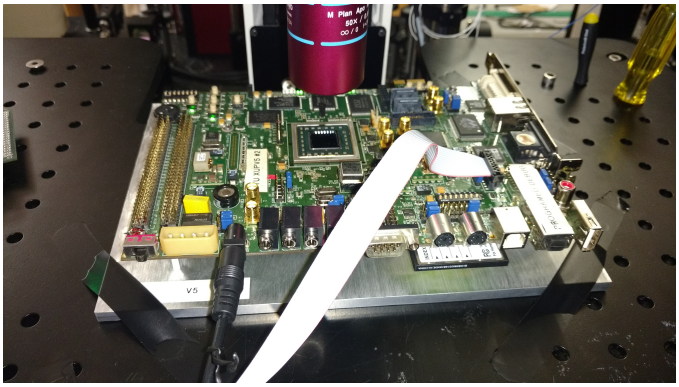

Figure 1. Closeup of the thinned and polished Virtex-5 FPGA in the laser facility at the University of Saskatchewan.

was used for the test to gain a more detailed view of the devices through an IR microscope.

The primary laser mode used during this test is a "Region of Interest" (ROI) in which laser pulses are applied to a predetermined rectangular region. An example of a ROI over the tested V5 FPGA is shown on Figure 2. To conduct an experiment, first a parameter is set, then laser is run and the number of configuration upsets is counted (SEUs in the FPGA configuration memory). All experiments maximize the number of configuration upsets (as this implies that the laser is focused on the active region of the silicon).

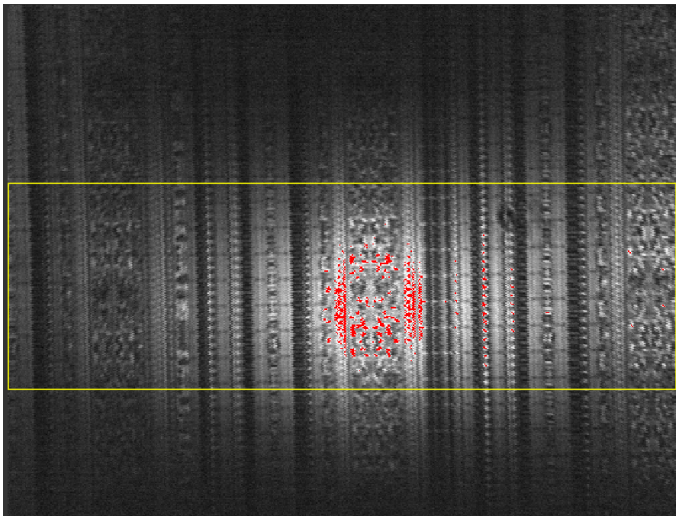

Figure 2. View of V5 metal layers using an IR microscope. The yellow box represents the region of interest (ROI). The ROI can be defined to be any rectangular shape within the field of view and thus can be changed to target any component on the FPGA.

The goal of each experiment is to gain a set of parameters that will aid in conducting experiments that specifically target regions or structures on the FPGA. These parameters will be used to define the functionality of the laser for these and future experiments, such that repeatable and reproducible results can be measured.

B. Z Depth Experiment

The first parameter that was measured was the z-depth (up and down) of the deposited laser charge in the silicon. While the height and width (x and y direction) of the charge deposited by the laser is on the order of 1 μm in length and width, it is also only a few μms in height in the z direction (depth). This implies that if the laser is not focused on the active region in the silicon, laser pulses may not induce SEEs in the circuit. Thus, before any comprehensive study about the chip can be done, the laser must be calibrated to the correct depth.

Using the metal layers as a reference point (z=0), a Z-Depth study can be conducted by slowly increasing z (i.e. focusing the laser above the metal layer) and finding the most sensitive depth i.e., in this case, the z-depth in which the most configuration upsets occur. This is done by adjusting the z-depth by .5 or 1 micron increments and performing a run at that point.

This test was conducted on both the Virtex-5 and Kintex-7 FPGAs and the results are shown in Figures 3 and 4, respectively. As seen in the figures, it appears that the z-depth in sensitive to the process technology size (size of the unit transistor, in this case $65nm$ or $28nm$). Because the Kintex-7 part is more sensitive to the z-depth than the Virtex-5, it will need to be more carefully calibrated.

C. Pixel Size Experiment

The laser software allows for a user-defined grid, where each square is referred to as a pixel. Each pixel will receive exactly one laser pulse. This differs from the laser characteristic, spot size. The spot size refers to the physical dimensions of the laser (width and height). The pixels-size is a software parameter which defines a sub-region within the ROI that will receive one laser pulse. The pixel-size does not have to be the same size as the spot-size. In the ideal case, the entire area of the ROI will receive exposure to the laser exactly once, which is the case when the pixel size and spot size are equal. Because of software limitations, it may be advantageous to set the pixel size as high as possible.

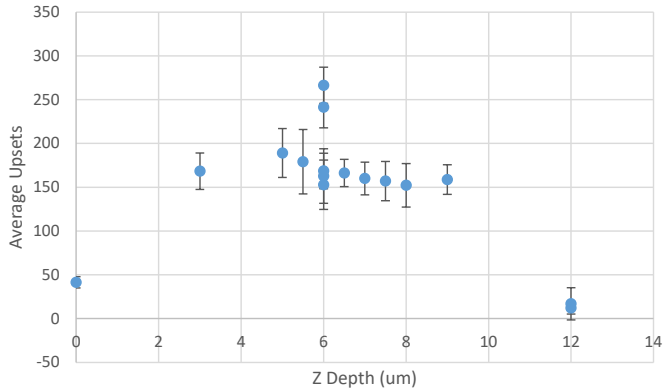

Figure 3. Results of Z-Depth study for Virtex-5 device, for one ROI. For this ROI, the optimal z-depth is between $3\mu m$ and $9\mu m$. The z-depth study would have to be redone for each ROI as the device can have a slight tilt in the setup or could have an uneven surface. ROI Size is $285.96\ \mu m \times 10.15\ \mu m$.

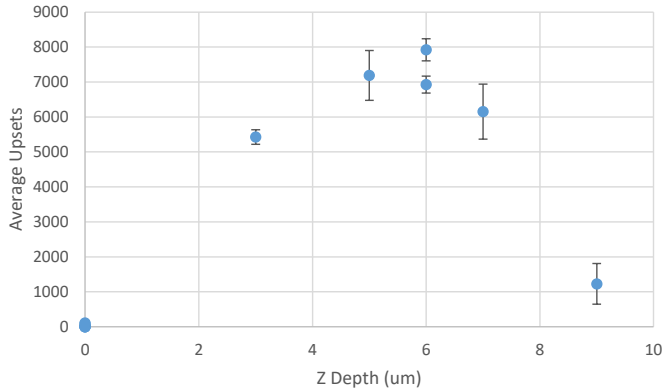

Figure 4. Results of a Z-Depth study on a Kintex-7 device. The best z-depth region is between $4\mu m$ and $6\mu m$ below the bottom-layer metal, over 2x narrower than was seen in the 65nm Virtex-5, possibly implying that smaller feature size makes greater z sensitivity. ROI Size is $61.76\ \mu m \times 285.12\ \mu m$.

As depicted in Figure 5, with optimal size (e.g. pixel size = laser spot size) the ROI receives full coverage. When the pixel size is too big, the are un-hit sections of the ROI (underfill), and when too small (overfill), there are spots that are hit multiple times. The optimal pixel size is needed so that each component on the die can be targeted *exactly* one time.

Overfill causes the problem that the same spot may be hit multiple times, causing a bit to flip (0−>1) and then to flip back (1−>0) causing fewer upsets to be observed. Underfill has the problem that not all of the potential bits in the ROI are exposed to the laser. This becomes more of a problem as the feature size shrinks and it is more likely that there

Table I
PIXEL-SIZE STUDY FOR VIRTEX-5 PART.

Pixel Size	**ROI Area** (μm^2)	**Upsets**	**Upset Density** ($\#upsets/\mu m^2$)
1.5 um	17284	1539.1	.089
2.25 um	17480	1538.7	.088
1 um	4431	172.9	.039
1.286 um	8609	640.5	.074
1.5 um	17243	1525	.088

are structures in the un-hit gap between laser pulses.

This experiment was also conducted on both the Virtex-5 and Kintex-7 FPGAs and the results are shown in Table I and Figure 6. The Virtex-5 was not greatly affected by increasing pixel size (steady upset density), unlike the Kintex-7 which showed a steady drop in number of upsets at the higher pixel sizes, likely due to the smaller feature size ($28nm$ versus $65nm$).

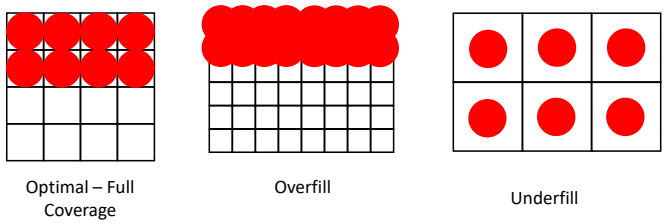

Figure 5. The optimal pixel size (equal to the laser spot size) will fully cover the ROI. In overfill, the pixel size is made smaller than the laser size, leading to regions that are hit multiple times. In underfill, the pixel size is made bigger than the laser spot size, leading to regions of the ROI that are un-hit.

D. Energy Study

An important aspect of radiation testing is the generation of a weibull curve, depicting how the cross-section of the device increases with the energy of the particle (e.g. an SEE is more likely to occur the higher the energy of the particle). Varying the energy of the laser should have a similar effect. Two important aspects to find are the onset energy (the minimum energy needed to induce an SEE) and the saturation energy (the energy at which the number of SEEs that can be induce saturates).

With the correct z depth and pixel size, the onset and saturation energies can be measured. This can be achieved by varying the laser energy over the same ROI and measuring the number of upsets seen. The results for the Virtex-5 and Kintex-7 are shown

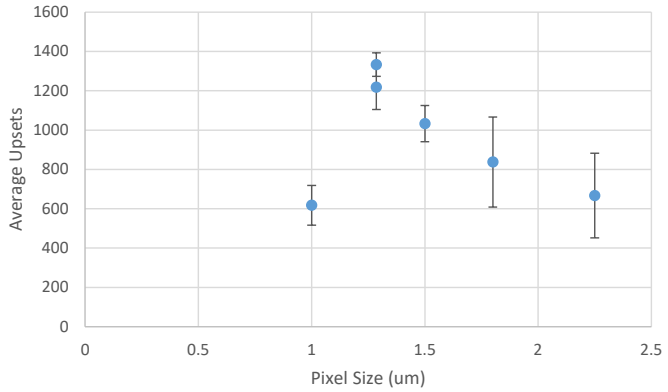

Figure 6. Pixel-Size study for Kintex-7 part. The sharp peak at 1.2 μm shows that the Kintex-7 is much more sensitive to pixel size than the Virtex-5 part. ROI Size is about $61.24\ \mu m \times 61.41\ \mu m$.

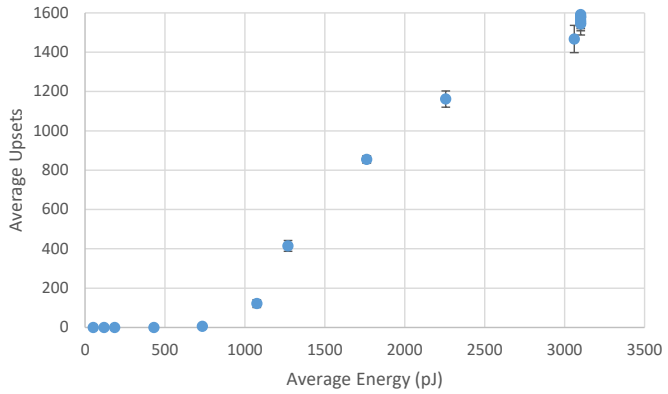

Figure 7. Energy study for Virtex-5 part, showing the onset energy around 1000 pJ and saturation energy around 3500 pJ. ROI Size is $61.2\ \mu m \times 281.76\ \mu m$.

in Figures 7 and 8. There is an ongoing discussion whether the pJ or mV measurement provides the most accuracy, but this does not prohibit the generation of the curves.

Using the information about optimal z-depth, pixel size and knowing the onset and saturation energies, specific components on the FPGA can be targeted for more in-depth studying.

IV. Micro-Latch Site Location

In a previous study, the presence of sites that cause micro-latching was found on 7-Series devices [4]. This causes a problem for space applications, where the electronics cannot sustain an increase in power consumption. This event is observed in the beam, but the actual location and cause is unknown as it has a very small cross-section (suggesting that the size of this events is very, very small. Using the laser, the location and cause can be found through localized targeting.

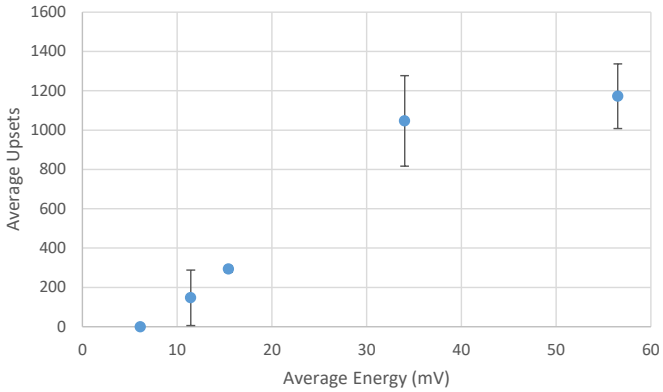

Figure 8. Energy study for Kintex-7 part, showing the onset energy around 9 mV and the saturation energy around 50 mV. ROI Size is $60.72\ \mu m \times 60.72\ \mu m$.

Using the parameters found during the previous study, a comprehensive scan of the chip can be done to find the specific location. This is done by choosing an area to scan, performing the scan with the laser, observing whether the site was activated or not and, if not, move on to the next area. If a latch was activated, then a more in-depth scan of that area can be done.

Once the general location of the micro-latch site is found, it can be located to a specific structure by performing a "binary search"[1]. Such a search is shown in Figures 9, 10 and 11. In Figure 9, the general location of the site has been located. The search is then refined to search half the region and if not found, search the other half as shown in Figure 10. This process is then repeated until the structure is found as shown in Figure 11.

Knowing the specific location has advantages for radiation hardening techniques. Specific mitigation techniques can be developed and then be quickly tested using the laser, avoiding the time and monetary cost associated with radiation testing. The location can then be further investigated in the future.

V. Conclusion

This work constitutes a tudy to use a laser to induce repeatable and reproducible SEEs in SRAM

[1]In Computer Science, a binary search is an algorithm to quickly find an item in a sorted list. The algorithm continually splits the search space in half until the item is found. This method mimics that algorithm.

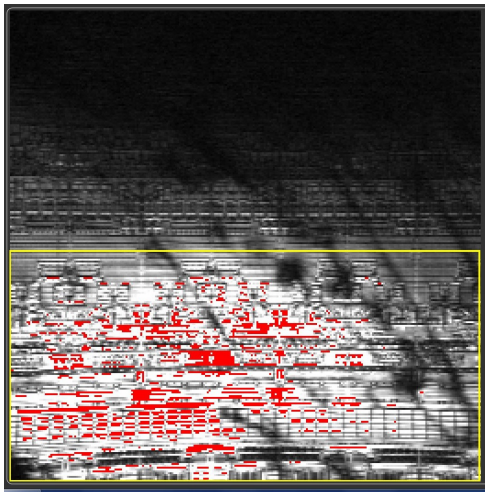

Figure 9. Generalized region of Micro-Latch site on Kintex-7 FPGA.

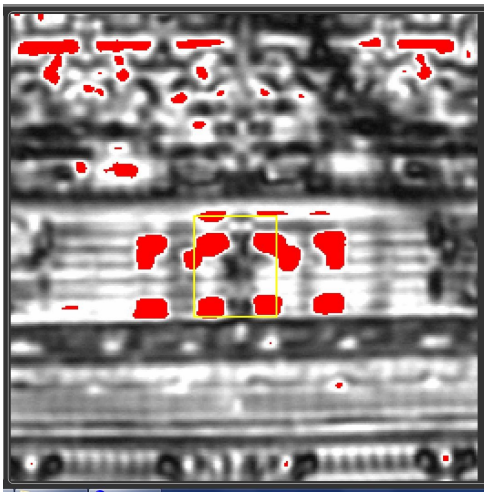

Figure 11. Specific location of the micro-latch site after completing the "binary search".

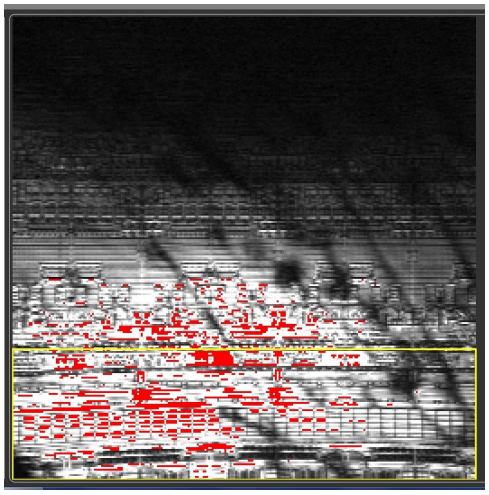

Figure 10. First step of "binary search" to find the specific structure causing the micro-latch in the Kintex-7. The generalized area is cut in half and then each half is tested to refine the location of the site. This process is then repeated until the size of the site is refined to a specified granularity.

FPGAs. While laser testing will not replace broad-beam radiation testing, it can be used to supplement it and to target specific components on the chip, which is much harder to accomplish in a beam. User defined parameters, such as the z-depth, pixel size and energy have the potential to greatly effect the results of any studies that have not been properly calibrated.

Two structures on the FPGA chip have also been targeted for detailed study - a micro-latch site and a handful of configuration cells on the device. The location of the micro-latch site was unknown, but through searching with the laser, the specific location was found, using a "binary search" like method. The configuration cell study provided interesting results and the discovery of a LUT SEFI.

Now that the parameters needed to calibrate the laser is known, laser testing can be used for more detailed study on the specific structures and dedicated circuitry found on the FPGA chip. Such studies would include targeting components, such as the BRAMs, MGTs, DSPs, MMCMs, PLLs, etc. The unique upset modes of each of these components can be studied in detail and mitigation techniques developed. These mitigation techniques can then applied and tested through the laser. Future tests are already being planned to test these components as well as introduce new devices into the laser.

ACKNOWLEDGMENT

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REFERENCES

[1] M. Cannon, M. Wirthlin, A. Camplani, M. Citterio, and C. Meroni, "Evaluating xilinx 7 series gtx transceivers for use in high energy physics experiments through proton irradiation," *IEEE Transactions on Nuclear Science*, vol. 62, no. 6, pp. 2695–2702, Dec 2015.

[2] D. McMorrow, W. T. Lotshaw, J. S. Melinger, S. Buchner, and R. L. Pease, "Subbandgap laser-induced single event effects: carrier generation via two-photon absorption," *IEEE Transactions on Nuclear Science*, vol. 49, no. 6, pp. 3002–3008, Dec 2002.

[3] N. A. Dodds, N. C. Hooten, R. A. Reed, R. D. Schrimpf, J. H. Warner, N. J. H. Roche, D. McMorrow, S. Buchner, S. Jordan, J. A. Pellish, W. G. Bennett, N. J. Gaspard, and M. P. King, "SEL-Sensitive Area Mapping and the Effects of Reflection and Diffraction From Metal Lines on Laser SEE Testing," *IEEE Transactions on Nuclear Science*, vol. 60, no. 4, pp. 2550–2558, Aug 2013.

[4] D. S. Lee, M. Wirthlin, G. Swift, and A. C. Le, "Single-event characterization of the 28 nm xilinx kintex-7 field-programmable gate array under heavy ion irradiation," in *2014 IEEE Radiation Effects Data Workshop (REDW)*, July 2014, pp. 1–5.