A Software Defined Radio AIS for the ZA-002 Satellite

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***Abstract*—ZA-002 is the second South African satellite, and is scheduled to be launched in December 2006. A software defined radio (SDR) automatic identification system (AIS) receiver is proposed as a possible experimental payload for this satellite. The AIS receiver can be used to track and store movement of ships at sea, and then forward this information to the ground station upon request.**

This paper demonstrates the design of a SDR AIS receiver for a satellite. The design of a GMSK/FM modem as used in AIS is presented, followed by simulation results.

1. Introduction

The ZA-002 Pathfinder satellite is the second satellite developed fully in South Africa. The satellite's primary mission is earth observation, and it will be used *inter alia* for disaster management, water resource management agricultural monitoring. Provision has been made for two 1-kg experimental payloads to be included for the secondary mission of the satellite. One possible experimental payload is a software defined radio (SDR) automatic identification system (AIS) receiver.

The primary purpose of the SDR AIS experimental payload is to monitor marine traffic on the South African coastline. The secondary purpose is to carry out a scientific experiment in SDR that will demonstrate the possibility of reconfiguring a radio system on a satellite through software updates, and to serve as a proof-of-concept of SDR for satellite communications systems. Software defined radio is a technology that is currently being researched at Stellenbosch University because of its potential to help realize reconfigurable radio systems and networks, that use the same hardware for different applications [1]. SDR allows reconfigurable radios, and system upgrades can be done through software updates. Generic hardware can then be used for a variety of applications [13].

Traditional analog radios consist of analog components that are subject to factors such as temperature, and their parameters may degrade with time. Because of this potential instability, analog radios may need to be recalibrated often. Digital systems, on the other hand, perform signal processing consistently, are not sensitive to temperature and their performance generally does not degrade with time.

SDR is particularly suitable to space applications, because communications systems on mobile platforms such as satellites can then be maintained and reconfigured using software updates, thus increasing the satellite lifetime. The satellite mission can then be changed by reconfiguring and upgrading the radio through software updates – capability that is not possible with conventional hardware-defined radios. It is from this background that a SDR AIS receiver is designed and implemented for the ZA-002 satellite.

2. ZA-002 Overview

The ZA-002 is a Low Earth Orbit (LEO) satellite with multispectral imaging capability. The main payload on the satellite is a multi-sensor microsatellite imager (MSMI) which will be used to take high-resolution images of the earth. Collected images are downloaded to the ground station using an S-band downlink. Low-bandwidth VHF and UHF channels are used as telemetry, tracking and command links. The satellite is three-axis stabilized, and will be launched into a sun-synchronous orbit at a nominal altitude of 500 km, with a nominal local time (at the equator) of 10:00 AM. The ZA-002 is a 70-kg satellite and the launch is tentatively scheduled for late 2006 or early 2007. The entrance pupil of the imager will normally be pointed at nadir. Two South African based ground stations will be used to download data and command the satellite, one at the Stellenbosch University Electronic Systems Laboratory (ESL), and one at Hartebeeshoek, near Pretoria. The remote sensing capability of the satellite will be used to monitor land, water and vegetation.

3. AIS Functional overview

Automatic Identification (AIS) is a shipboard broadcast system that continuously and autonomously broadcasts a ship's identification, position and other maritime navigational messages [2]. AIS operates in the VHF maritime band and it allows ships to easily track, identify and exchange navigation information between one another or the shore. Each AIS system consists of one VHF transmitter and two VHF Time Division Multiple Access (TDMA) receivers [2]. Time division multiplexing is a method whereby each channel is dedicated to a single line during a specific time slot. TDMA works by assigning multiple users or stations to a single frequency channel. A carrier frequency is assigned to the channel, and digital signals sent out from different stations are transmitted on that frequency in specified time slots in a repetitive frame structure.

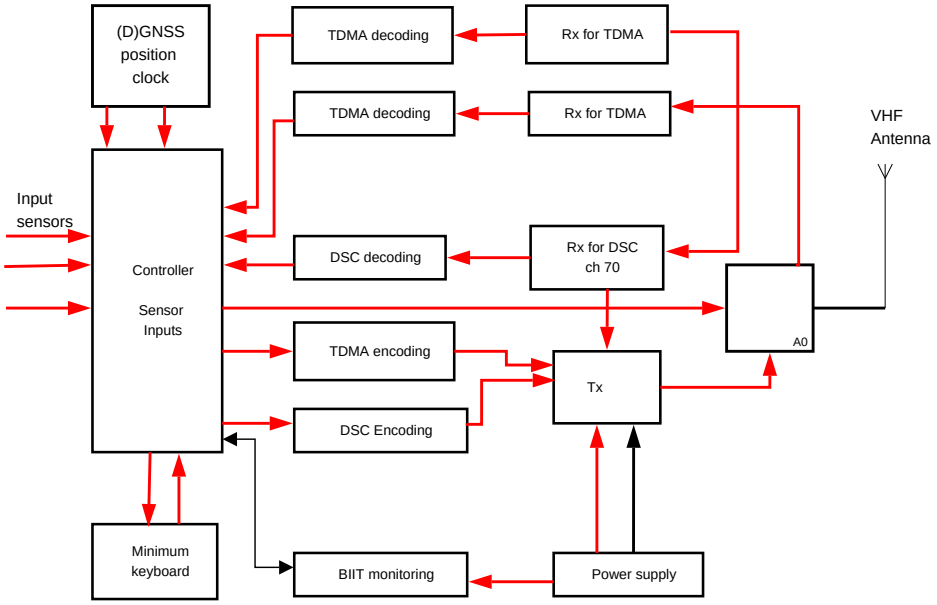

Figure 1: Overview of a ship-borne AIS mobile station.

Figure 1 shows a block diagram of an AIS mobile station. AIS uses 161.975 MHz and 162.025 MHz as carrier frequencies. The AIS receiver should be capable of operating on 25-kHz or 12.5-kHz channels. Bandwidth-adapted frequency-modulated Gaussian-filtered minimum shift keying (GMSK/FM) is used in the AIS physical layer.

A non-return-to-zero inverted (NRZI) waveform is used for data encoding. The NRZI encoded data are then GMSK encoded before frequency modulating the carrier. AIS uses a GMSK bandwidth-time (BT) product of between 0.3 and 0.5.

4. System-Level Design

Figure 2 shows how the satellite will be used to monitor marine traffic. The satellite is equipped with an SDR AIS receiver for ship surveillance purposes. Each ship is fitted with an AIS transponder, and continuously broadcasts AIS information.

AIS uses a bit-oriented protocol for data transfer, which is based on the high-level data link control (HDLC) standard, as specified by ISO/IEC 3309: 1993 – *Definition of packet structure* [4]. Data is transmitted using a transmission packet as shown in Figure 3.

Packets are sent from left to right in the diagram. Data transmission begins with a 24-bit training sequence (the preamble) consisting of one synchronization segment. This segment consists of alternating ones and zeros (0101…) and the sequence can either start with a 1 or a 0 since NRZI encoding is used [4]. The training sequence is used to synchronize the receiver. The start flag is 8 bits long and consists of a standard HDLC flag, marking the start of each transmission packet. The data portion is 168 bits long in the default transmission packet.

The FCS uses a 16-bit cyclic redundancy check (CRC) polynomial to calculate the checksum as defined in ISO/IEC 3309: 1993 [4]. The CRC bits are preset to one (1) at the beginning of the CRC calculation. Only the data portion is included in the checksum calculation. The end flag is 8 bits long and identical to the start flag. The buffer is normally 24 bits long and is used to compensate for bit stuffing distance delays, repeater delay and synchronization jitter. The total length of the normal packet is 256 bits, which is equivalent to one TDMA time slot.

The satellite receives the AIS signals on the VHF uplink. The AIS information is then stored and forwarded to the ground station using either the S-band channel or the UHF downlink provided on the satellite (the S-band channel allows high-speed data transmission). Both downlink channels were developed separately from the project described in this paper, and are not considered further here.

Proposed system

Figure 4 shows an overview of the satellite subsystems used to receive the AIS signals. The on-board computer (OBC) used

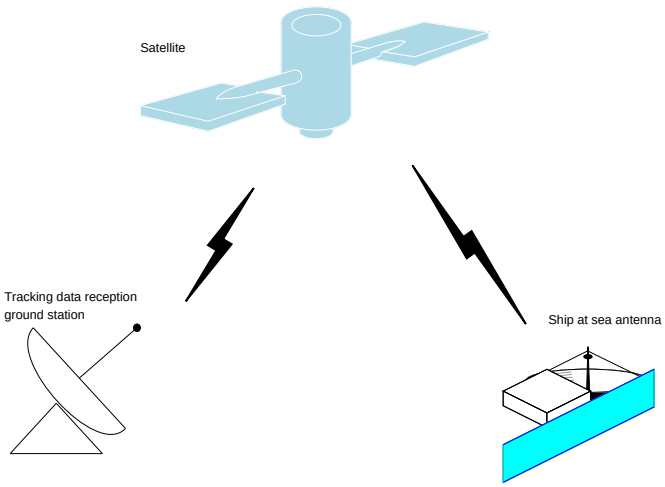

Figure 2: Diagram of the satellite monitoring marine traffic and relaying it to a ground station.

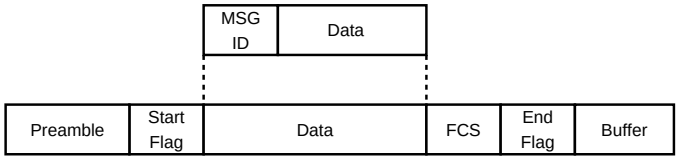

Figure 3: Structure of the AIS data transmission packet [4].

for satellite control is a Sun Space and Information Systems design, and it contains a Hitachi SH4 as primary CPU.

The RF front end consists of the RF amplifier, a mixer for downconversion of the RF signal to the required intermediate frequency (IF), a bandpass filter or lowpass filter to remove the other mixer products and allow only the IF to pass through, and an ADC to digitize the analog IF signal. The digitized IF signal is then routed to the SDR processor. Demodulation, filtering, synchronization and signal recovery are all performed in software by the digital processor.

The next few sections will detail the design of the signal processing software, starting with an overview of the SDR architecture.

5. SDR

Stellenbosch University (SU) has been involved in SDR research since 1998. The university is developing a software architecture for rapid SDR development. The goal is to develop a library of reusable radio building blocks that are portable to many platforms.

A. SDR Functionality

The SU SDR architecture allows the development of a library of components that are used to build a radio system [8]. Figure 5 shows a generic SDR component.

A typical SDR component models a hardware component. The SDR components operate on the principle that all components receive, process and output streams of samples as illustrated in Figure 5, regardless of the number of input and output ports. The exact process function of each component is defined by the type of component being modeled.

B. Component methods

SU SDR components are designed in such a way that they are reusable. Three functions are used in each component to receive, process and dispatch samples between components. These functions are:

- A "read' method that acquires samples from the component's input buffer.
- A virtual "process" function that specifies what process gets performed.
- A "write" method that dispatches samples to the input buffer of the next component.

C. System topology and linking of components

The way in which different modeled components transfer data samples amongst each other depends on the topology used. Since data is streamed on a sample-by-sample basis in the SDR architecture, a control-based topology is employed. In

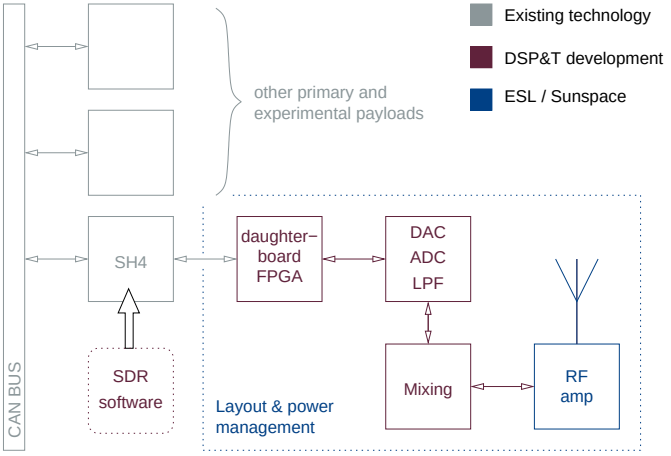

Figure 4: Block diagram of the SDR subsystem on ZA-002.

SDR, each component has its own input buffers and it is the responsibility of a director called a *subcontroller* to monitor the status of each buffer and to schedule processing. The scheduler activates process routines of each component in a round-robin schedule, allowing each component to fully deplete its input buffer [8]. The SDR components are linked by their input and output ports.

D. GMSK modulation

Minimum shift keying (MSK) is a form of continuous-phase frequency shift keying (CPFSK) binary modulation where the modulated carrier has no phase discontinuities, and frequency changes occur at the carrier zero crossings. In MSK modulation, the frequency spacing between the two frequencies transmitted during the FSK is $1/2T_b$, where T_b is the bit interval [19], [20]. This minimum frequency spacing allows the two FSK signal waveforms to be orthogonal to each other and to be correctly detected using a coherent detector. The FSK signal subsequently has phase continuity.

Gaussian minimum shift keying (GMSK) is MSK modulation with a Gaussian premodulation filter [10]. The information bit input or pulse train is passed through the Gaussian LPF, and the output of the filter is MSK modulated. This results in GMSK achieving smooth phase transitions between signal states, thereby reducing the bandwidth requirements. In most cases, the Gaussian pulse is made longer than one bit interval, which results in pulses overlapping, giving rise to intersymbol interference (ISI). The extent of the intersymbol interference is controlled by the product of the Gaussian filter bandwidth and bit duration [5]. The smooth phase transitions of GMSK signals make demodulation at the receiver more complex. For the receiver to achieve a specified bit error rate, more power must be generated at the transmitter in order to overcome the receiver noise in the presence of ISI [14]. GMSK requires more bandwidth than ordinary MSK at the receiver to effectively recover the carrier.

GMSK can be considered to be a combination of frequency and phase modulation, where the phase of the carrier is increased or decreased by $\pi/2$ over a bit period, depending on the data pattern. The rate of phase change is limited by the

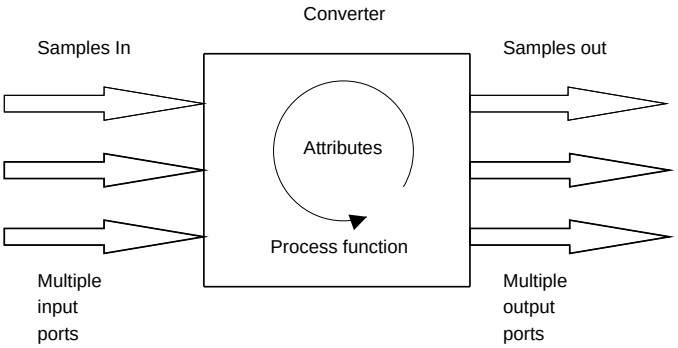

Figure 5: A typical SDR component.

Gaussian filter response. This assists in improving the bandwidth efficiency [14].

E. Detail design

1) Mathematical development

GMSK signals can be generated either by using a quadrature baseband process followed by quadrature phase modulation, or by frequency modulation. The FM technique was used to develop the GMSK modulator in this paper. This method was chosen because it is simple to implement using direct digital synthesis (DDS), and the demodulation process can be implemented using a simple FM discriminator.

The GMSK modulator was implemented by first differentially encoding the data, representing it as a non-return-to-zero inverted (NRZI) signal and then passing it through a Gaussian low-pass filter. The signal is then frequency modulated using a DDS system. Each NRZI symbol consists of eight samples. The Gaussian filtered signal was then resampled to the carrier sampling frequency, before frequency modulating the carrier.

The GMSK modem was designed to provide the GMSK signal to be demodulated by the proposed GMSK demodulator. The block diagram of the GMSK modulator is shown in Figure 7.

The first step in the modulator is the differential encoder. The differential encoder calculates an exclusive-NOR between the incoming bit and the reference bit, and outputs the differentially encoded bit.

The Gaussian filter component is designed using the coefficients of the Gaussian filter for a given bandwidth-time product. A Gaussian-shaped impulse response filter produces a signal with low side lobes and narrower main lobe than the rectangular pulse [18]. Figure 6 shows Gaussian filters with BT = 0.3 and 0.5.

The impulse response of the Gaussian LPF is given by [5]:

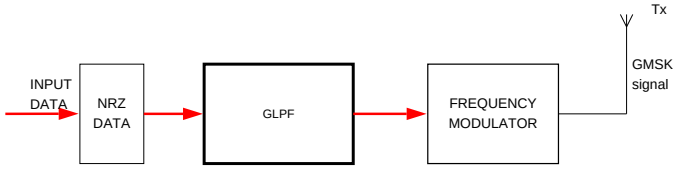

Figure 7: Block diagram of a GMSK modulator.

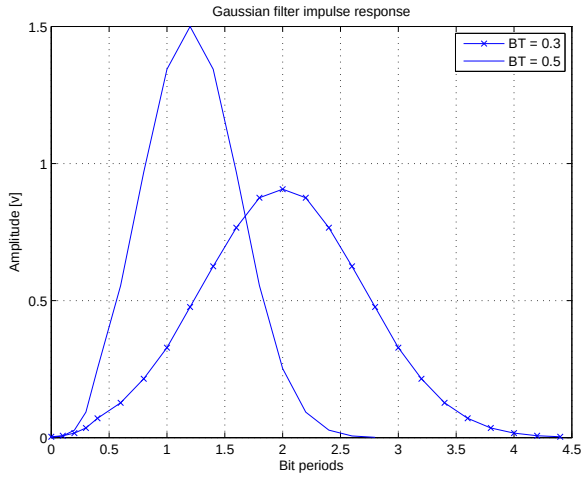

Figure 6: Gaussian filter impulse responses with BT products of 0.5 and 0.3 respectively.

$$h(t) = \frac{1}{\sqrt{2}\,\pi\,\sigma\,T} \exp\left(\frac{-t^2}{2\,\sigma^2\,T^2}\right), \tag{1}$$

where

$$\sigma = \frac{\sqrt{\ln(2)}}{2\,\pi\,BT} \tag{2}$$

and B is the 3-dB bandwidth of the filter and T is the symbol period.

The response of the Gaussian LPF to the square pulses is equivalent to convolving the filter with the square pulses and is given by:

$$g(t) = h(t) * \Pi\left(\frac{t}{T}\right). \tag{3}$$

The pulse response $g(t)$ (which is equivalent to multiplying the Fourier Transform of $h(t)$ and the Fourier Transform of $\Pi(t/T)$, can be written as:

$$g(t) = \frac{1}{2\mathrm{T}} Q\left(2\,\pi\,BT\,\frac{t - T/2}{T\sqrt{\ln(2)}}\right) - Q\left(2\,\pi\,BT\,\frac{t + T/2}{T\sqrt{\ln(2)}}\right), \tag{4}$$

where $Q(t)$ is the function

$$Q(t) = \int_t^{\infty} \frac{\exp\left(-y^2/2\right)}{\sqrt{2\,\pi}}\,dy\,. \tag{5}$$

The GMSK signal is given by:

$$s(t) = \sqrt{2\,E\,T_b}\cos\left(2\,\pi\,f_c t + \theta + \theta_0\right), \tag{6}$$

where θ_0 is the initial phase at $t = 0$.

The Gaussian filter component takes each sample from the differential encoder and filters it using the Gaussian filter coefficients. The frequency modulator component then takes the incoming Gaussian-filtered samples and frequency modulates the carrier frequency using the direct digital synthesis technique. This technique is discussed next.

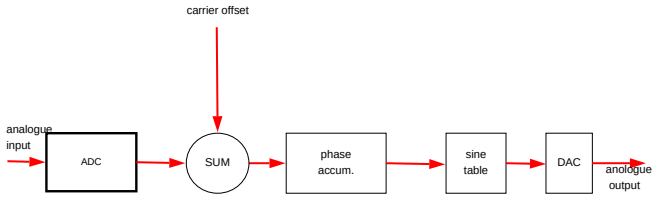

Figure 8: Block diagram of a DDS system.

2) Direct Digital Synthesis

Direct digital synthesis (DDS) is used to digitally synthesize a desired analog signal, usually a sine wave of which the frequency must be variable. DDS uses a fixed sampling frequency, and different output frequencies are obtained by sampling a sine wave using variable phase increments. If a higher frequency is desired, the sine wave is sampled at larger phase increments [15]. Figure 8 shows a block diagram of a DDS system.

The heart of the DDS system shown in Figure 8 is the phase accumulator. The value in the accumulator represents the current phase ($0 \le \phi \le 2\pi$) of the output signal wave. Every clock cycle, the phase of the accumulator is incremented by $\Delta\phi$. The size of this increment is directly proportional to the output frequency. Phase wrap from 2π to 0 radians is achieved by simply ignoring the phase accumulator overflow. The phase value in the accumulator can then be matched to a value in the sine or cosine lookup table, thus producing a sampled sine wave. The resulting sampled sine wave can be reconstructed to produce a desired output sine wave.

[7] shows that an output frequency of f_0 can be produced if the phase increment is:

$$\Delta\phi = 2\pi\left(\frac{f_0}{f_s}\right) \text{ radians.} \tag{7}$$

By dynamically changing the phase increment, it is possible to implement different modulation schemes.

The instantaneous phase of an analogue frequency modulated signal is given by:

$$\theta(t) = \omega_c t + k_f \int_0^t m(\tau)\, d\tau + \theta_0\ , \tag{8}$$

where ω_C is the carrier frequency in radians, k_f is the frequency deviation constant, $m(t)$ is the modulating signal, and θ_0 is the initial phase angle at $t = 0$.

To perform the frequency modulation (FM) in discrete form using DDS, the instantaneous phase of the FM signal can be calculated to be:

$$\theta(nT) = nTF_c + k_f T \sum_{k=1}^{n} m(kT) + \theta_0\ , \tag{9}$$

where T is the sampling interval, n is the sample number, F_C is the constant that determines the carrier frequency of the discrete-time output signal, and θ_0 is the initial phase in radians. Sampling must be performed below the half Nyquist frequency.

The DDS FM modulator can synthesize an FM signal directly at the desired broadcast frequency or at an intermediate frequency which can then be up-mixed to a desired broadcast frequency.

3) GMSK demodulator

The GMSK demodulator uses an FM discriminator. The ideal FM discriminator consists of a differentiator and a low-pass filter and a decision device.

Since GMSK is a special form of FM, the message is contained in the instantaneous frequency of the modulated signal. The demodulation process is performed as follows [16]: Let

$$x(t) = A_c \cos\left[\omega_c t + k_f \int_0^t m(\tau)\, d\tau\right], \tag{10}$$

be the GMSK signal, with k_f equal to $2\pi f_d$, where f_d is the frequency deviation. The differentiated signal is given by:

$$\begin{aligned} e(t) = &-A_c\left[2\pi f_c + 2\pi f_d m(t)\right]\cdot \\ &\sin\left[2\pi f_c t + 2\pi f_d \int_0^t m(\tau)\, d\tau\right]. \end{aligned} \tag{11}$$

Rectifying the differentiated signal and lowpass filtering results in:

$$\begin{aligned} y(t) &= \left|A_c\left[\omega_c t + k_f m(t)\right]\right| \\ &= A_c\left[\omega_c + k_f m(t)\right]. \end{aligned} \tag{12}$$

Removing the DC component yields

$$y(t) = A_c k_f m(t). \tag{13}$$

However, in the presence of additive Gaussian noise, the carrier amplitude variations cause distortion at the output of the discriminator. The receiver uses a bandpass filter to remove the out-of-band interference.

After successfully demodulating the modulated carrier, the receiver must have an accurate knowledge of the beginning of the symbol and the end of the symbol. This is necessary for the receiver to make correct symbol decisions [9]. If the receiver integrates over an interval of inappropriate length, the ability to make accurate symbol decisions will be degraded. The early-late gate is the method chosen to achieve symbol synchronization in this implementation.

The generic early-late gate synchronizer operates by performing two separate integrations of the incoming signal energy over two different ($T - d$) portions of the symbol interval, where T is the symbol interval and $d = T/2$ [9]. For the AIS demodulator the symbol synchronizer was modified by performing three separate integrations instead of two. This was done in order to use the same synchronizer when demodulating M-ary pulse amplitude modulated (PAM) signals, resulting in a more widely reusable component. Figure 9 shows a block diagram of the early-late gate symbol synchronizer.

The first integration, I_1, (the early interval) starts the integration at the loop's estimation of the beginning of a symbol period (the nominal time zero) and integrates to $T/3$, where T is the nominal symbol period. The second integral, I_2, (the central interval) delays the start of its integration for $T/3$ seconds, and then integrates to $2T/3$. The last integral, I_3, (the late interval) delays the start of its integration for $2T/3$ seconds,

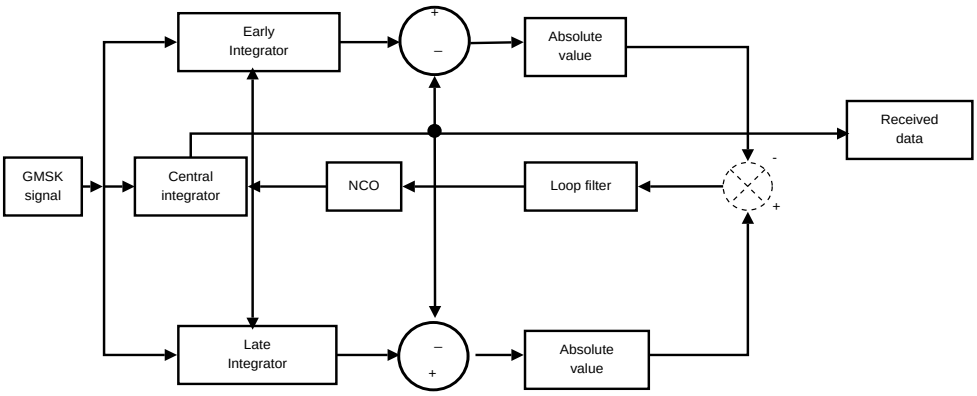

Figure 9: Block diagram of an early-late gate symbol synchronizer.

and then integrates to the end of the symbol period (the nominal time T).

The measure of the receiver's symbol timing error is now given by

$$\epsilon = \left| I_2 - I_1 \right| - \left| I_2 - I_3 \right| \tag{14}$$

which can be fed back to the loop's timing reference to correct loop timing. When the synchronizer is achieves lock, all the integrators will accumulate the same signal energy, and $\epsilon \approx 0$. Thus, when this device is synchronized, it is stable and there is no tendency to drive itself away from synchronization [9].

4) Software Design of the GMSK demodulator

Figure 10 shows a block diagram of the SDR GMSK discriminator. The modulated signal is passed through a bandpass filter with sufficient bandwidth to let through the lower and upper sidebands and to remove out-of-band interference.

The first step in the GMSK demodulation process is differentiation. Note that differentiation in the continuous-time domain can be approximated in the digital domain by calculating

$$\frac{d}{dt} x(t) \approx \frac{x[nT] - x[(n-1)T]}{T}, \tag{15}$$

where $x(t)$ is the continuous modulated signal, T is the sampling period and n is a positive integer representing the sample index. The original message signal is proportional to the phase difference of the consecutive data samples. The differentiator computes a new phase difference vector for each new sample.

The differentiated signal is then passed through the rectifier component. The rectification process is accomplished in software by taking the absolute value of the differentiated signal. The resulting signal is then divided by $2A/\pi$ (where A is the carrier amplitude) which are the coefficients for full-rectified sine wave.

The rectified signal is lowpass filtered using an 8th order butterworth low pass filter with a cutoff frequency slightly higher than half of the symbol frequency. A filter with a high cutoff frequency is desired to avoid introducing intersymbol interference at the receiver. The DC component is removed by subtracting the $2\pi f_c$ from (12). The baseband signal is recovered as follows:

$$\begin{aligned} y(t) &= A_c \left\{ \omega_c + 2\pi f_d m(t) \right\} - A_c \omega_c \\ &= A_c 2\pi f_d m(t) \end{aligned} \tag{16}$$

and then dividing by the frequency deviation term to recover the baseband signal:

$$\begin{aligned} y(t) &= \frac{\{ A_c 2\pi f_d m(t) \}}{\{ 2\pi f_d \}} \\ &= A_c m(t). \end{aligned} \tag{17}$$

The demodulated signal is then passed through the early-late gate synchronizer for bit synchronization, as described in the previous section. The central integration result, I_2, is used to decide whether the symbol represents a 1 or a 0.

The recovered symbols are finally passed through the differential decoder component. The decoding process is performed by comparing the received symbol and its delayed symbol version, to reverse the encoding process, thus recovering the transmitted symbols.

6. Physical-Layer Simulation

In this section the performance of the proposed GMSK modem is evaluated, first in ideal noise-free conditions, then in the presence of additive white gaussian noise (AWGN). The GMSK modem was simulated using Matlab. The simulation was performed using a data rate of 9600 b/s, a carrier frequency of 100 kHz, frequency deviation of 12.5 kHz, a carrier sampling frequency of 1 536 000 samples/s, and both $BT = 0.5$ and $BT = 0.3$. An input frame length of 1 000 bits was used in the bit error rate (BER) performance simulation.

Figure 11 shows the Gaussian-filtered bits. Because the information bits are sampled at 76800 samples/s and the

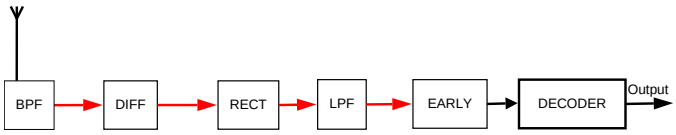

Figure 10: Block diagram of the SDR GMSK demodulator.

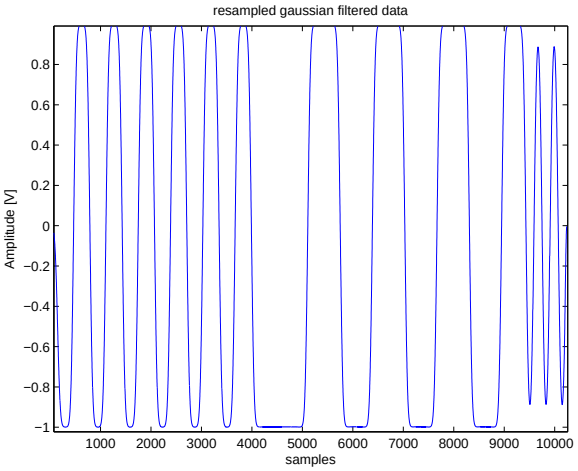

Figure 11: Resampled Gaussian-filtered data. A Gaussian filter with BT = 0.5 was used in this experiment.

carrier frequency is sampled at 1536000 samples/s, the Gaussian-filtered bit stream must be upsampled to the carrier frequency's sampling frequency.

Figure 13 and Figure 15 show the differentiated and rectified signals respectively. The results show the message signal contained in the envelope of both the differentiated and rectified signal. The DC component at 6.2832e5 corresponds with to carrier frequency ω_c in radians per second.

In Figure 12 the low-pass filter has removed the high-frequency components of the original modulated signal. The recovered baseband signal still contains an unwanted DC component proportional to the carrier frequency.

Figure 14 shows the low-pass filtered signal after passing through the early-late gate symbol synchronizer. We see that at the beginning, synchronization has not yet been achieved, and this is indicated by diamonds displayed on the graph. As the synchronizer continues to feed back the symbol timing error to the loop's timing reference to correct loop timing as in (14), there comes a time when all the integrators accumulate the same amount of signal energy, and $\epsilon \approx 0$. When this happens,

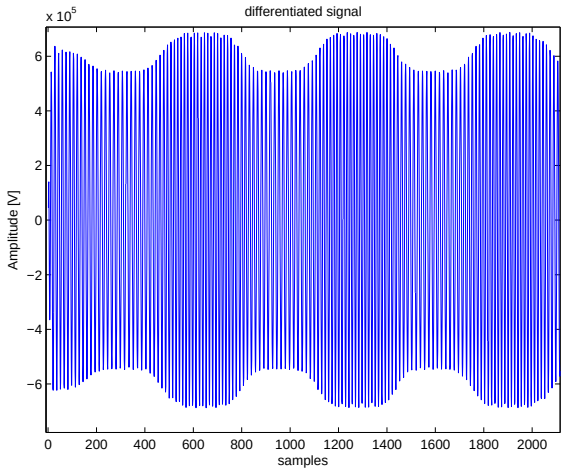

Figure 13: The differentiated FM signal.

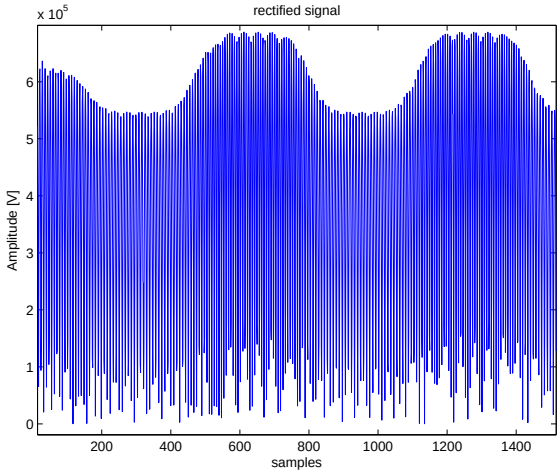

Figure 15: After differentiation, the received FM signal is rectified in order to extract its envelope.

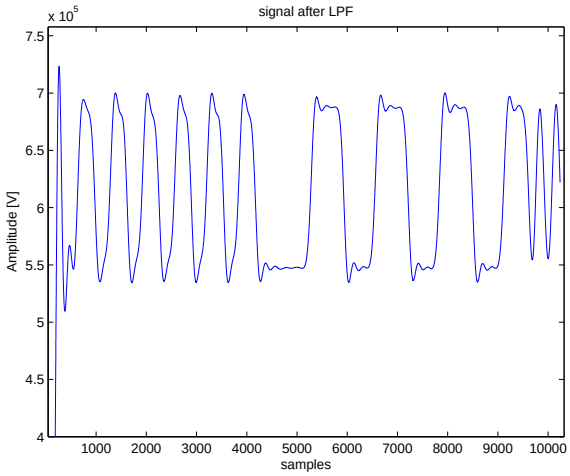

Figure 12: The rectified FM signal after lowpass filtering. The modulating signal has now been recovered.

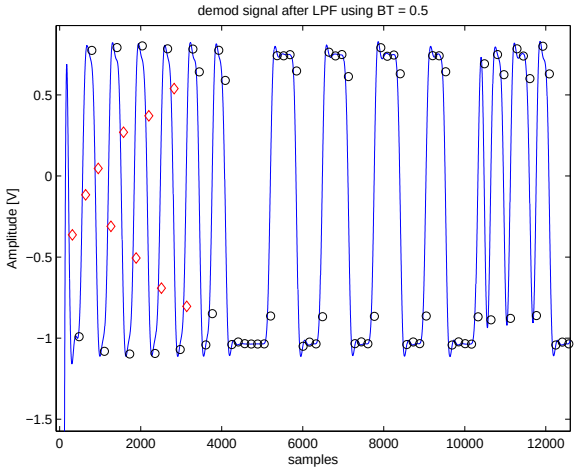

Figure 14: The demodulated GMSK signal after symbol synchronization.

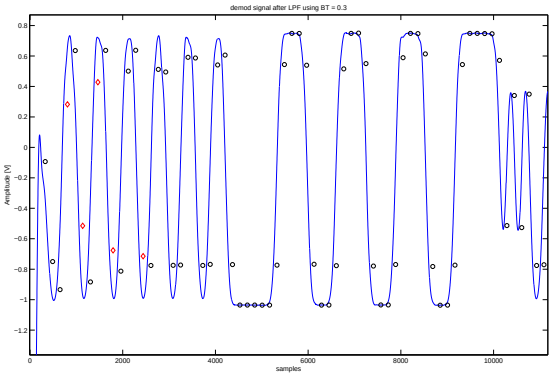

Figure 16: Demodulated signal after symbol synchronization using BT = 0.3.

the synchronizer displays circles on the graph to show that synchronization is achieved.

The simulation was performed using the 24-bit training sequence specified for AIS, an 8-bit start flag, and then randomly generated bits representing the message signal. The results shows the training sequence of alternating ones and zeros, followed by start bits and then the message data.
Figure 16 shows the demodulated signal when BT = 0.3 is used. The effect of the intersymbol-interference is displayed on the demodulated signal.

Figure 17 and Figure 18 shows the rectified signal and the recovered signal after early-late gate synchronizer in the presence of additive Gaussian noise. The degradation of the signal by the noise is evident in the rectified signal. This is shown by the amplitude variations of the rectified signal. This results in errors being introduced in the recovered bits.

Figure 19 shows the power density spectrum of the GMSK signal with frequency deviation of 12.5 kHz and BT = 0.5. The spectrum in Figure 19 was generated by windowing the GMSK signal by the Hamming window. The results show that the Gaussian filter helps to prevent the GMSK signal power from spilling into adjacent channels. The spectrum has lower side-lobes outside of the 25-kHz bandwidth, about 30dB below the

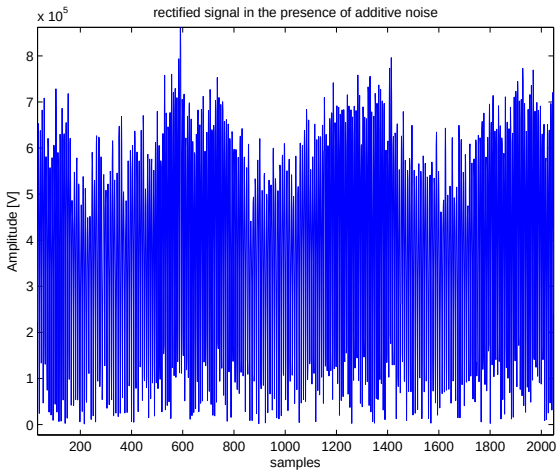

Figure 17: The rectified signal with AWGN at 10 dB SNR.

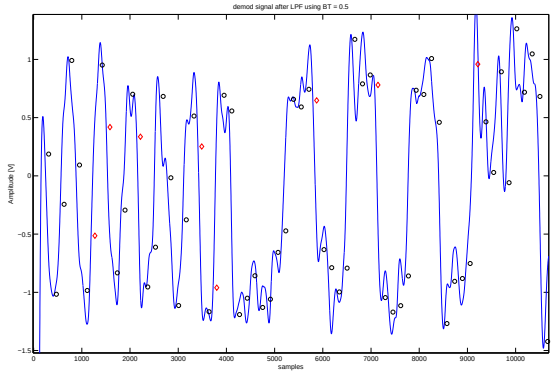

Figure 18: Demodulated baseband signal after symbol synchronization in the presence of AWGN.

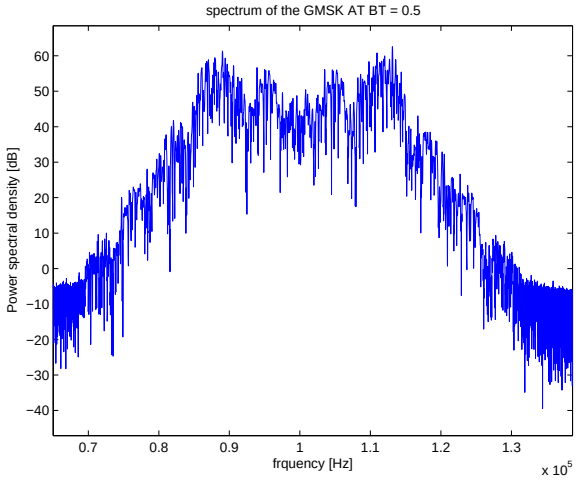

Figure 19: Frequency spectrum of a GMSK signal with a frequency deviation of 12.5 kHz and BT = 0.5.

main lobe. The maximum permissible adjacent-channel interference limit for radio transmissions is -60 dB [12]. According to [12], both GSM and Digital European Cordless Telephone (DECT) may not meet the recommended value of -60 dB, and for DECT, adjacent-channel interference of only -40 dB can be guaranteed.

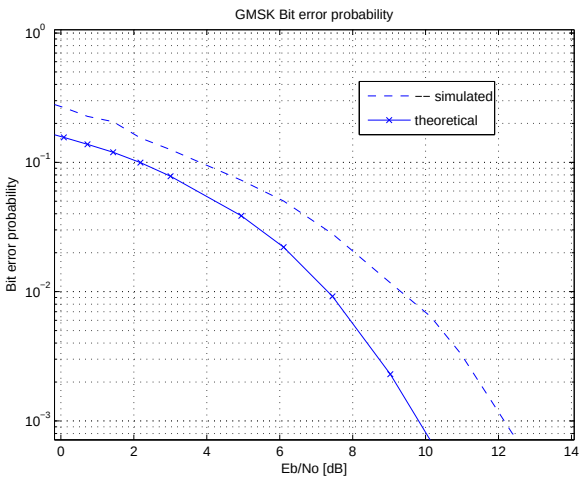

Figure 20: Bit error probability curve for GMSK.

Figure 20 shows the bit error probability performance of the discriminator receiver for GMSK in the presence of additive Gaussian noise using BT = 0.5. The simulated results differ from the theoretical results by about 2.5 dB.

7. Link Budget

A link budget for the uplink was calculated to verify that it is possible for a LEO satellite to reliably receive AIS transmissions. An AIS antenna height of 20 m was assumed. The transmission power of the AIS station is 12.5 kW at maximum. A 600 km orbit is used to compute the slant range of 2328 km with 5 degrees minimum ground station elevation [17]. Table 1 gives the link budget.

Table 1 Link budget, uplink performance

Item	*Symbol*	*Value*	*Unit*
Frequency	f	161.975	MHz
Transmitter power 12.5W	P_t	10.97	dB
Bit rate	R	9600	bps
Transmit Antenna Gain	G_t	5	dBi
Minimum elevation	$\in$	5	deg
Transmitter Line loss	L_t	-1.0	dB
Effective isotropic radiated power	EIRP	14.97	dB
Propagation path length	S	2328	km
Space path loss	Ls	143.9	dB
Satellite Rx Antenna Gain	G_r	-6.0	dBi
Receiver noise figure	F	6.0	dB
Receiver noise temperature	T_r	1000	K
Receiver IF bandwidth	B	20	kHz
Noise spectral density	N_O	-198.6	dBW/Hz
Minimum required RX SNR	SNR	10	dB
Other Losses	L_O	6	dB
Received signal power	P_r	-110.9	dBm
Received signal to noise ratio	SNR_r	14.69	dB
Link margin	***M***	**4.69**	**dB**

The link budget results shows a link margin of 4.69 dB, which is more than sufficient to receive the AIS signals on the satellite from ships at sea. The link budget was computed for the worst-case scenario.

8. Further Work on the SDR Implementation

Further development of the GMSK demodulator is scheduled to be implemented in SDR environment as from May 2006. The GMSK modulator and demodulator must be implemented using the C++ programming language. To verify the design, actual AIS signals will be transmitted and then demodulated using the software defined radio AIS receiver. An AIMSmIV AIS mobile station from Marine Data Solutions was acquired and will be used to transmit reference AIS signals.

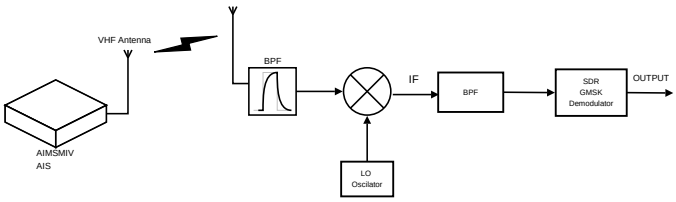

Figure 21: Block diagram of the experimental implementation of the SDR GMSK demodulator.

The proposed SDR implementation is shown in Figure 21.

9. Conclusions

In this paper we have presented the design and simulation of the proposed SDR GMSK modulator and demodulator, which is used in AIS. The GMSK demodulator is proposed to be used on the ZA-002 satellite to monitor maritime AIS signals. The GMSK demodulator was implemented as a software-defined radio, which allowed us to test much of its functionality by simulation. The simulation results showed that both the differentiation and rectification processes can successfully be performed in the digital domain by calculating a backward difference, and by taking the absolute value of the signal. The early late gate synchronizer performed as expected and achieved symbol synchronization on the demodulated signal within the training sequence of a received AIS signal.

In the presence of AWGN, the bit error probability performance of the GMSK discriminator showed 2.5 dB loss compared to theoretical results. The link budget for the uplink was calculated and a link margin of 4.69 dB was obtained, which demonstrated that sufficient AIS signal power will be received at the satellite's altitude.

There are several advantages to the demodulation taking place in the digital domain. First, the modulation scheme can be updated as new software techniques become available. It also means that there is a possibility for a radio system on mobile platforms such as satellites to be reconfigured to entirely new applications. This demonstrates the concept that it is possible to change the satellite mission completely while the satellite is already in orbit by performing a simple software update. The disadvantage may be the speed of processing that is needed in processing signals, especially at high intermediate frequencies, due to the limited sampling frequency of the ADCs.

The GMSK modem presented here is scheduled to be implemented on the SDR environment of the University of Stellenbosch, which will allow hardware tests to be performed. The actual AIS signals will be transmitted and then be demodulated by the proposed SDR demodulator.

Acknowledgments

The research in this paper was partially sponsored by Sun Space and Information Systems, and its submission was made possible by Prof. Jan du Plessis of the same company. The author wishes to extend his thanks to Marine Data Solutions for assisting with the AIS equipment for testing.

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