A 10-bit SAR ADC with an ultra-low power supply

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***Abstract* — This paper presents a successive approximation analog-to-digital converter (SAR ADC) design, which operates with a 0.2 V power supply. The design utilizes a dynamic bulk biasing scheme to dynamically adjust the relative NMOS and PMOS strengths, which are very sensitive to temperature, process, and mismatch variations at low supply voltages. The design achieves a very low power consumption due to the 0.2 V supply. Several circuits in the design are optimized for full functionality at 0.2 V. Extracted simulations show a total power consumption of 9 nW with a peak SNDR of 61.3 dB and a Walden Figure of Merit of 1.91 fJ/conversion-step.**

Keywords—SAR ADC, low-power, low-voltage, bulk-biasing, wireless sensor networks

I. Introduction

A. Wireless Sensor Networks in Space-Based Applications

There is an ever-increasing need for wireless sensor networks in different environments. Wireless sensor networks are spatially distributed autonomous sensors that monitor different physical and environmental conditions, such as temperature, sound, and air quality [1]. They cooperatively gather data and then pass the data through a network to a main location to be processed and analyzed. These sensor networks have been successfully used in health care [2], environmental sensing [3], and military applications including surveillance and reconnaissance [4]. They provide a flexible, cost-efficient alternative to traditional remote monitoring. Instead of manufacturing one large sensor, engineers have been able to create many small, cost-efficient sensors called "nodes" to work together and perform the same function. Wireless sensor networks are composed of these individual sensing nodes that are each made up of one or more microcontrollers, an energy source, a radio transceiver, and electronic circuits interfacing with the sensors and microcontrollers. They are actively being studied for many applications, including use in space exploration.

Wireless sensor networks provide an attractive option for use in space exploration because of their flexibility and low cost of operation. In space, wireless sensor networks could be used for a variety of functions such as: weather monitoring missions in low earth orbit (Figure 1) and missions where the networks are deployed on a planet to monitor the surface conditions. Several space-based applications are currently being researched. Wireless sensor networks could be deployed around a spacecraft on a planet to aid in ground measurements [5]. They could be used on the outside of a spacecraft to check and report hull integrity [6]. Furthermore, they could be distributed in a planetary atmosphere to collect data about the atmospheric conditions [7].

In order to function effectively in space-based applications, wireless sensor networks need to be able to operate while consuming very low power [8]. Traditional wireless sensor network nodes will need to be modified in order to meet the power requirements of operating in space. One of the most important requirements for the individual sensing nodes is that each consumes as little power as possible. It is critical to the success of wireless sensor network space applications that the networks operate for as long as possible with a given amount of battery power.

B. ADCs in Wireless Sensor Networks

In order to properly digitize signals from the sensor node's environment, each node must contain an Analog-to-Digital Converter (ADC). The ADC takes in an analog input and outputs a digital code that best represents the analog input. This digital data can then

be transmitted to a network center, where it can be analyzed and manipulated. Obviously, the stringent power requirements placed on the sensing nodes extend to the ADC. The ADC must consume extremely low power (<10nW) and have a sample rate of 1-5kHz to properly function. We propose a 10-bit ADC that can operate according to these requirements due to an unprecedented lowering in power supply voltage. This 10-bit ADC can operate at 5kHz, which is fast enough for wireless sensing node applications.

Figure 1. An artist's rendering of a wireless sensor network in space monitoring Earth's atmosphere. [7]

II. ADC Design

For our ADC design, we chose to build a Successive Approximation Register (SAR) ADC. The SAR architecture was chosen due to its simplicity and inherent low power consumption. Its basic operation is described in the subsequent section

A. General SAR ADC Architecture

The SAR ADC realizes a binary search algorithm to obtain the digital code that best matches an analog input. An example for a 3-bit SAR ADC is shown in Figure 2, where an analog input voltage (V_{in}) is converted to an output code. In the first step, the unknown V_{in} is compared to a reference (V_{ref}) that is initially set to the middle of the ADC range, which is 0 V in this example. As shown in the figure, $V_{in} < V_{ref}$, so the first bit is a 0, and the reference is now changed to the middle of the remaining search range. Since we know that V_{in} is between -1 and 0 V, the new reference is thus set to -0.5 V. In the next cycle, $V_{in} > V_{ref}$, so the second bit becomes 1; and, therefore, the reference voltage is now updated to -0.25 V, which again is the middle value of the remaining search range. The third comparison resolves the third and final bit, which is 0, causing the final digital code to be 010.

The circuitry to implement this algorithm requires three main parts. The first is a digital-to-analog converter (DAC) is necessary to produce the reference voltage V_{ref} that is updated depending on the previous bit decisions. Second, a comparator is required to compare V_{in} to V_{ref}. Finally, logic is needed to time the various operations and to store the attained digital code. Additionally, a sample and hold switch is also required to sample the analog input voltage before holding the value and performing the binary search method. Figure 3 shows a block diagram of a SAR ADC. In this case, rather than comparing V_{in} against V_{ref}, V_{ref} is subtracted from V_{in} first, and the comparator simply determines the sign of $V_{in} - V_{ref}$, which is identical to comparing V_{in} against V_{ref}. Typically, the sample and hold is nothing more than a set of switches, and the DAC is composed of a switched-capacitor network, which leads to a straightforward hardware implementation.

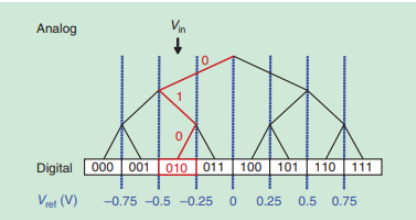

Figure 2. A binary search tree of a 3-bit SAR ADC. [9]

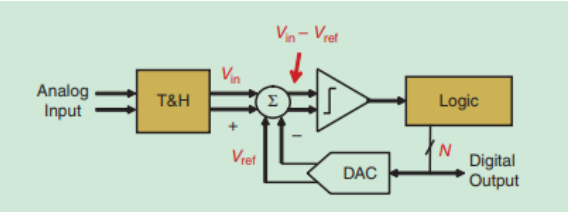

Figure 3. A block diagram of a differential SAR ADC. [9]

B. Proposed SAR ADC Architecture

We chose to design a 10-bit ADC, which provides high accuracy. When the ADC resolution goes beyond 10 bits, the switched-capacitive DAC tends to be limited by capacitor mismatch and has to be sized larger, thus degrading power efficiency. The ADC design is differential, to combat power supply noise. It consists of double bootstrapped sample and hold switches, a switch-capacitor DAC, a dynamic, two-stage comparator, and digital logic. Our SAR

ADC is asynchronous, meaning that it internally generates all required clock signals to operate and only needs a sampling clock input.

C. Lowering the Power Supply Voltage

Many previous designs have taken advantage of the simplicity of the SAR ADC and have successfully used a reduced power supply voltage in an effort to conserve more power. [9-13] The lowest supply voltage these designs have used is 0.3 V. In order to reduce power consumption even further, our design uses a power supply of 0.2 V, which is unprecedented, especially considering that the nominal supply voltage for the process we use is 1.8 V. The following section details the challenges of a 0.2 V design.

III. 0.2 V Design Challenges

A. Noise

Previous results have shown great success in scaling the supply voltage down to 0.4 V [17], 0.3 V [13], and even 0.2 V in one case [21]. In scaling down the supply voltage, noise becomes more of an issue. This is because the single-ended input voltage is typically limited to the supply voltage, which reduces the value of the LSB voltage in the ADC. If the LSB value is smaller, the noise performance of the ADC must be much better in order to detect changes as small as an LSB voltage. This LSB voltage can be calculated in a differential ADC using the formula:

$$V_{LSB} = \frac{2V_{REF}}{2^N} \quad (1)$$

Additionally, the RMS quantization noise of an ADC can be calculated as:

$$V_{Q(RMS)} = \frac{V_{LSB}}{\sqrt{12}} \quad (2)$$

Therefore, in our ADC design, the LSB voltage is 391 μV, which means that the quantization noise is 113 μV. For good noise performance, all circuits in the ADC should have a noise level lower than the quantization noise level.

B. Speed

Another issue of lowering the supply voltage is speed. When a transistor is in the subthreshold or weak-inversion region, there is an exponential relationship between the gate-source voltage and drain current shown by equation (3).

$$I_D = I_0 e^{\frac{V_{GS}-V_{TH}}{\alpha V_T}} \quad (3)$$

α is usually greater than 1 and is a nonideality factor. V_T is the thermal voltage of kT/Q. Lowering the supply voltage to 0.2 V can drastically decrease the speed of all the circuits in the design, especially the digital logic, as show.

V_{DD} (V)	Inverter Delay (ns)
1.8	0.052
0.2	1600

Table 1. Inverter delays with different supply voltages

A typical inverter delay is simulated at different supply voltages, and the input being a square wave with a peak-to-peak voltage of VDD. It can be seen that at 0.2 V, the delay of the inverter is more than 1000 times larger than at the nominal 1.8 V supply. One way to resolve this issue is by reverse bulk biasing. It has been shown that the threshold voltage of a transistor is represented by the following equation:

$$V_{TH} = V_{TH0} + \gamma\left(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}\right) \quad (4)$$

V_{SB} is the voltage from the transistor source to bulk. If V_{SB} is negative, the threshold voltage will be decreased, thus increasing the drain current for a given gate voltage by equation (3). Typically, the bulk of a PMOS transistor is set to V_{DD} and the bulk of an NMOS is set to ground. In order to achieve a negative source-to-bulk voltage the NMOS and PMOS bulk voltages can be switched, thus setting the PMOS bulk to ground and the NMOS bulk to V_{DD}. This technique can only be used when the supply voltage is well below the turn-on voltage of the PN junction that exists between the source or drain and bulk of a transistor. In our 180nm process, this turn-on voltage is ~0.5 V, which is much higher

than a supply of 0.2 V. Figure 4 shows an inverter with the bulks connected in a normal manner, and Figure 5 shows the same inverter with reverse bulk biasing implemented. If reverse bulk biasing were implemented on the entire design, all PMOS bulks would be connected to ground and all NMOS bulks would be connected to V_{DD}.

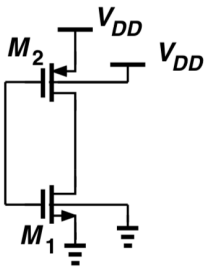

Figure 4. Inverter without bulk biasing

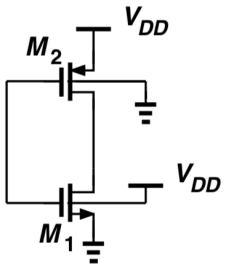

Figure 5. Inverter with reverse bulk biasing

C. Variable N/P Ratios

The third design challenge presents the greatest risk to our design. Because of the exponential relationship between the drain current and several transistor parameters, a small change in these parameters can cause a large change in drain current. These parameters are affected by local mismatch, process corner, and temperature. Thus, the design is extremely sensitive to variations in process corner, mismatch, and temperature. These sensitivities could even cause logic failures in the design. We have already discussed that one way to increase the speed is to lower the transistor threshold voltages by reverse bulk biasing. However, if reverse bulk biasing is implemented, the design becomes even more sensitive to the variations previously discussed.

IV. Circuit Design

A. Double Bootstrapped Sampling Switch

In most modern ADCs, the problem of poorly conducting sampling switches is resolved by bootstrapping the switches. A bootstrapped switch is a circuit that minimizes the on resistance of a transistor despite large input and output voltage swings. During the sampling phase switches are turned on so the gate voltage remains a constant V_{DD}. During hold phase, the capacitor is recharged to V_{DD}. Typically, this approach provides enough linearity in the sampling switch, so the output tracks the input well. However, at our intended supply of 0.2 V, just a single bootstrap is not enough to provide the needed linearity. We need to 'double bootstrap' the switch which adds an additional capacitor. During the hold phase, both capacitors are charged to V_{DD}. During the sampling phase, the two capacitors are connected in series, thus providing a gate voltage (V_G) of $2V_{DD}$. Figure 6 shows the design used to provide the double bootstrapping. This design was simulated in Cadence and the SFDR was measured. The simulated design was able to achieve a SFDR of 94.01dB (Figure 7) thus ensuring that the sampling switches will provide enough sampling linearity for our 10-bit design.

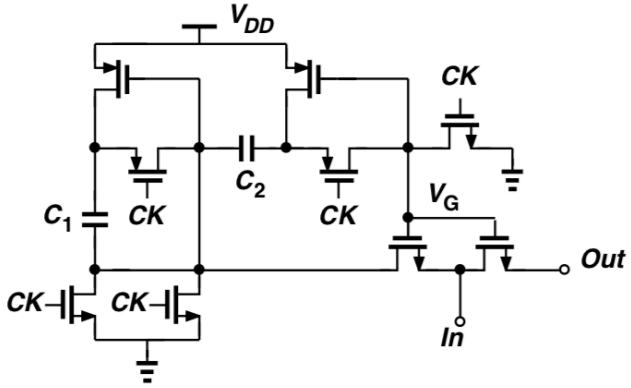

Figure 6. Double bootstrapped switch schematic

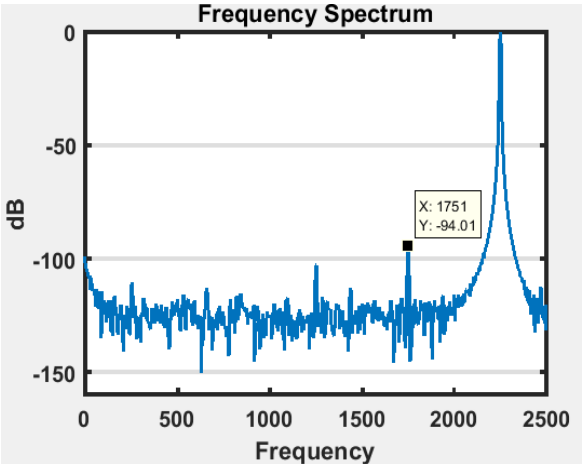

Figure 7. Output spectrum of double bootstrapped switch

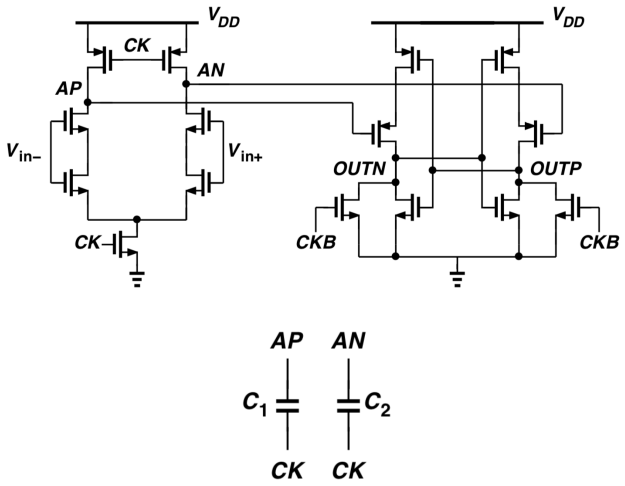

Figure 8. Two-stage dynamic comparator schematic

B. Comparator

The comparator (Figure 8) is a two-stage, dynamic comparator. The first stage is an amplification stage with Vin+ and Vin- as a differential input at AN and AP as a differential output. This stage utilizes a double input NMOS pair to decrease discharge time and increase noise performance. The second stage is a simple voltage amplifier and a positive feedback, cross-coupled latch to obtain rail-to-rail digital outputs OUTN and OUTP. Additionally, capacitors C1 and C2 are inserted between CK and AN/AP to boost up those nodes so they discharge for a longer period of time, thus providing higher gain in the first stage. This improves the overall noise performance of the comparator. To illustrate the operation, Figure 9 shows the transient voltages during one comparison cycle. During the reset phase (CK low and CKB high), AN and AP are reset to VDD and OUTN and OUTP are reset low. To start a comparison, CK transitions high (CKB transitions low), and AN/AP start to discharge from VDD to ground. Because the input is differential, one node will discharge slightly faster than the other, which produces the differential output as the common mode output falls to ground. When the common mode voltage is low enough, the second stage input transistors are turned on and the differential signal is again amplified. Eventually, the positive-feedback latch takes over and forces the outputs to rail to V_{DD} and ground.

This comparator virtually has no power dissipation because the power dissipation in the first stage stops when all nodes have discharged. In the second stage, the power dissipation stops when the positive-feedback amplifier has settled. Therefore, when the comparator is not active, there is virtually no power dissipation, except for leakage currents.

The main source of input-referred noise in the comparator is the first stage. The noise of the second stage is divided by the gain of the first stage so its noise contribution can be neglected. The noise of the first stage is mitigated by use of the boosting capacitors C1 and C2, and by the stacked NMOS input pair. These techniques keep the overall noise of the comparator below the quantization noise of the ADC.

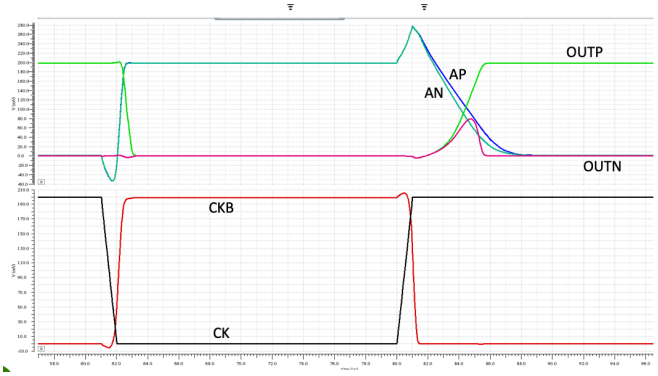

Figure 9. Waveforms showing comparator operation

V. Simulation Results

The proposed 10-bit differential SAR ADC was designed using a 0.18 um CMOS process. The design was simulated and verified. The circuit layout was then completed, Design Rule (DRC)/Layout vs. Schematic (LVS) checks were run, and parasitic extraction was performed. Extracted simulations were conducted to measure the SNDR and SFDR with and without transient noise. Without noise, the SNDR is 61.3dB (Figure 10). With noise, the SNDR drops to 57dB. The ADC and bulk bias circuitry consume 9nW of total power while operating at 5kS/s. Calculating Walden's figure of merit for our circuit yields a power efficiency of 1.91 fJ/conversion-step. All simulations were run in the Cadence design environment. Table 2 compares our results with the results of similar SAR ADC designs.

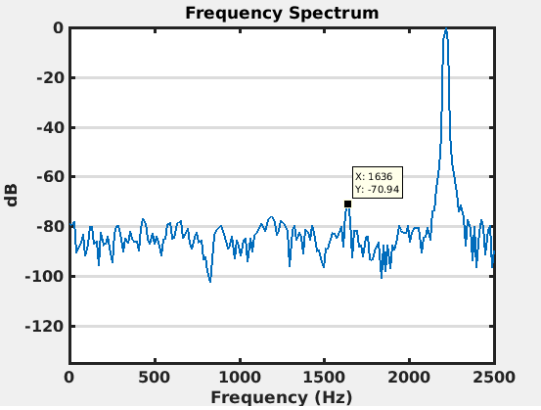

Figure 10. Reconstructed Output Spectrum of ADC

	[16]	[19]	[22]	[21]	This Work
VDD (V)	0.5	0.3	0.3	0.2	0.2
Tech. (nm)	180	180	90	180	180
Fs (kS/s)	4	5	90	0.25	5
Power (nW)	31	15.6	35	0.61	9
SNDR (dB)	59.3	54.56	52.2	47.7	61.3
ENOB	9.55	8.77	8.34	7.63	9.88
FOM (fJ/c.step)	10.3	7.3	1.17	12.4	1.91

Table 2. Comparison of our design with other works

VI. Conclusion and Future Work

This paper has discussed a 10 bit 0.18um CMOS SAR ADC for use in a distributed wireless sensor network in space. By using a 0.2 V supply voltage, asynchronous dynamic logic, and low-complexity design, an energy efficiency of 1.91 fJ/conversion-step could be achieved at 5 kS/s in extracted Cadence simulations. The future research that needs to be done is post-silicon testing. The chip is being fabricated by On Semiconductor and will be ready for testing in May 2019. We expect the testing to be completed by August 2019. Post-silicon test results will be available after testing.

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