Low Power, High-Speed Radiation Tolerant Computer & Flight Experiment

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Sponsors: Air Force Research Lab & NASA/MSFC
Space Micro Satellite Computer Goals

- Space Computer Performance Goals:
  - >1,000 MIPS throughput
  - Less than 1 SEU in 1,000 days
  - Less than 10 watts power

Results:

- **Proton100k** Performance:
  - >1,000 MIPS throughput
  - Less than 1 SEU in 1,000 days
  - 7-9 watts power

- **Proton200k** Performance:
  - 4,000 MIPS throughput
  - Less than 1 SEU in 1,000 days
  - 5-7 watts power
SEU Correcting Technology: Time-Triple Modular Redundancy

➢ Combines Time and Spatial (TMR) Redundancy techniques
➢ Runs TMR'd software on different ALUs of VLIW processor
➢ Two versions of software are run in first time step
➢ Time redundancy used in running the third version
➢ Third version run only if the results of first two versions don't match

TTMR is Patent Pending

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TTMR™ Software Flow

- Pre-compiler inserts TTMR
- Modifications made according to the algorithm selected
- The output program is SEU hardened!

High Level (C / C++) input program

TTMR Algorithm

Space Micro's Pre-compiler

TTMR'd Program
SEFI Solved with Hardened Core™: H-Core is More Than a Chip!

- Timer code when NO SEFI
- KILL Threads post SEFI
- Read H-Core Status Flags
- Flush cache & registers
- Recovery routines
- Rollback software routines

** Patent Pending **

Software + hardware
Software allows for post SEFI Recovery

** Patent Pending **
TTMR™ & H-Core Enable New CPUs

Equator BSP-15:
- 2,400 MIPS
- 4.9 W @ 400MHz
- 0.15um TSMC

TI 320C6415/6713 DSP:
- 8,000 MIPS fixed point
- 1.35 GFLOPS floating pt
- 1.7 W @ 1 GHz
TTMR & BSP-15 Test Results

➢ During the test the processor was bombarded with proton flux ranging from $1 \times 10^{-12} \text{A}$ to $7.5 \times 10^{-9} \text{A}$ (at 51 MeV)

➢ Earlier TTMR tests showed stored errors

➢ TTMR algorithms modified (v2.2)

➢ During the test, multiple SEUs were observed, TTMR v2.2 was able to detect and correct all SEUs

➢ The expected error rate in mitigating SEUs using TTMR is $1 \times 10^{-4}$ unrecoverable upsets/day

➢ BSP-15 has a total dose of 95 krad making it a good candidate for use in aerospace applications

➢ TTMR has been shown to detect and correct SEU’s in both VLIW processors (100% of the time)
**H-Core Radiation Success Rate**

**Intel Pentium III**

- NMI
- INT#
- BUS#
- SOFTWARE WATCHDOG
- LOCAL APIC
- HARDWARE WATCHDOG
- RESET

**Texas Instrument 320C6713**

- NMI
- GT
- GP
- GP#
- GT#
- HINT
- INT#
- INT!
- IRST
- RESET

Note: OS prevented full access to interrupts

**Equator Tech. BSP-15**

- NMI
- INT#
- INT!
- INTE

**H-Core has been shown to detect & correct SEFI’s (100% of the time)**

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Small Satellite Conference 2005
Proton100k Computer in RoadRunner Mission

Fusion Processor - Top View

To Spacecraft Bus

To TDRS Bus

350-400 MHz
95 MHz
47.5 MHz
23.75 MHz

3 MB EEPROM

RS-422

SEM

Power Control

EDAC FPGA 208 pin
RT54SX72S (CQFP256) - Final
APA-450 (PQFP208) - Brass

EDAC FPGA 165 pin
RT54SX72S (CQFP256) - Final
APA-450 (FBGA256) - Brass

128 MB SDRAM

PCI & S-CRTL FPGAs
RT54SX32S (CQFP256)-Flt
APA-450 (FBGA256)-BB

Power Conversion
28 Vin
(DC-DC & Vreg)

Power Control

UART #1

UART #2

I2C

Comm

to Flash or EEPROM

SEFI H-Core

To Spacecraft Bus

To TDRS Bus

SEFI

64 bit +

12 control

jpeg + Rx

set & clk

Addr + Ctrl

Addr + Ctrl

64 Data

Clocks

PCI Target

SDRAM Controller

RX data from MSP

Redundant Supply

Solid State Buffer
8 GB – Separate Board

MSP
Fusion Processor – aka Proton100k

Air Force: Fusion Processor version of Proton100k

- BSP-15 VLIW CPU
- >1,000 MIPS
- 256 MB local SDRAM
- EDAC for SDRAM
- 2 UARTs – 230 kbps
- 2 MB EEPROM memory
- Reconfigurable firmware
- PCI interface to SSB
- 2 Gbps 64 bit data interface
- Rx 64 bit data interface
- Power circuits & control
- 4 RH FPGAs

- Master ROPE controller
  - Imager control (on/off)
  - Image storage to SSB
  - CDL communication
- Management of SSB & MSP
- Storage of IAU telemetry
- Reconfigurability of FP/MSP
Proton100k cPCI 8GB Memory Board

Air Force: 8 Gbyte Solid State Buffer

- 8,000 MB SDRAM
- 2 Interfaces
  - PCI bus interface
  - 2 Gbps 64 bit data interface
- Segregated Rx Data IO
- 2 RH FPGAs
- EDAC for SDRAM option
- 6.6 W operational power
**ROPE Fight Experiment Operation**

**Flight Test of Proton100k will provide SEU & SEFI data**
Space Micro Rad Hard Computer Summary

Technology:
• TTMR & H-Core Proton Tested

Products:
• Proton100k developed & built

Flight Programs:
• Multiple flight programs
• Flight software & housing developed
• Proton100k Flight units delivered to AF
• SSB Flight units delivered to AF
• Currently in integration at AF
Next Step: Extensions to Proton100k

- Rad Hard Proton200k currently available
  - 675 GFLOPS floating point DSP
  - 4,000 MIPS fixed point DSP
- Ran test examples of TTMR in Xilinx FPGAs
- Rad Tested performance
  - TTMR works to correct SEUs
  - H-Core2 works to reconfigure FPGAs
- Space Micro currently designing Proton300k

Thank You