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APPLICATION OF THE NUCLEAR MICROPROBE TO THE IMAGING OF SINGLE EVENT UPSETS IN INTEGRATED CIRCUITS

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Abstract

A new form of microscopy has been developed which produces micron-resolution maps of where single event upsets occur during ion irradiation of integrated circuits. Utilizing a nuclear microprobe, this imaging technique can irradiate, in isolation, individual components of an integrated circuit (e.g. transistor drains, gates, feedback resistors) and measure immediately the effect of a high energy ion strike on circuit performance. This detailed circuit characterization technique provides a precision diagnostic with which to evaluate the design of integrated circuits that are to be used in space or other radiation environments.

Key Words: Single Event Upset, Nuclear Microprobe, Radiation Testing, SEU-Imaging

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Introduction

Nuclear microprobes utilize magnetic and/or electrostatic lenses to focus high-energy ion beams to micron dimensions. Using a variety of traditional ion beam analysis techniques, including Rutherford Backscattering Spectrometry (RBS), Proton Induced X-ray Emission (PIXE) and Nuclear Reaction Analysis (NRA), ion microbeams can be directed at a fixed point on a target to provide highly localized information about a target's composition, or scanned across a small area of the sample to generate a high-resolution compositional map [2]. Since its introduction over a decade ago, the nuclear microprobe has been used to study a wide variety of problems; target materials have included samples of mineral ore deposits, biological specimens, the extremely fine bond wires used to connect integrated circuits within their packages, and even the debris from explosions - in order to investigate possible causes. The common trait in all of these applications of the nuclear microprobe has been their reliance on the spectrometry of atomic or nuclear reaction products, or scattered ions, to discern the composition of the target. In applying nuclear microscopy techniques to the problem of radiation-induced upsets in integrated circuits (IC), we depart from this traditional practice and instead use the malfunction of the irradiated IC itself as the detected signal - thus creating a wholly new form of microscopy we call SEU-Imaging.

Single Event Upset

Increasingly, the operation of modern avionic and space systems has become critically dependent on complex electronics. However, the radiation environment of space and the outer atmosphere is far harsher than that experienced at the earth's surface. Without the protective barrier of the Earth's atmosphere, systems which operate in this environment are regularly bombarded with energetic charged particles of both

galactic and solar origin. The collision of a single high energy cosmic ray with sensitive regions of a system's electronics can result in disruption of its functions; such an event is called a single event upset (SEU).

Continuing advancements in IC fabrication technology have led to more densely packed integrated circuits with reduced feature sizes. These developments have heightened the problem of IC failure resulting from exposure to transient ionizing radiation. As the feature size in current generation ICs has decreased, the amount of stored charge which represents a logic state has also decreased. Consequently, an upset can now occur as a result of the charge deposited by a cosmic ray strike that would have been insufficient to upset an older, less densely packed IC. The advent of even higher resolution masking technologies using x-ray lithography only enhances this trend toward smaller feature size and therefore "softer", more upset-prone, electronics.

Existing techniques designed to obtain high resolution spatial information about the upset susceptibility of integrated circuits have used pulsed picosecond lasers [1] or focused, pulsed electron beams [4] to produce upsets in their targets. However, unlike energetic ions, a laser beam can be obstructed by optically opaque layers within the circuit. An electron beam can, likewise, be shadowed by thick metallic lines or overlays. This impediment to testing all areas of a circuit becomes more acute when such techniques are applied to more complex, multi-layered circuits. Another disadvantage of not using ions to simulate the upset process lies in the differences in geometrical shape and time scale of the ionization track produced by a pulsed electron or laser beam and that produced by an incident ion. Conversely, use of focused ion beams, and all the requisite support equipment, is not nearly as convenient as a laser or electron beam-based system. In order to test upset-hardened circuits, high energy linear accelerators or cyclotrons must be used. Furthermore, to achieve controlled single ion delivery, special modifications to an accelerator's beam transport system are necessary. Nevertheless, by using accelerated ions we come closest to reality in simulating the radiation effects encountered by integrated circuits in space.

By applying ion microbeam techniques to the study of upset generation in integrated circuits, micron-resolution "upset maps" can be recorded which locate where upsets occur in an integrated circuit under irradiation. Comparison of the SEU-Image with the circuit mask provides detailed information about which components of an IC upset under irradiation. Unlike traditional whole-chip SEU testing using broad ion beam exposures, in which the identity of the upsetting circuit elements must be inferred from the aggregate measured upset cross sections, the SEU-Imaging technique allows

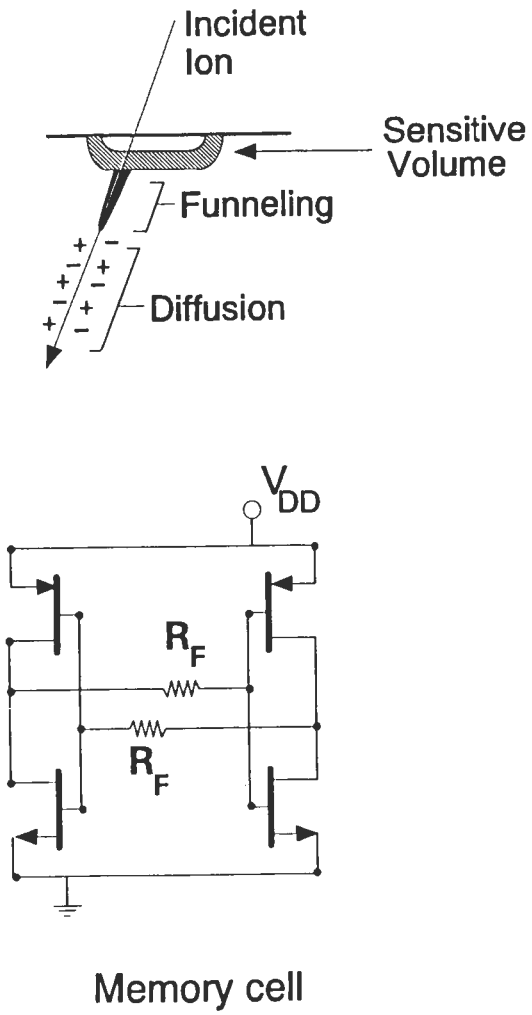

Figure 1. A charge spike can be introduced into a circuit by the passage of an energetic particle through an IC. If the collected charge exceeds a critical amount and persists for a sufficiently long time, the logic state of the memory cell (below) can be altered.

direct observation of those components which upset. Furthermore, use of the ion microbeam allows threshold upset measurements to be made on the scale of a *single* transistor component, rather than the entire chip.

Before describing the SEU-Imaging technique, it is necessary to briefly introduce the primary features of the upset process itself. Shown in the lower portion of Fig. 1 is a schematic diagram of a single cell of a static random access memory (SRAM). It is comprised of two cross-coupled inverters forming a bi-stable memory element. The feedback resistors present in the cross-coupling act to increase the time-constant for charge transfer (the decoupling time), thus reducing the memory cell's upset sensitivity - but also reducing the response time of the circuit [7]. The decoupling time determines how long charge must be present at a node before the

memory cell changes states.

As illustrated above the circuit, when an energetic ion strikes and penetrates into the silicon of an integrated circuit, it leaves in its wake a trail of excess electron-holes pairs. Some portion of this excess charge is collected, via a process which has been termed "funneling" [5]. If the resulting collected charge persists for longer than the decoupling time of the circuit, it can induce the memory cell to change its logic state. It has been observed, however, that not all areas of an IC are equally susceptible to upset [6]. On the microscopic scale of the circuit, there may be only a small fraction of circuit components, or sensitive regions within these components, which cause upset. The SEU-imaging technique allows these areas to be directly imaged and differences in their upset sensitivity to be determined.

Linear Energy Transfer

The occurrence of a radiation-induced upset in an integrated circuit depends primarily on where the incident ion strikes the circuit, and on how much ionization occurs along the ion's path within the circuit. Using the nuclear microprobe, the impact point of the incident ions on the IC can be controlled with micron resolution. The amount of ionization which occurs within the sensitive regions of the circuit is controlled by the selection of the ion species, incident energy, and angle of incidence of the ion beam.

Ion energy loss in materials has been extensively studied in the field of ion beam analysis - with the emphasis placed on the energy loss incurred by the incident ion, i.e. the target material's stopping power (dE/dx) [8]. In the study of radiation effects in devices and circuits, the emphasis is placed not on the energy lost by the incident ion, but on the charge generated by the ion within a limited volume of the target through ionization. In this context, the ion's loss of energy in the target is referred to as the ion's Linear Energy Transfer or LET. Both processes, of course, share the common units of energy loss, MeV/mg/cm^2.

By varying the ion species, ion energy and incident angle, we can control the LET, and therefore the amount of collected charge. With regard to Fig. 1, this corresponds to generating a higher density of electron-hole pairs in the sensitive volume and therefore more collected charge. The selection of the ion beam(s) to be used in an SEU-Imaging measurement is dictated by the minimum LET required to upset the circuit, as well as by the depth of penetration required to completely traverse the sensitive volume of the circuit. By changing the ion's angle of incidence, its path length in the sensitive volume can also be increased, resulting in greater charge collection. For modern microcircuits the

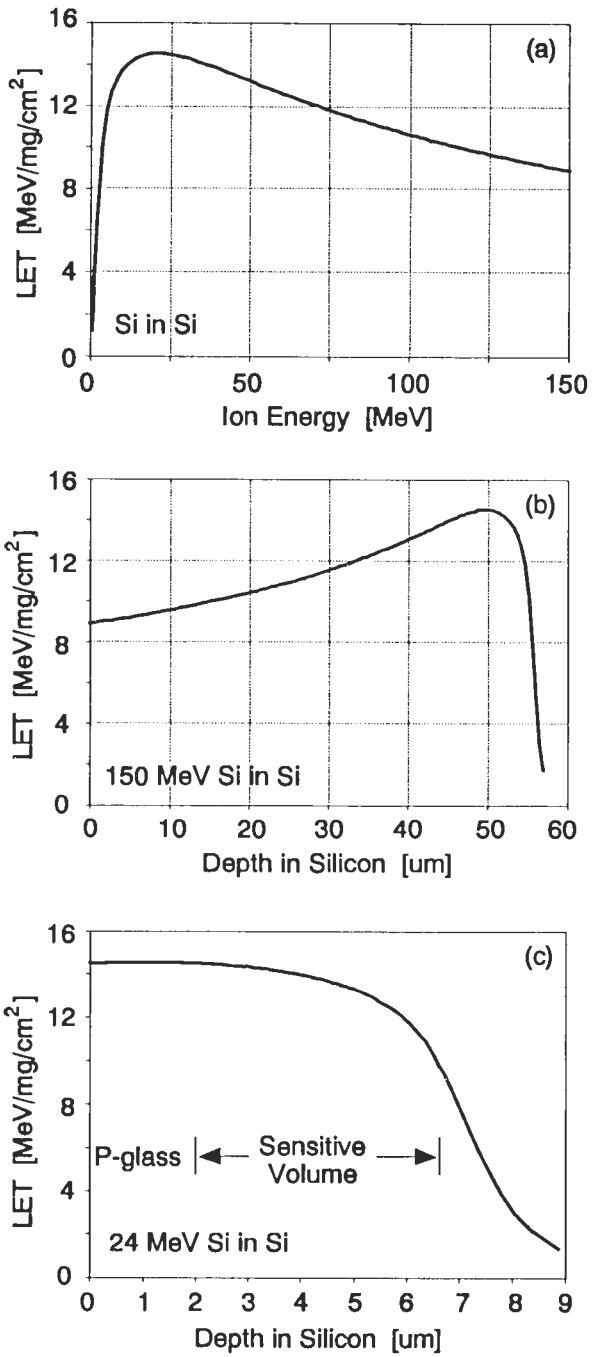

Figure 2. The LET (Linear Energy Transfer) of an ion varies with energy and depth. (a) calculated LET spectra for 150 MeV Si ions in Si, (b) LET vs. depth for 150 MeV Si in Si, and (c) LET vs. depth for the 24 MeV Si ions used in the SEU-Imaging of the TA-670.

sensitive volume is generally from 2 to 10 microns deep.

To illustrate the dependence of LET on energy, a plot of calculated LET versus ion energy for a 150 MeV silicon ion in silicon is illustrated in Fig. 2a. The characteristic maximum energy loss, or Bragg peak,

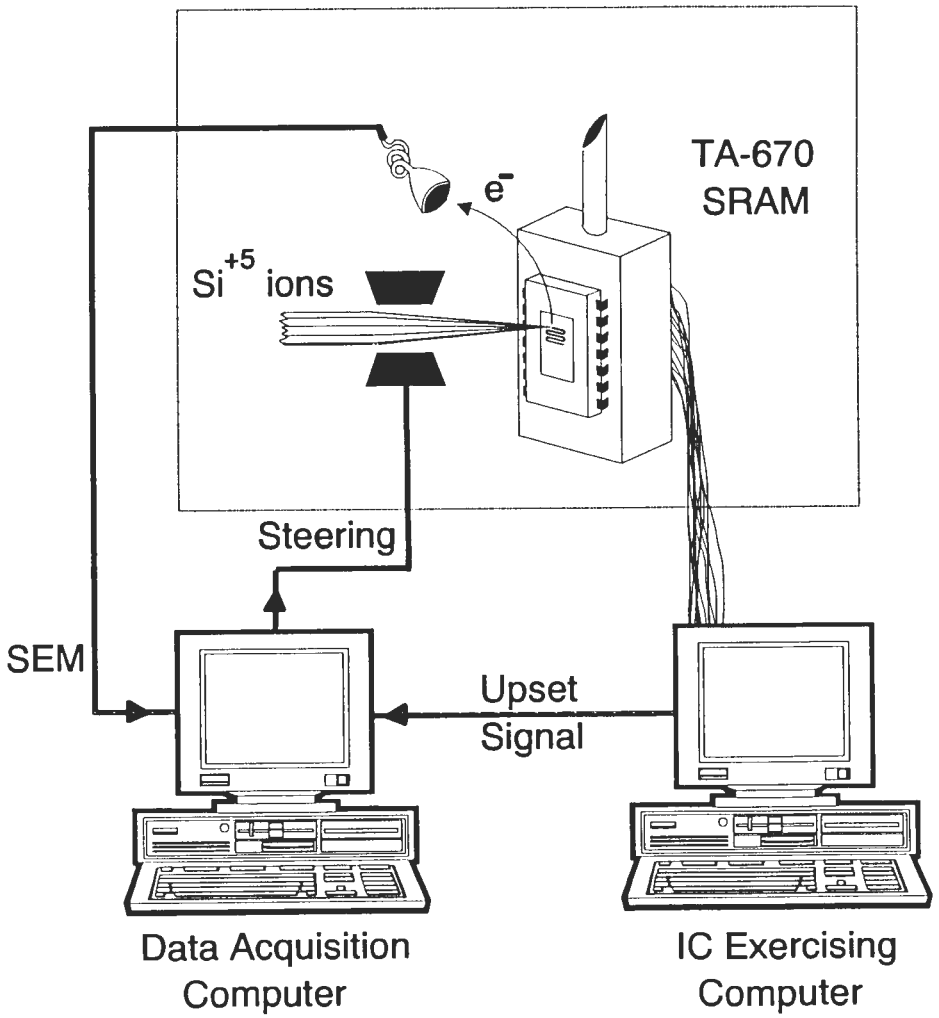

Figure 3. Schematic diagram of the SEU-Imaging apparatus.

occurs at an ion energy of about 21 MeV. At both lower *and* higher energies, the LET of the ion is lower. The significance of this elementary fact is that as the ion loses energy, its LET will change. Therefore, the ion's LET will also change with depth in the target IC, as illustrated in Fig. 2b. For the purposes of extracting detailed dosimetry data, it is important to provide as constant a particle LET as possible within the sensitive volume.

In order to mitigate the effect of changes in LET during the ion's passage through the circuit, the energy of the ion, if possible, is selected to be above the Bragg peak. In this way the least change in LET occurs as the ion loses energy traversing the circuit. A plot of LET versus depth is shown in Fig. 2c for the 24 MeV silicon ions used in the SEU-Imaging measurements of the TA670 SRAM presented below. The depth of the overlying p-glass passivation layer and the sensitive volume of the TA670 circuit are also indicated within the figure.

SEU-Imaging Technique

Depicted in Fig. 3 is a schematic representation of the SEU-Imaging apparatus. We utilize the existing microbeam facility on the EN Tandem Van de Graaff accelerator at Sandia National Laboratories to deliver a focused beam of energetic ions to the target IC. The design details of this ion microbeam system are presented elsewhere [3]. The target is mounted in a commercial IC socket which is appropriately wired to an external "exercising" computer that operates the chip during the ion exposure. The critical task of focusing the ion beam in the plane of the target IC is done by optimizing the secondary electron image obtained from a corner of the silicon chip. Since there are no circuit elements near the edges of the chip, focusing procedures can be carried out with prolonged ion beam exposures without any cumulative radiation damage to the circuit. Moreover, the corner of the chip is an opportune focusing target since the focus in both the x and y directions can be optimized simultaneously. After focusing, the width of the incident ion beam at the target

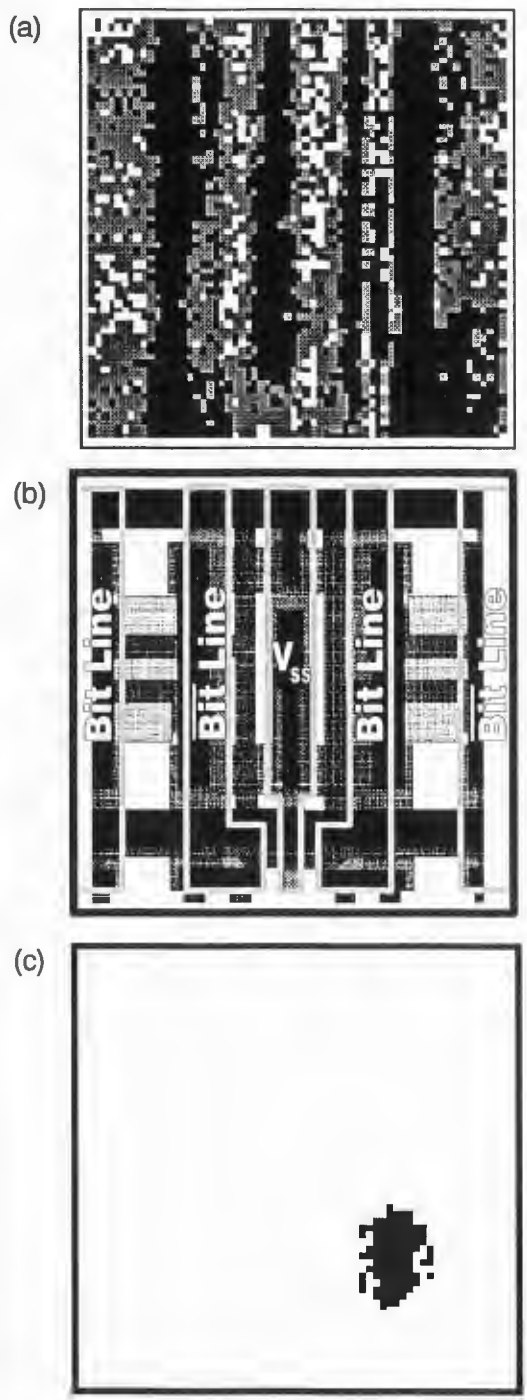

Figure 4. SEU-Images: (a) secondary electron image produced by the ion beam, (b) circuit mask of the TA670 SRAM with the metallic surface features highlighted, and (c) the corresponding SEU-Image recorded for logic 1 to 0 upsets.

surface is approximately 1 micron; this is determined from secondary electron micrographs of transmission electron microscope (TEM) grids also mounted on the target holder.

The normally incident ion beam is rastered over a 64x64 position grid, covering an area approximately 50μ on edge on the IC surface. The rastering of the ion beam, and therefore its impact point on the target surface, is controlled by the "data acquisition" computer. In this way, registry is maintained between the position of the incident ion beam on the target and the signals arising from that exposure. The impinging ion beam can give rise to two detectable signals - the emission of secondary electrons from the target (produced when the ion strikes the surface) and secondly, the generation of a malfunction, or upset, in the target circuit's operation (resulting from the charge generated as the ion penetrates into the silicon).

The emission of secondary electrons is detected by a channeltron secondary electron detector mounted in the target chamber. The intensity of the secondary electron signal that is detected as the ion beam sequentially exposes each of the 64x64 positions of the raster scan is stored in a 64x64 element memory array. This array, in toto, constitutes a secondary electron image of the surface of the circuit over which the ion beam is being rastered. Comparison of this image with the circuit's design mask, then, tells us where the ion beam is *striking* the target circuit.

The occurrence of an upset in the circuit is detected by the "exercising" computer. This computer is programmed to operate the IC, and if a fault is detected, to output a pulse to the data acquisition computer. Upon receiving an "upset" pulse, the data acquisition computer increments the array element corresponding to the current position of the ion beam on the target in a separate 64x64 array. This "upset array" constitutes a map of where SEUs are occurring in the circuit for the selected LET. This image tells us where the ion beam is *upsetting* the target circuit.

The duration of the ion beam exposure at each point in the scan is controlled by the data acquisition computer. All pixels in the scan are exposed for an equal period of time, and therefore to an equal incident dose. The duration of the ion exposure at each point can be changed in the control software, ranging from 1 microsecond to an arbitrarily longer time, in order to accommodate the tolerances of each particular test chip. For the images presented in Fig. 4, 5, and 6 a dwell time at each scan point of 5 milliseconds was used.

Of course, the number of ions required to generate a single event upset is, by definition, only one, while the number of ions needed to produce a secondary electron image of the scanned region can require the use of beam currents of tens of picoamps. So, in practice, the upset image is recorded first using an ion flux on the femtoamp scale, and only afterwards is the secondary electron image measured using picoamp beam currents.

Displayed in Fig. 4 are the images produced during an SEU-Imaging measurement of a TA670 16K SRAM. The ion-generated secondary electron image of the scanned region is shown in Fig. 4a. The design mask, scaled to the size of the secondary electron image, is given in Fig. 4b. The design mask has been annotated to highlight and label those metal surface features which are most visible in secondary electron imaging. Lastly, the upset image, measured for a single scan of the microbeam across the target area, is shown in Fig. 4c.

From comparison of Fig. 4a and 4b, the positioning of the design mask relative to the SEU-Image of Fig. 4c is determined. Because the secondary electron image arises not from the microamp electron beam of a commercial SEM, but rather a picoamp ion beam, and because the overlying passivation layer of the IC is not removed for SEU-Imaging measurements, the resulting secondary electron image is less distinct than usually produced by secondary electron microscopy. However, these limitations notwithstanding, the acquired image does display the characteristic convergence of two bit-lines and a V_{ss} line, thus providing a landmark with which to scale and orient the design mask of Fig. 4b. Exactly which of the TA670's 16,384 memory cells is being struck by the ion beam is initially determined by momentarily exposing the chip to the rastered ion beam and polling the entire memory chip to find out which cell has upset. Thereafter, only that single memory cell is polled for upsets. Once correctly oriented with respect to the upset image, the circuit's design mask is used to determine which circuit components are being scanned by the ion microbeam. Finally, comparison of the upset image in Fig. 4c and the circuit design mask in Fig. 4b allows identification of the circuit element which is upset by the heavy ion beam. In this instance, the upset image overlays an n-drain in the TA670.

Upset Images of the TA670 SRAM

The upset images presented in Fig. 4, 5, and 6 were measured using a TA670 SRAM chip which utilizes 2 micron fabrication technology. We made use of a small number of TA670s which had been specially fabricated with reduced feedback resistance in order to increase their otherwise low upset susceptibility. However, using our 4 MeV EN Tandem accelerator, we still had to rely upon coincident ion strikes of a 100 femtoamp, 24 MeV Si ion beam (15 LET) to produce upsets in the chip. We might note however, that subsequent SEU-imaging measurements have been made on unhardened commercial 1 Mbit SRAMs, which possess much lower upset thresholds, and that on such chips single ion upsets can be produced using ion energies normally used for ion beam analysis applications (2 to 6 LET). The effect of accumulated radiation damage during the imaging process was checked by recording the number of upsets per ion beam scan until total failure of the memory cell occurred. This measurement indicated that, for these conditions, up to a hundred individual scans could be performed before significant changes in performance were observed.

As stated previously, in order to avoid damage to the memory cell before its upset response is measured, upon moving to a new location on the IC, the upset image is recorded first - and only after that is a secondary electron image collected. This means that for each measurement, the memory cell is arbitrarily positioned under the microbeam's scan. Thus, the position of a memory cell within the frame of the microbeam's scan area must be determined for each upset image, after the measurement, from comparison of its secondary electron image with the circuit design mask.

The upset image in Fig. 4 results from a single scan of the microbeam across the memory cell. A second upset image is shown in Fig. 5, in which scanning was continued until no new upset locations were recorded - requiring in this case, seven scans. The upset image is presented in gray-scale to illustrate the variation in upset frequency within the upsetting region. The design mask of Fig. 5a has been annotated to highlight the n- and p-drains of the memory cell. As is evident, the ion impact positions which give rise to measured upsets at this ion beam energy are quite localized and cover a region encompassing an n-drain.

The SEU-Imaging technique also affords the opportunity to measure logic-state dependent upsets and to look at their positions in the memory cell. Fig. 6 displays the upset images measured from a memory cell that has been ion irradiated under two different conditions: (a) while a logic high was stored in the cell and (b) while a logic low was stored in it. Under both conditions the memory cell experiences upset. However, as is apparent from the figure, depending on the logic state stored in the memory cell, the upsets occur in different regions of the memory cell and the area sensitive to upset is of a different shape and size.

Future Applications

The ability of this new microscopy technique to identify, on a micron scale, upset-prone components in integrated circuits has applications ranging from its use by VLSI engineers to "design-out" weak components in an integrated circuit to the verification of three-dimensional software codes used to simulate radiation upset processes. As the trends toward smaller IC feature size continue, experimental verification of circuit

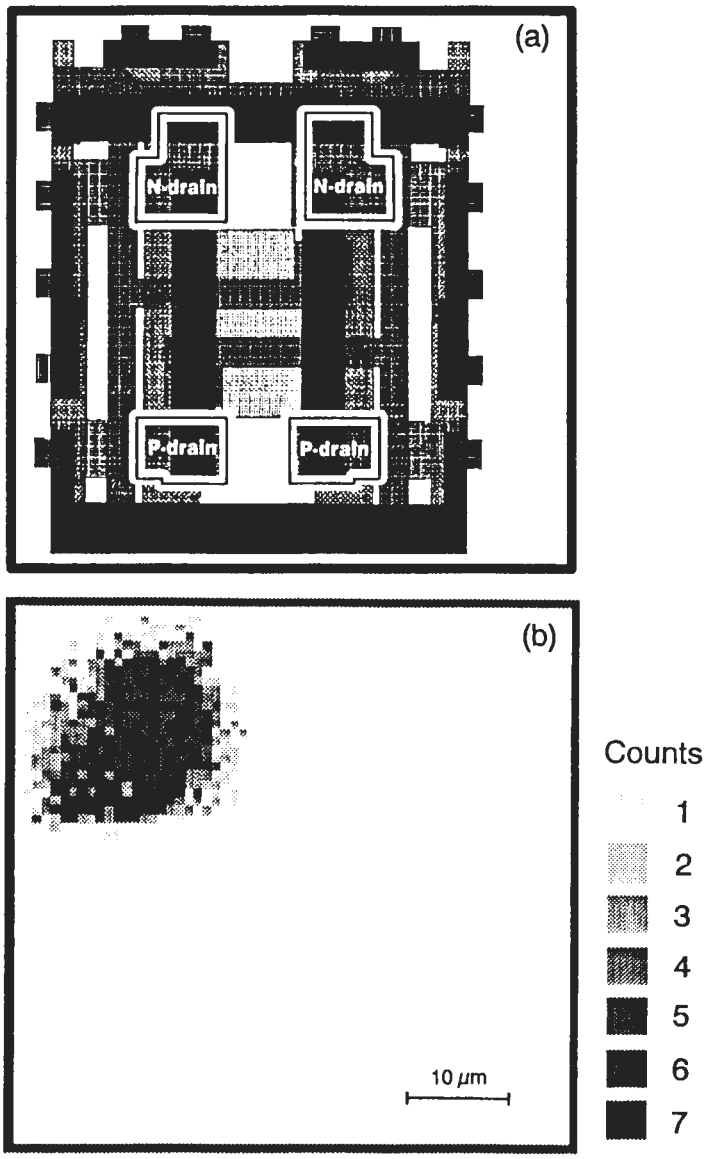

Figure 5. SEU-Images: (a) circuit mask of an individual memory cell scaled to size, (b) gray-scale upset image of a single TA670 memory cell recorded for logic 1 to 0 upsets.

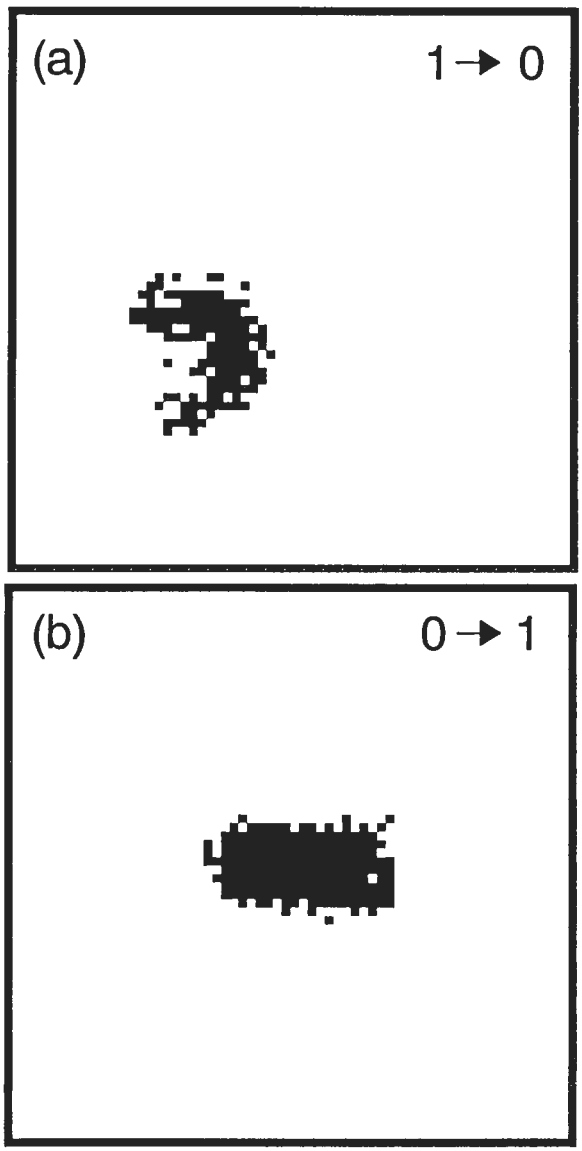

Figure 6. Logic state dependence of the SEU-Images measured on the TA670: (a) logic 1 stored in the memory cell during SEU-Imaging, (b) logic 0 stored in the memory cell during SEU-Imaging.

simulators will become increasingly important.

One interesting application of the SEU-Images may be to identify isolated areas of upset susceptibility (perhaps a certain register or logic unit in a CPU) so that software designers can "program around" such regions to avoid system disruption or at least concentrate error detection and correction (EDAC) codes on these "upset-prone" regions and thereby increase the effective hardness of the IC.

This new microscopy technique affords the opportunity to uncover a wide range of important and previously inaccessible information. As advances in fabrication technology continue to enhance the power and speed of integrated circuitry, their use in space systems and high-altitude avionics will also increase. However, the increased vulnerability that these systems will have to radiation upset will also demand continued study of the upset process. Application of ion microbeam techniques to this problem provides a realistic simulation of the cosmic ray-circuit interaction and allows the position of this interaction to be controlled with micron resolution. As current generation microbeam systems achieve sub-micron spot sizes, this new diagnostic technique can be applied to current and future generation integrated circuits and serve as a useful simulation of the upset process.

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Discussion with Reviewers

E. Kubalek: Is your SEU-Imaging Technique applicable to more complex circuits with multiple metal layers, and how do you overcome the metal shadowing effect?

Authors: The technique can be used on complex circuits with multiple metal layers. A chief advantage in using ion microbeams to induce upset is that the ionization track is not shadowed or blocked by circuit structure. Only the energy loss (LET) of the ion changes as it traverses different material layers within the silicon - as occurs in reality for cosmic rays. The LET within any particular layer can readily be calculated.

E. Kubalek: How far are your simulated upsets in ICs under terrestrial conditions comparable to the real conditions in space (cosmic rays or nuclear recoil fragments versus ions, temperature, pressure, encapsulation of ICs etc.)?

Authors: Because high energy cosmic rays (GeV/amu) are far above the Bragg peak (see Fig. 2a), the LET of these ions is not at its maximum. It is only as such ions lose energy and approach the Bragg peak that they pose their maximum upset potential. This situation allows high energy terrestrial accelerators to simulate the worst upset effects of cosmic rays. The effects of other target parameters (temperature, pressure, etc.) can be determined experimentally. The issue of nuclear recoil fragments from the IC package or surrounding material is more difficult to simulate because of the extremely high energies which can contribute to the process. The products of such events can be estimated for each system based upon its design and the known nuclear reaction mechanisms and cross sections; upset testing can then be performed on the IC for these particular nuclear reaction products.

D.N. Jamieson: Have the authors attempted to correlate the peculiar shape of the '1 to 0' region shown in figure 6a with irregularities in the shape of the n-drain that could perhaps be imaged with micro-RBS?

Authors: We have not performed micro-RBS on the upset regions. The relatively high beam currents which must be run for RBS measurements would be destructive to the memory chip's operation. Such a measurement could be done only at the conclusion of all other measurements. Because of the inherent difficulty in resolving the silicon and aluminum peaks with RBS, use of micro-PIXE would probably be the best analysis technique to differentiate the doped silicon n-drain region from the surrounding silicon and aluminum of the integrated circuit.