OBSERVATIONS OF SINGLE-EVENT MEMORY UPSETS ON THE UOSAT-2 SATELLITE

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This paper describes observations of single-event memory upsets in the UoSAT-2 satellite Digital Communications Experiment. Two years of SEU observations for Harris 6564 memories are included, presented both as error rate statistics and as a map of satellite orbital location at the time of error occurrence. The results presented here are the preliminary observations in a long-term single-event upset study funded by ESA-ESTEC.

INTRODUCTION

The Spacecraft Engineering Research Unit at the University of Surrey (UK) has designed and built two technology demonstration and education satellites - UoSAT-1 and UoSAT-2. Both satellites were launched into low-earth polar orbits by NASA/DELTA (UoSAT-1 in 1981 and UoSAT-2 in 1984), and both are still operational in orbit. Amongst the many payloads carried by UoSAT-2 is a store-and-forward Digital Communications Experiment (DCE). The DCE comprises an NSC-800 CPU and 124 kbytes of CMOS static RAM used for store-and-forward digital message transfer. The UoSAT-2 DCE is amongst the first civilian store-and-forward satellite transponders, and it has demonstrated that inexpensive satellite terminals interfaced to standard personal computers can participate in a store-and-forward communications network using small low-earth-orbiting satellites. [1] [2] [3]. In addition to conducting communications experiments, the UoSAT-2 DCE monitors the transient and permanent effects of radiation on semiconductor memories.

DCE MEMORY CONFIGURATION

To obtain in-orbit experience with a range of memories of various sizes from several manufacturers, the DCE carries the following memory devices:

Manufacturer	Part	Chip Size	Quantity
Harris	HM-6564	4K X 1 bit	16K X 12 bits (equivalent to 48 HM-6504s)
Harris	HM-6516	2K X 8 bit	7 ICs
Hitachi	6264-LP	8K X 8 bit	8 ICs
Hitachi	6116-L	2K X 8 bit	16 ICs

The positioning of these devices within the DCE hardware is discussed in [4].

SEU MONITORING IN PROGRAM RAM

Programs and critical data are stored in the Harris 6264 memories. Each 8-bit data byte in this memory is protected by a 4-bit Hamming error detection and correction (EDAC) code. Thus, the memory is 12-bits wide. The code used is the standard Hamming (8,12), with distance 3, which can detect and correct single-bit errors. Programs, file allocation tables, and other frequently-accessed, critical information is stored in the EDAC-protected RAM.

Figure 1 is a block diagram of the Hamming generation and decoding circuits. On write cycles, data from the CPU is stored in data RAM, and presented to the input of a Hamming code generator. The output of the generator is the 4-bit check code, which is stored in code RAM. On a read, the stored data is applied to the input of a Hamming generator and a correction circuit. The generated code is compared with the stored code, and the result of this EXOR addition is also fed into the correction circuit. The correction circuit sends an error detect signal to the EDAC counter and the corrected data byte is sent to the CPU. An important characteristic of this circuit is that when it detects and corrects an error, the corrected byte is presented to the CPU, but not re-stored in data memory. To remove the upset from memory, the CPU must write the byte through the Hamming generator, back into memory. This requirement for a read-correct-write cycle influences the design of EDAC and SEU logging software.

The Hamming-based EDAC system can detect and correct any single-bit error. If the decoder reads a byte containing more than one bit error, that byte will be incorrectly interpreted and either passed on un-corrected or 'mis-corrected.' For correct DCE operation there must never be more than one upset bit in a byte before that byte is corrected by a write cycle. Hardware design and software techniques are used to guard against such multi-bit errors.

In hardware, the use of 1-bit-wide memories in the EDAC system physically and electrically isolates the bits in a byte from each other. Thus, even if a single cosmic particle event upsets several adjacent bits in the same memory chip, the upset bits will be spread across several different bytes. They will appear to the EDAC system as single bit errors and be corrected. A single cosmic ray event can cause an uncorrectable error only by upsetting bits in different chips which happen to be bits from a single byte - an unlikely event.

Uncorrectable errors will also occur if several separate SEUs change bits in the same byte. To protect against this possibility, DCE software must periodically check each byte in the program memory for errors and re-write (corrected) bytes which contain SEUs. The period between these checks must be smaller than the expected period between SEUs. This is called a 'memory wash', and it is part of the main loop in the DCE

system software. The main loop executes once in every 32 msec., resulting in a complete wash of the program RAM in less than 9 minutes.

The memory wash algorithm (Table 1) protects the program memory against accumulating SEUs and provides an accurate log of the time and memory address at which each SEU occurred. (The SEU log is kept in EDAC memory and is downlinked to the Command Station using the DCE messaging system.) Timestamps, which are read from the UoSAT-2 serial telemetry system, are accurate to within 1 minute, but SEU detection time is also influenced by the 9-minute wash cycle time. Before this on-board logging software was installed DCE SEUs were monitored by noting the hardware EDAC counter value during UoSAT-2 passes over the UoS Command Station. This resulted in good measurements of total SEU count, but the relationship between SEU occurance and satellite orbit location could not be studied. The new logging software was loaded in November, 1987, and has been operating nearly uninterrupted since then.

Table 1

DCE MEMORY WASH ALGORITHM

```
Begin Main Loop {

     disable interrupts;
     Save error counter value (N);
     Read the byte from next wash address;
     Save error counter value (M);
     enable interrupts;

     /*  If  error counter changed during the read, correct and  log  an
         error.
     */
     if (n <> m) {
          Write the byte back to the wash address to correct the error;
          Get the time from the telemetry system serial output;
          Log the wash address and the time;
     }

     Set wash address to next location;

     /* The rest of the DCE Main Loop is here. */

}    /* end of Main Loop */
```

EXPERIMENTAL RESULTS

Error Probabilities

Table 2 contains the log of SEUs since 10 November, 1987. These results reflect SEUs found in 144 kbits of Harris 6564 CMOS static RAM. (Although the DCE carries 192 kbits of this memory, 48 kbits had to be removed from service in 1986 because of a permanent failure.) There were 25 bit upsets in the 322-day observational period. There are three occurances of 'simultaneous' errors, which are assumed to be the result of single cosmic particles. This results in a mean error rate

$$22 \text{ SEU}/(322 \text{ days} * 144 \text{ kbits}) = 4.633 \times 10^{-7} \text{ SEU/bit/day} \quad (1)$$

Assuming an underlying Poisson distribution, the 5 to 95% confidence band is between 6.529×10^{-7} and 3.370×10^{-7} SEU/bit/day.

Still using the Poisson distribution, we can calculate the probability of two independent SEUs occuring within the same 9-minute memory wash interval.

$$P(9 \text{ min}) = 9.1 \times 10^{-8} \quad (2)$$

For an error to go undetected, two SEUs would have to occur in the same wash cycle and in the same byte. The memory size is 12 kbytes, so

$$P(\text{undetected}) = P(9 \text{ min}) / 12k = 7.4 \times 10^{-12} \quad (3)$$

This demonstrates that the 9-minute wash period is more than adequate to protect the DCE program and critical data from multiple bit errors from separate SEUs.

Orbital Position of SEUs

The SEUs have been plotted against satellite orbital position (Fig. 2). Most of the SEUs occurred when UoSAT-2 was traversing the magnetic South Atlantic Anomaly (SAA) - a point at which the magnetic field lines dip toward the Earth. UoSAT-2 is subject to increased trapped-particle radiation in the SAA, and this seems to cause a great increase in the SEU rate. This correlation will be studied in detail as more experimental data is gathered.

CONCLUSION

The UoSAT-2 DCE provides an in-orbit experiment in radiation-induced single-event memory upsets. The results of two year's SEU monitoring indicate that current hardware and software techniques can easily protect satellite computer software and data from SEUs in Harris 6564 RAMs. The strong correlation between SEUs and the South Atlantic anomaly

will be the topic of further investigation, as they are not consistant with current SEU simulation software packages.

Table 2
SINGLE EVENT UPSET LOG

EDAC Count	Date	Time	Location Address
1	10-19	01:52:50	7aee
2	10-25	13:19:11	7b78
3	11-05	03:25:45	56fe
4	11-20	21:44:14	7930
5	11-21	06:01:21	70cd
6	11-21	06:01:21	74ed
7	01-09	19:07:42	4299
8	01-09	19:07:42	4499
9	01-25	18:31:56	7375
10	02-01	02:51:21	7c96
11	03-17	01:13:25	5a15
12	03-20	02:06:15	4998
13	04-05	23:48:41	74c5
14	04-30	11:02:11	4402
15	05-03	02:07:39	5cb9
16	05-03	04:23:13	562b
17	05-03	04:23:13	580b
18	05-14	23:53:35	7de3
19	05-17	12:01:13	5805
20	?	?	?
21	06-17	01:06:36	45c1
22	06-17	03:12:35	7649
23	06-29	00:24:14	7641
24	07-04	01:59:32	5609
25	08-06	20:07:51	4dc9

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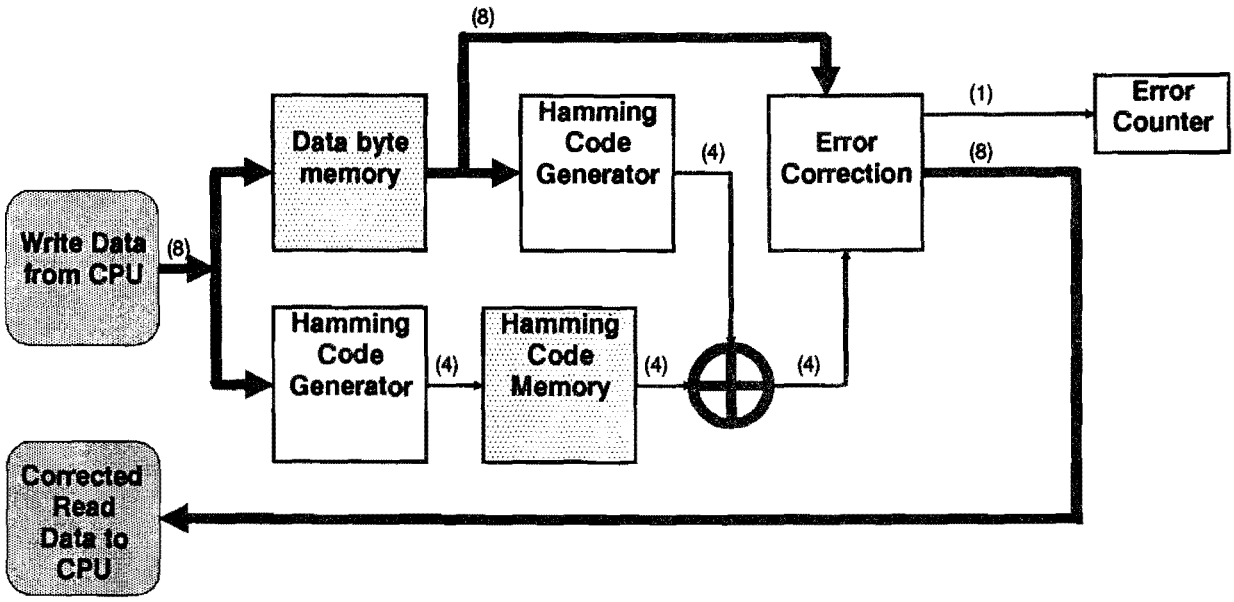

Fig. 1 EDAC Memory Block Diagram

Fig. 2 Orbit Position of SEUs