CubeSat Avionics Optimization

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• Introduction
• Motivation
• Approach
• Final Design
• Assessment and Discussion
• Acknowledgements
Introduction

- Candidate for S.M. in Aeronautics and Astronautics
- B.S. Aerospace Engineering with Information Technology, MIT ‘14
- Ensign, United States Navy
- Avionics Hardware Lead, Microwave Radiometer Technology Acceleration (MiRaTA) Spacecraft

Approach to optimizing CubeSat avionics on MiRaTA, whose mission is science technology demonstration*

*which means they keep trying to steal my SWaP
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Motivation

Examples of Current State of the Art

| Space Micro Proton 400K [1] | • Fits in 2U stack  
| | • 1 GHz, dual core, 32-bit processor  
| | • 1 MB EEPROM, 32Gb flash memory  
| | • 8-12W operating power  
| | • Radiation tolerance up to 100krad TID  
| | • Support for multiple OS’s (Linux, VxWorks)  

| Pumpkin Motherboard RevE [2] | • Fits in 1U stack  
| | • Open architecture – up to 32MHz, 16-bit  
| | • 256KB ROM, 64Mb flash memory  
| | • 100mW operating power  
| | • Tested radiation durability  
| | • Embedded C programmable  

MiRaTA needs: Efficient management of spacecraft activities using minimal resources, with COTS parts that can survive the harsh space environment.
Motivation

Minimal Resources

- Power
  - Electrical
  - Processing
- Size
  - Volume
  - Memory
- Cost
  - Money
  - Time

Harsh Environment

- Temperature
- Radiation
- Vibration
## MiRaTA Avionics Requirements

<table>
<thead>
<tr>
<th>Requirement</th>
<th>Limit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrical Power</td>
<td>200 mW idle, 2 W receiving, 10 W transmitting</td>
</tr>
<tr>
<td>Processing Power</td>
<td>32 MHz</td>
</tr>
<tr>
<td>Volume</td>
<td>100 mm x 100 mm x 85 mm</td>
</tr>
<tr>
<td>Memory</td>
<td>2 GB storage, 256 KB program</td>
</tr>
<tr>
<td>Cost</td>
<td>$30,000</td>
</tr>
<tr>
<td>Time</td>
<td>19 months</td>
</tr>
<tr>
<td>Radiation Tolerance</td>
<td>9.36 krad</td>
</tr>
</tbody>
</table>
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Approach: Resource Management

- Stacked, 4-Layer boards, no blind vias
- Smarter ICs and reprogrammability
- Off-board power/data management
- Flash memory on SPI network
- Appropriate selection of TTL vs CMOS
- Commercial off-the-shelf (COTS) where possible
**Approach: TID Radiation Testing**

**Expected Total Ionizing Dose for MiRaTA: 9.36 krad**

*Given minimum 1mm Al shielding over 1 year mission life in SSO* [4]

**Procedure:** Characterize components before and after TID gamma irradiation and compare to expected datasheet values at 8 krad, 16 krad, and 24 krad

**Results:** Components proved suitable for proposed orbit

<table>
<thead>
<tr>
<th>Component</th>
<th>Manufacturer</th>
<th>Tolerance</th>
</tr>
</thead>
<tbody>
<tr>
<td>Industrial-Grade Micro SDs</td>
<td>Delkin, San Disk, Transcend</td>
<td>24 krad</td>
</tr>
<tr>
<td>N25Q512 Serial NOR Flash Chip</td>
<td>Maxim</td>
<td>24 krad</td>
</tr>
<tr>
<td>MAX892 Current Limit Switch</td>
<td>Maxim</td>
<td>24 krad</td>
</tr>
<tr>
<td>FPF2000 Current Limit Switch</td>
<td>Fairchild</td>
<td>24 krad</td>
</tr>
<tr>
<td>SN65HVD Line Transceiver</td>
<td>Texas Instruments</td>
<td>24 krad</td>
</tr>
<tr>
<td>ADG452 SPST Switch Array</td>
<td>Analog Devices</td>
<td>16 krad</td>
</tr>
</tbody>
</table>

*assuming an elliptical SSO*
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Final Design

MiRaTA Avionics Stack

COTS

Custom

Custom
Final Design

Top Interface Board

<table>
<thead>
<tr>
<th>Sub-circuit</th>
<th>Driver</th>
</tr>
</thead>
<tbody>
<tr>
<td>Payload Power Distribution</td>
<td>Radiation Tolerance</td>
</tr>
<tr>
<td>Payload data transceiver</td>
<td>Radiation Tolerance</td>
</tr>
<tr>
<td>Magnetometer</td>
<td>Size, Cost</td>
</tr>
<tr>
<td>Beacon Radio Interface</td>
<td>Electrical Power</td>
</tr>
<tr>
<td>Primary Radio</td>
<td>Processing Power</td>
</tr>
</tbody>
</table>
## Bottom Interface Board

<table>
<thead>
<tr>
<th>Sub-circuit</th>
<th>Driver</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature Compensating Crystal Oscillator</td>
<td>Radiation Tolerance, Time</td>
</tr>
<tr>
<td>Inertial Measurement Unit</td>
<td>Electrical Power, Size</td>
</tr>
<tr>
<td>Thermal Knife Drivers</td>
<td>Radiation Tolerance, Cost</td>
</tr>
<tr>
<td>Coarse Sun Sensors</td>
<td>Electrical Power, Processing Power</td>
</tr>
<tr>
<td>Resistance Temperature Detectors</td>
<td>Processing Power, Cost</td>
</tr>
</tbody>
</table>
# Final Design

## Motherboard

<table>
<thead>
<tr>
<th>Sub-circuit</th>
<th>Driver</th>
</tr>
</thead>
<tbody>
<tr>
<td>PIC24 Microcontroller</td>
<td>Processing Power, Cost, Electrical Power, Memory</td>
</tr>
<tr>
<td>Micro SD card</td>
<td>Size, Radiation Tolerance, Memory</td>
</tr>
<tr>
<td>Flash Memory</td>
<td>Radiation Tolerance, Memory</td>
</tr>
<tr>
<td>Serial UART interface</td>
<td>Size, Complexity</td>
</tr>
<tr>
<td>Unregulated Power Port</td>
<td>Size, Complexity</td>
</tr>
</tbody>
</table>

**Diagram of the Motherboard**

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*Small Satellite Conference*

8/6/2015

Mic Byrne
MIT Space Systems Lab
## Backup Radio

<table>
<thead>
<tr>
<th>Sub-circuit</th>
<th>Driver</th>
</tr>
</thead>
<tbody>
<tr>
<td>CC1110 System-on-Chip</td>
<td>Processing Power, Size, Complexity</td>
</tr>
<tr>
<td>RF6504 Front End Module</td>
<td>Electrical Power, Size</td>
</tr>
</tbody>
</table>

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Final Design

Electrical Power System / Battery

- Highest single-cost component
- Smallest batteries still within mission requirements (20 Whr)
- Small size
- Self-regulated processing and telemetry
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Assessment

• Processing power sufficient for the needs of the mission

• Non-volatile memory sufficient to store 2 days of science data
  – 32x more memory than Pumpkin, 32x less memory than Proton

• Size Reduction
  – Decrease from 100-200cm\(^2\) to 70cm\(^2\) motherboard + 30cm\(^2\) backup radio

• Complexity minimization
  – Component reduction from Proton design by \(~200\%\)
  – Component reduction from Pumpkin design by \(~50\%\)

• Decrease in number of boards
  – From 6 in MicroMAS to 5 on MiRaTA

• Maintained power draw
  – Expected minimal decrease as compared to Pumpkin design

• Environmental durability
  – Tests indicate at least 24krad TID tolerance
Discussion

• Trade-off between size reduction, accessibility, and cost
  – If we use all 0201 components, last-minute fixes will be difficult

• Optimization will be different for each case
  – E.g., University vs industry budget, timeline, and resources
  – Hard to standardize

• Is there a “lite” avionics core that satisfies most use cases for the next 5-10 years?
  – Include common GPS, payload, sensor interfaces
  – Include some extra interfaces/capability (memory, reprogramming, better oscillators)
  – Include less common interfaces? Propulsion?

• What is the “just right” testing profile?
  – When is it better to build a bunch or sequentially, test on orbit?
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  - Hans Richter
- Planet Labs
  - Henry Hallam
  - Ben Howard
- Clyde Space
- Pumpkin Inc.
References


Questions?
Backup Slides
Final Design

PIC24 Microcontroller

2Gb Flash Memory

RBF Switch

Power (unregulated)

UART

Micro SD

Indicator LEDs

UHF Radio
<table>
<thead>
<tr>
<th>COTS</th>
<th>vs</th>
<th>Custom</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Pros</strong></td>
<td></td>
<td><strong>Pros</strong></td>
</tr>
<tr>
<td>• No development time</td>
<td>• Adaptable to the mission</td>
<td></td>
</tr>
<tr>
<td>• Low initial investment</td>
<td>• Full resource utilization</td>
<td></td>
</tr>
<tr>
<td>• User community</td>
<td>• Structural flexibility</td>
<td></td>
</tr>
<tr>
<td><strong>Cons</strong></td>
<td></td>
<td><strong>Cons</strong></td>
</tr>
<tr>
<td>• Unused functionality</td>
<td>• Higher initial investment</td>
<td></td>
</tr>
<tr>
<td>• Not designed with the future in mind</td>
<td>• Some development time</td>
<td></td>
</tr>
<tr>
<td>• Difficult debugging</td>
<td>• May not interface with other COTS devices</td>
<td></td>
</tr>
</tbody>
</table>
Durability: Space Radiation

**Total Ionizing Dose**: Long-term exposure to radiation that generates electron-hole pairs

**Displacement Damage**: Physical damage to materials caused by particle collisions

**Single Event Effects**: Unintended photoelectric events causing bit flips or other electron behavior in semiconductor logic
## Design Trade-Space

<table>
<thead>
<tr>
<th></th>
<th>FPGA</th>
<th>Microcontroller</th>
</tr>
</thead>
</table>
| **Processing Power** | • Parallel execution  
  • ~500MHz | • Real-time programmable  
  • ~50-500MHz* |
| **Memory**     | • Configurable RAM  
  • ~1 million gates | • Internal, pre-set size  
  • ~500kB ROM |
| **Electrical Power** | • ~50mW | • ~500mW |
| **Volume**     | • 0.5U PCB to support | • 0.5U PCB to support |
| **Cost**       | • ~$100 each | • ~$3 each |
| **Time**       | • Significant HDL training  
  • Lengthy development time | • Rudimentary C training  
  • Ready off-the-shelf |