Frontier Radio Lite: A Single-Board Software-Defined Radio for Demanding Small Satellite Missions

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ABSTRACT

Recent development by JHU/APL's Space Exploration Sector RF Engineering Group has led to a next generation, high-reliability, extremely low size, weight, and power (SWaP) software-defined radio (SDR) product for near and deep space applications called Frontier Radio Lite (FR Lite). A derivative from the TRL-9 Frontier Radio product implemented for the NASA Van Allen Probes (current), Solar Probe Plus, and Europa Clipper (future) missions, this evolution is a single card comprising the entire radio electronics system as opposed to four or more packaged slices. In addition to volume and DC power savings, this hardware was created with reconfigurability in mind. This paper discusses the research, development, challenges, and technology that enabled the jump to the FR Lite product as well as its capabilities and versatility to adapt to a multitude of different applications.

INTRODUCTION

The Frontier Radio is a TRL-9 SDR platform currently flying or to be flown on the following NASA Class A/B missions: Van Allen Probes (S-band), Solar Probe Plus (X/Ka-band), and Europa Clipper (X/Ka-band). While a highly capable and radiation tolerant, low-power, low-mass product, its four or more 4 x 6" packaged slices are still too large and power hungry for some highly resource constrained small satellite missions. This has spurred the development of a next generation configuration, called Frontier Radio Lite (FR Lite), which approaches the capabilities and reliability of the existing product, but with a fraction of the SWaP. This smaller, more efficient version occupies considerably less volume as a single 3.8" x 6" printed circuit board, resulting in a 75% mass reduction (Figure 1). Receive mode power has been reduced to less than 1.5 W, with a 0.35 W standby mode now available, and two-way coherent duplex mode of 4 W (including an onboard 1-W RF power amplifier). The improvements in SWaP mirror improvements in production time, cost, and reconfigurability as a single automated assembly pass can now complete the entire radio build without the complexity of further integration steps. As with the parent product, a modular architecture methodology is employed in hardware, firmware, and software to make reconfiguration a much simpler matter of selecting and combining existing modular blocks whether they are hardware component populations or firmware or software IP. The heavy use of up-screened commercial components allows the mission to select the cost/risk posture enabling FR Lite to target many mission classes. FR Lite prototypes currently exist in two design variants: a two-way radio operating at S-band (Figure 2), and an alternately-populated board operating as an L-band receiver for the GPS L1 & L2 bands. The

Figure 1: Comparison of the Van Allen Probes Frontier Radio (left) vs. FR Lite (right)

architecture supports additional variants operating in UHF through X-band, with options for adding Ka-band for missions that require it. Once FR Lite has been successfully flight qualified, APL will seek to transition the design to industry as part of its rich and successful technology transfer program.

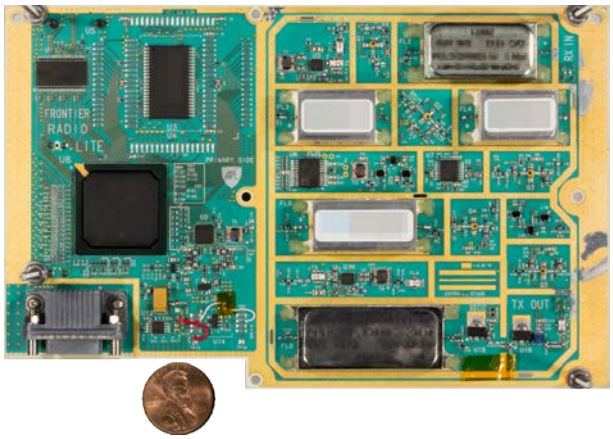


Figure 2: FR Lite primary side (no RF shields)

OVERVIEW

The Frontier Radio product family was born out of the successful development of a low-power, deep-space receiver for the New Horizons mission to Pluto[1]. This receiver saved approximately 12 W from the total mission power consumption (a mission enabler), was the first to fly Regenerative Pseudorandom Noise (PN) Ranging capability, and performed sensitive radio occultation and radiometer measurements of Pluto's atmosphere and surface with the integrated REX instrument. Performing communication, navigation, and radioscience in one radio was a significant advancement for deep-space systems. However, it was apparent that a lot more could be done by moving to a modular SDR architecture that could do these same functions, but for many different missions.

The first Frontier Radio was developed under a NASA grant. That specific unit targeted near Earth communication applications seeking 150-Msps Ka-Band downlink throughput capabilities. The SDR platform however was designed for a much wider set of applications. Key RF circuit components were identified and configured into adaptable blocks for multiple bands of operation (S, X, Ka, etc.)[2]. The digital processing platform was optimized for low SWaP, and made heavy use of commercial and custom processors embedded into ProASIC and RTAX family FPGA devices[3]. The embedded processors created significant opportunities for software-based manipulations of the communication, navigation, and radioscience waveforms.

The successful testing of this first design led to the development of the first flight unit for the Van Allen Probes mission to explore Earth's radiation belts. During this mission, significant effort was spent on refining the hardware design for manufacturing, and qualifying the SDR in a harsh radiation environment. This S-Band version of the Frontier Radio was the only radio—single string, onboard—and therefore had to meet very extensive requirements for radiation-induced events. Since launch in 2012, many radiation events have been detected and corrected (as expected and reported by telemetry), with seamless communications and mission operations throughout; this demonstrates the robust radiation handling capabilities of the Frontier Radio.

The Solar Probe Plus and Europa Clipper deep space missions are refining the main Frontier Radio product line further (Figure 3) for ease of manufacturing as well as new capabilities; Δ-DOR, LDPC encoding, 10-Mbps uplink, SpaceWire interface (networked), etc.[4] In parallel, the needs of other missions are continuing to diverge, resulting in the creation of new products in the family. As this divergence occurs, key components, common circuits, and modular firmware/software link the family together to quickly port fundamental blocks between units and to respond to adapting needs.

Figure 3: Flight Solar Probe Plus Frontier Radio

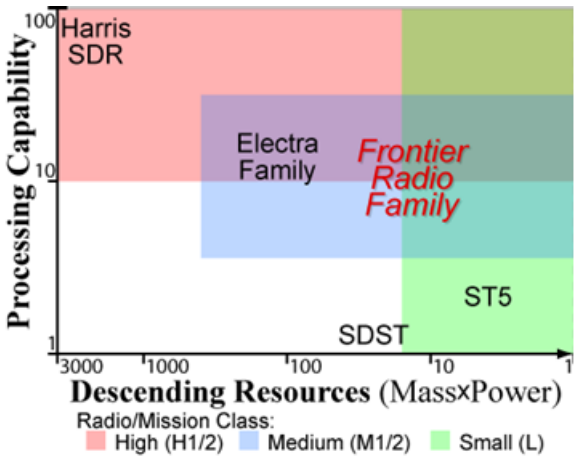
The Lite product is responding to the need for lower SWaP, while maintaining nearly all of the main product line capabilities. The capabilities listed in Table 1 show that most features are still available—especially since a similar capacity FPGA is used. However, maximum data rates and signal sensitivity have been reduced to achieve the low power consumption.

Table 1: Key performance parameters of Frontier Radio vs. FR Lite

Parameter	Frontier Radio	FR Lite	Unit
Frequency Band	S / X / Ka	UHF to C	
Volume	2050	320	cc
Mass	2.1	0.4	kg
Temperature	-35 to +60	-35 to +60	C
Power input	+28	+6 to +9	V
Power, Rx Only*	5	1.4 (0.35 Standby)	W
Power, Full Duplex, S-Band*	7 w/o SSPA (external)	2 w/o SSPA (onboard, 1W)	W
Rx / Tx Channels	2 / 2	1 / 1	
Receive Rate	1 - 1 M	100 - 10 M	sps
Transmit Rate	10 - 150 M	100 - 10 M	sps
Rx Sensitivity	-160	-150	dBm
Noise Figure (Integrated LNA)	2.5	3	dB
FPGA Device	RTAX4000	ProASIC3E 3000	
Interfaces	SpaceWire	SpaceWire	
Non-Volatile Memory Storage	2	2	MB
SRAM	1	0.5 to 2	MB
Radiation (TID)	100	20	krad
Radiation (SEL for LET)	>85	>85	MeV-cm^2/mg

*Frontier Radio with ovenized oscillator vs. TCXO on FR Lite.

Within the deep space radio market, the Frontier Radio product family occupies a unique territory defined by relatively light resource demands with a full spectrum of processing capabilities. Its position overlaps several mission capability/resource classes (Figure 4a) and stands out from other products as a resource bargain for processing power (Figure 4b).



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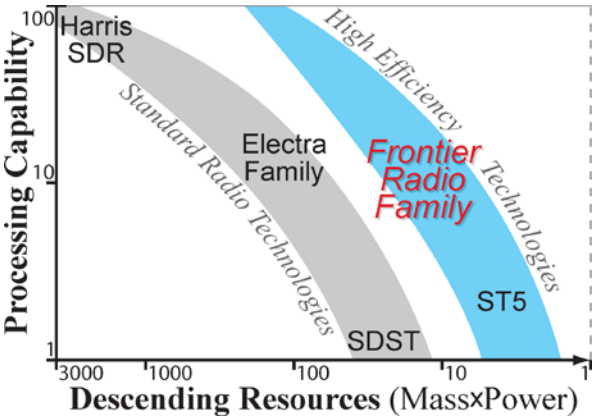


(b)

Figure 4: Frontier Radio & FR Lite market position

FPGA & FIRMWARE

The FPGA

Like the larger Frontier Radio, a core tenet of the FR Lite design is its use of a capable central FPGA for all processing and programmable logic needs. The FPGA's programmable logic allows the system architecture to be customized to the needs of the application while remaining responsive to changes in requirements well into the design cycle. These traits are critical for the FR Lite system, which must accommodate a wide range of communications links and spacecraft busses while remaining extremely power-efficient. FR Lite currently uses a 3-million gate re-programmable Microsemi RT (Radiation Tolerant) ProASIC3 FPGA, which is a departure from the Frontier Radio product that is based on a one-time-programmable Microsemi RTAX4000SL FPGA. While the RTAX has better radiation characteristics and can be procured at higher screening levels than the RTProASIC3, the ProASIC3's lower cost, physical size, and power consumption are a better fit for the design goals of FR Lite. Importantly, use of a re-programmable FPGA significantly lowers the cost of development and the final cost to sponsors by streamlining development and making the product more responsive to changes in requirements. FR Lite's spacecraft-facing connector includes the JTAG interface required to re-program its FPGA, which allows the firmware to be updated even late in the project after integration into the spacecraft, provided that the spacecraft has been designed to support that capability.

IP Reuse

Typical mission development flows have concurrent development of hardware, firmware, and software. This is driven by each mission being customized to optimize SWaP or to meet one or more new/unique mission requirements. The Frontier Radio product family takes

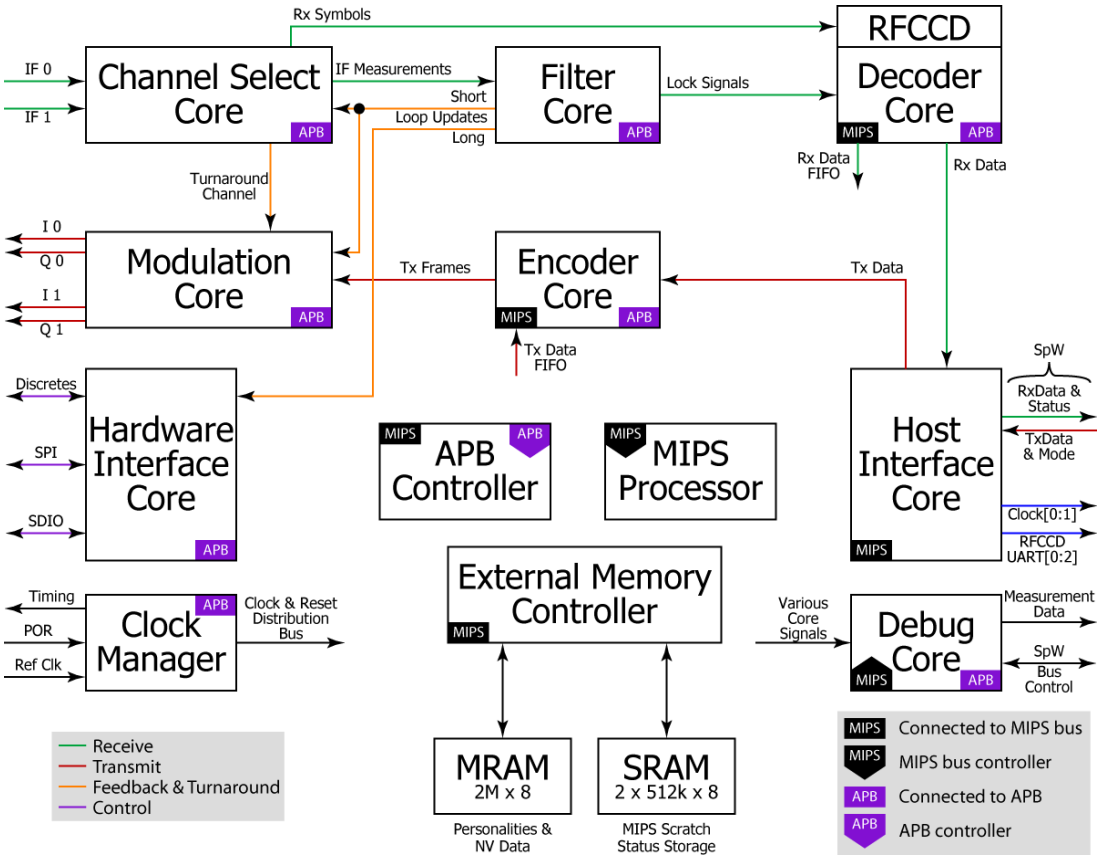


Figure 5: Representative block diagram of the Frontier Radio firmware architecture, including external memory

a different approach, building each mission-specific implementation on a strong foundation of reusable, customizable IP blocks, requiring firmware development on only the small subset of new capabilities required by each specific mission. This saves cost not only by amortizing the cost of firmware development across multiple missions, but also by allowing firmware development to complete early in the design cycle, providing a stable foundation for software development and system test.

Firmware Architecture

Figure 5 shows an example instantiation of the Frontier Radio firmware architecture and the modular blocks that comprise the IP. These blocks (and others) are populated and depopulated from designs as necessary per mission requirements. This firmware architecture along with its component IP modules have been successfully deployed on NASA's Van Allen Probes mission and have supported several technology demonstrations, and will be used for multiple upcoming flight missions including NASA's Solar Probe Plus mission, scheduled to launch in 2018. This processing architecture within the FPGA and the critical design trades that define it have been described in detail in other work[3]. Only relatively minor changes are required to the Frontier Radio architecture to allow it to function on FR Lite, owing to the Frontier Radio team's emphasis on modularity and efficiency during implementation.

HARDWARE & RF

SWaP Reduction

Several key factors enable the size decrease from the existing Frontier Radio to the FR Lite design. Chiefly among them are several sections of analog hardware transitioning to firmware. The largest sections of hardware absent from the FR Lite design are a second frequency conversion stage in the receive and transmit circuits. Previous limitations on the speed of analog-to-digital converter (ADC) and digital-to-analog converter (DAC) components required intermediate frequencies (IFs) in the ones to tens of MHz. To get there from multi-GHz RF waveforms required multiple frequency conversions with a several hundred MHz IF in between. However, high-speed digitization is now enabled by ADCs and DACs that were qualified for the parent

product on previous missions. Taking advantage of the full capabilities of these parts, in conjunction with undersampling in the receiver, and selecting a high frequency DAC image in the transmitter, allows the final/initial low-frequency conversion to take place in the digital domain of the FPGA.

Two other circuits eliminated from the FR Lite parts list are the direct digital synthesizers (DDS) for fine frequency tuning and the modulator for the transmitter. The modulator in the parent Frontier Radio is a separate IC with a large amount of support circuitry (transformers, biasing resistors, protection diodes, bypassing). It operates at S-band and is excited by baseband signals from the FPGA. By comparison, the FR Lite modulator is in the FPGA itself and operates at the transmit baseband frequency (roughly 50 MHz), eliminating most of the circuitry's power and area requirements. The DDS circuits missing from the FR Lite receiver and transmitter hardware are implemented with an external DDS chip on the parent product. In its receiver, the DDS output is frequency mixed into the downconversion, counteracting frequency drift and creating a static IF for digitization. In the FR Lite case, drift in received frequency is accounted for after digitization by use of a DDS within the FPGA.

Optimizations also occurred in the hardware design. For both frequency up- and downconversion, a single frequency synthesis circuit serves as the local oscillator (LO) source (see Figure 6). Traditionally, each frequency conversion chain would have its own tunable LO source for independent operation. Such a circuit contains a synthesizer chip to control the Phase-Locked Loop (PLL) and Voltage-Controlled Oscillator (VCO). The synthesizer IC, support circuitry, and especially the VCO demand significant power and board-area resources. By sharing these components, the SWaP required for LO generation is cut in half. The drawback is an interdependency between the receive and transmit IFs. That is, there is one less knob to turn to get the front-end RF frequencies converted down to/up from the desired IF where the digital domain transition occurs. However, IF filter selection at the time of manufacture along with the tunable range of the firmware DDS's sufficiently compensate for the loss of independent control at the LO.

RF Design Challenges

Self-interference is the number one concern in implementing a highly sensitive receiver in close proximity to a relatively high power transmitter, a full suite of digital signal processing electronics, and switching power supplies. Beyond these 'outside' sources, within either the receiver or transmitter, wrapping a sequential chain of high-gain amplifiers around itself to compact it into a small area creates the potential for oscillations as the output of one amplifier couples back to the input of another. Many methods were employed to tackle these problems such as segmented ground planes (separating RF circuitry from digital) and careful consideration in component placement. However, the most critical step was compartmentalizing every RF sub-circuit (e.g. each mixer, amplifier, filter, etc.) inside of metal shields.

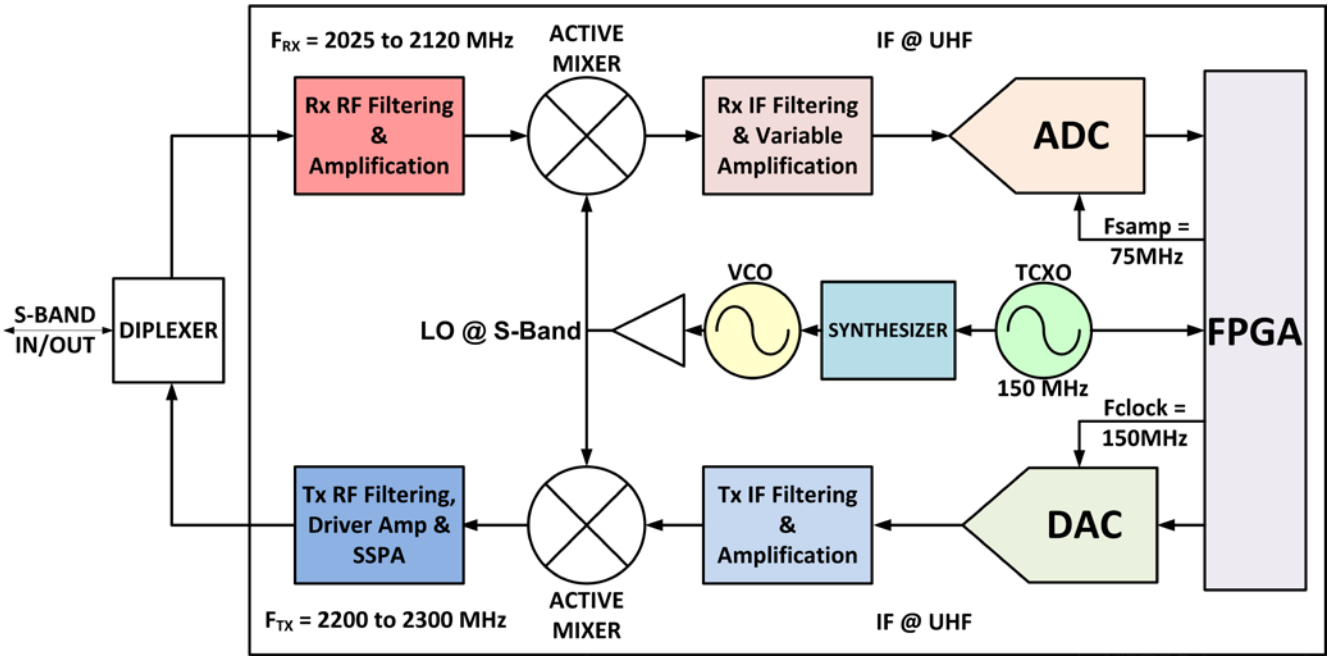


Figure 6: FR Lite simplified block diagram

These shields were custom designed to fit the layout after initial placement (they are visible in Figure 3 and Figure 7 as the gold tracks throughout the left side of the board). Not surprisingly, initial bench testing of the first unit revealed a significant oscillation generated by the close proximity of the high gain IF amplifiers in the receiver. However, when the RF shielding was soldered into place, this instability was eliminated. Further, installation of the shields attenuates interferers from elsewhere on the board (transmitter, switching supplies, digital clocks, etc.). This is confirmed when examining performance with and without the shield lid installed.

Trades and Process

The intrinsic mixed mode nature of the FR Lite design and the careful balance of proper implementation and guards against interoperability issues between sub-circuits had a heavy influence on the board stackup and component placement. In an attempt to make the design flexible for various mission needs and configurations (such as flight vs. prototype configurations), several multi-footprint parts were designed into the layout. Also, to minimize the risk of latent cross talk and signal integrity issues, extensive board design simulations in Mentor Graphic's HyperLynx were conducted and iterated upon prior to fabrication.

As the design contains both dense digital signals (typically routed on a multi-layer polyimide board) and RF signals (typically routed on a low loss material) a compromise was made between RF performance and feasibility of digital routing. The result is an eight-layer Rogers 4350B/4450B + FR4 core stackup that allows enough room for routing digital signals while still providing a low loss tangent for RF microstrip and stripline interconnects.

Layout of the board was primarily driven by the need to isolate RF, digital and power functional groups to prevent self-interference. This resulted in the segmented layout as shown in Figure 7. The digital circuitry is contained exclusively to the left while the RF components are laid out almost entirely on the right of the primary side (a). The receiver chain components are the top three rows of shielded compartments and the transmit chain is in the bottom three rows. The shared LO is placed on the secondary side (b) between the transmit and receive paths for ease of distribution and is also shielded. High-efficiency switching power supplies and LDOs were placed on the secondary side for isolation.

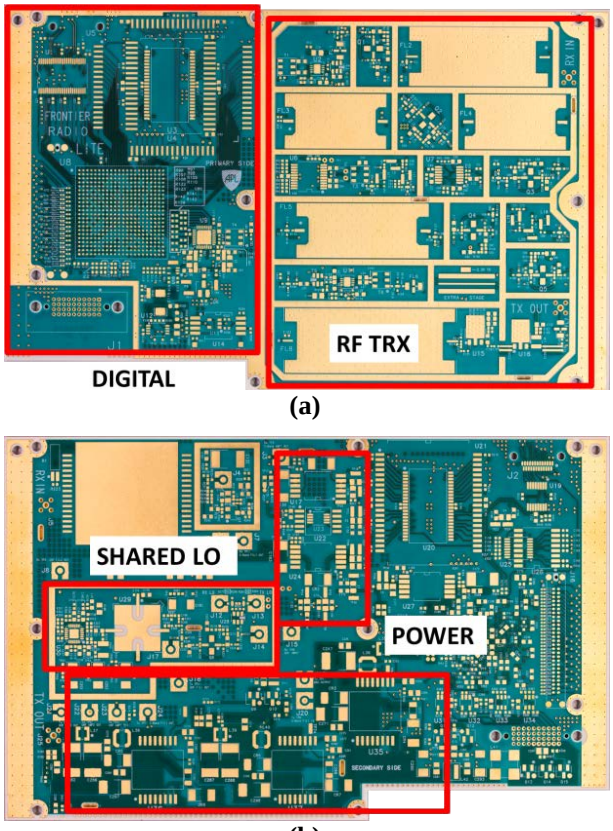


Figure 7: FR Lite bare board (a) primary side showing digital & RF sections and (b) secondary side circuit sections

To achieve flexibility of multiple design variants, the use of multi-footprinting is employed in the design to incorporate flight and prototype parts. The example in Figure 8 shows a triple footprint in the design that allows the population of a prototype 8-bit and flight 8-bit and 32-bit SRAM chips, all sharing common data, address and control lines.

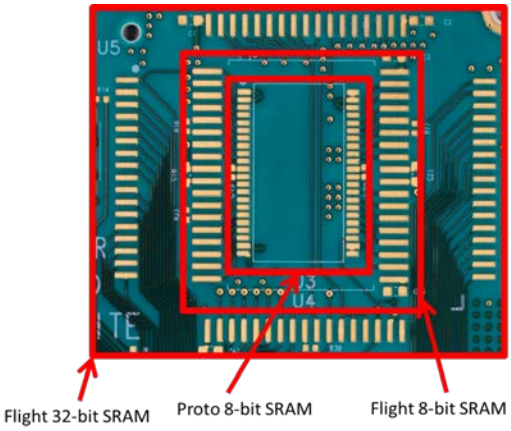
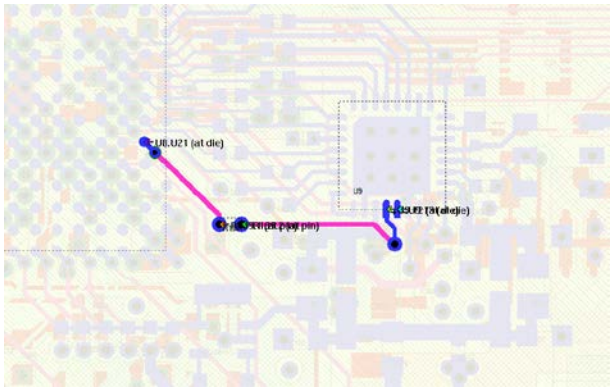


Figure 8: Triple-nested footprint for SRAM packages

Prior to board fabrication, post-layout simulations were conducted using HyperLynx. This allowed signal integrity verification for critical nets such as clocks and control lines while also identifying potentially disruptive crosstalk aggressors. An example parameter swept simulation of a digitizer clock line is shown in Figure 9. The simulation environment provided a quick way to experiment with various routing topologies and termination approaches, allowing rapid iteration towards a design that had a high probability of successful operation on the first revision. And indeed, testing has confirmed expected results.



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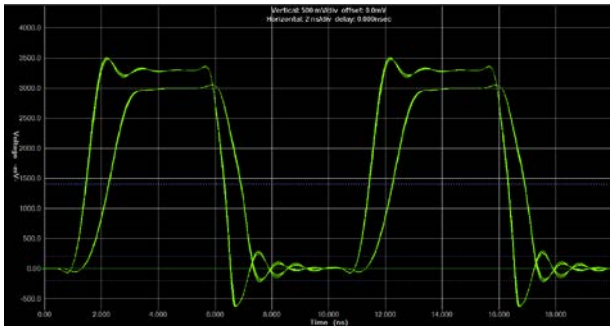

(b)

Figure 9: HyperLynx model of an example trace's (a) layout view and (b) simulated time-domain response

AN ADAPTABLE DESIGN

The ability to tailor this design to meet the needs of many different missions that require an array of modulation schemes and target frequencies is a critical feature of FR Lite. Implementing different communication standards is an inherent capability of an SDR such as FR Lite, however the use of modular firmware and software blocks enable rapid and reliable adaptations to new requirements. At the component level, the active devices are capable of wideband operation while the circuit designs allow for wide frequency tuning ranges with little to no modifications. When necessary, only small passive parts are replaced with footprint-compatible values to achieve tuning. Passive filters can be swapped out for footprint-compatible units to target different center frequencies and bandwidths. The large footprint of the ceramic S-band filters means higher frequencies are achievable, as component size decreases inversely with frequency. Lower frequency filters can be (and have been) implemented with less area by using discrete, passive components in place of the ceramic filters.

This design's versatility has already been proven with an adaptation of the S-band transceiver into an L-band receiver for GPS and other global navigation systems. By replacing the filters and updating impedance matching circuits (just minor changes of some passive component values), the existing PCB was populated to allow it to operate at different RF and IF frequencies. In total, design time of less than two weeks was spent in determining the new values and components. Because the PCB required no changes and copies were already on hand, the only other steps were to order parts and perform the assembly. In less than one month from the request for the design, a fully populated board was on the bench and under test. The following section further details this example.

RECONFIGURED DESIGN FOR NAVIGATION

The current generation of APL's GPS-based orbit determination system was designed primarily for NASA's TIMED mission[5], which has been operating in orbit for 15 years. TIMED's relevant capabilities are listed in Table 2. Its receiver had 12 satellite tracking channels, a GPS time-aligned one pulse per second (PPS), better than 15-meter real-time orbit position accuracy, a set of autonomous event-based commands, and, in the vernacular of the GPS community, it was always in a warm-start mode due to the onboard orbit determination. These capabilities are still impressive after 15 years of GPS receiver technology and algorithm improvement, and the performance exceeds many of the requirements of most current satellite missions. The primary drawback of the TIMED design, from the present-day perspective, is its SWaP. For example, TIMED's processor board area was 6"x9" (Figure 10, left), and that does not include two other critical components: the RF down-conversion chain and GPS Tracking ASIC (GTA).

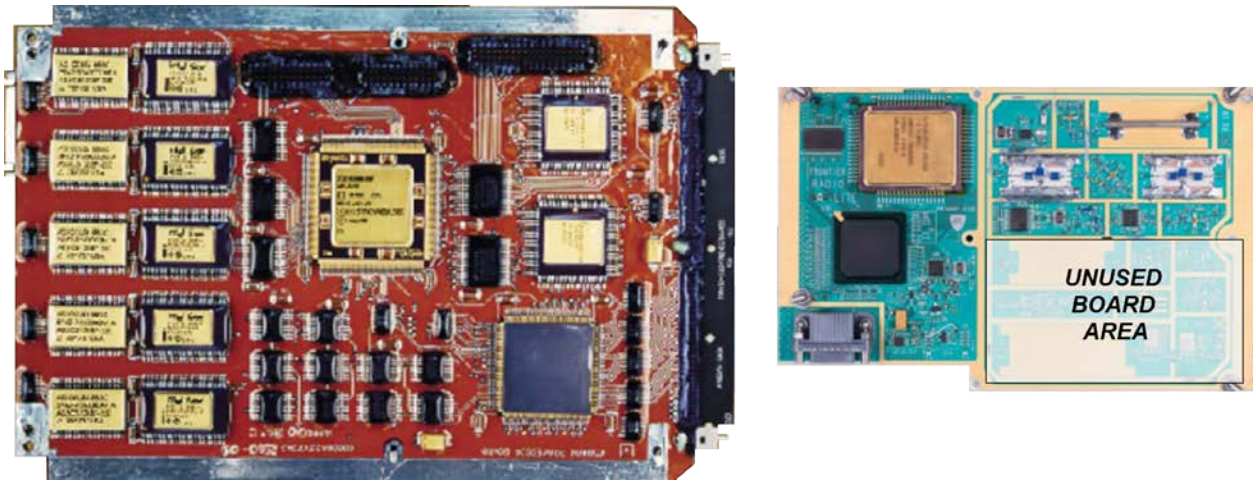

Figure 10: Size comparison of (left) NASA TIMED Mission's processor board (circa 2000) vs. (right) EGNS board (re-populated FR Lite board)

Table 2: Key performance parameters of NASA's TIMED GNS board and the new EGNS board

Key Performance Parameter	TIMED	EGNS
Number of Channels	12	12
Pulse/Second Accuracy	85 ns	20 ns
Warm-Start Time	1-2 min	1 min
Cold-Start Time	12 min	1 min
LEO Positioning Accuracy	15 m	15 m
Event-Based Commanding	Yes	Yes
Second GPS Frequency (L2C)	No	Yes
Combined GPS/OD Option	No	Yes

The primary goal of a recent internal R&D effort was to realize significant SWaP improvements for APL's onboard spacecraft orbit determination solution using the new design from FR Lite. The FR Lite board was re-populated with some modifications for the GPS implementation and renamed the Extensible Global Navigation System (EGNS) board (Figure 10, right). The components of the frequency down-conversion chain were swapped with those suited to the GPS L-bands:1.57542 GHz (L1), and 1.2276 GHz (L2). Additionally, the processor core was upgraded from a MIPS processor to a LEON3 processor and the 512 kB memory part was swapped for a 2MB part. The memory chip swap had only a minor impact as the FR Lite board was designed with a triple-nested footprint to accommodate several different memory components. The increased memory, more capable processor, and additional FPGA space to accommodate a floating-point unit, allow this board to take on the computations of the orbit determination Extended Kalman filter from TIMED. When the EGNS board executes the orbit determination code, it effectively takes the place of the secondary command and data handling processor on TIMED, further improving SWaP savings. The 6"x3.8" area of the EGNS board is nearly a 60% size reduction from the TIMED processor board and it now includes the RF down-conversion chain, GTA, and possibly the orbit determination code. The LEON3 processor and the GTA are contained in the single FPGA.

Reuse of the common architecture saves a significant amount of non-recurring engineering costs, but it naturally leads to a sub-optimal design. In this realization, FR Lite's transmit chain is unpopulated (bottom right 1/3 of the board in Figure 10, right) and thus the board is not fully area efficient. However, this area could be populated for additional capabilities (e.g., crosslinks, tracking other frequency signals, etc.) or a new board could be created that is more area-optimal from the EGNS perspective, if a sponsor required it.

A list of the EGNS board's specifications are shown in Table 3. The power draw is low and can be made lower based on the customer's desired EGNS duty cycle rate. The board can be heavily duty-cycled (turn the whole board off and back on) because spacecraft typically experience perturbing forces that are negligible over a short period of time, and thus a converged orbit solution requires infrequent GPS measurements. SpaceWire is the modernized interface to the main spacecraft processor, but other interfaces could be accommodated. The radiation tolerance is limited by the current FPGA, but the firmware LEON3 processor has internal memory scrubbing and the software has built-in receiver autonomous integrity monitoring (RAIM) capabilities that detect if serious errors have occurred. If an error does occur, the measurement can be ignored in some cases, and in others, the board can detect it and notify the main processor to power cycle the EGNS.

Table 3: EGNS Specifications

Parameter	Value
Volume	15.2 x 9.7 x 2.21 cm (0.33 U)
Board Mass	0.4 kg
Average Orbit Power	~0.5 W (duty-cycle based)
Instantaneous Power	0.35 W (stand by) 1.3 W (peak)
Data Interface	SpaceWire
Added Parts	Antenna, C&DH CPU (OD)
Radiation Tolerance	20 kRad + RAIM + SEU Protection

The capabilities developed on TIMED have been re-instantiated in new hardware, firmware, and software using the same board design as FR Lite. The reuse of a pre-existing board design greatly advanced the EGNS development cycle and kept engineering costs down. Massive SWaP improvements have been realized and the system has been modernized to meet current standards. Flexibility has been added to suit sponsor desires by using an FPGA instead of a fixed circuit design. The EGNS design is continuing to evolve on internal funding, and the final target capabilities are listed in the third column of Table 2.

SUMMARY AND FUTURE WORK

Component count reduction through newly available components coupled with reuse and innovative electrical and mechanical design techniques are enabling the next generation of space radio hardware. This radio design makes significant improvements in size, weight, and power at a lower cost and with faster development cycles without sacrificing capability or its high-reliability heritage. In addition, a library of modular, reusable firmware and software IP allow rapid adaptation of the SDR to meet the needs of a vast array of communication schemes.

Frontier Radio Lite fills out a family of three radio products that cover nearly every high-reliability application. FR Lite covers the most power and mass constrained missions with few compromises. While highly capable, it is geared toward higher risk, faster schedule mission classes. As such, missions with the lowest risk tolerance, longest mission durations, or most extreme radiation environments remain a job for the existing Frontier Radio—a flight proven, high throughput, extremely robust system. However, future work will enable even missions with the most demanding requirements and environments to fly with a smaller form factor product. Through ongoing internal R&D efforts, yet another permutation is evolving as a single-board computer (SBC) + RF card. Both cards in the same form factor as FR Lite, the RF card serves as the RF front end to the SBC and enables it with radio capabilities. The design will be reconfigurable for different combinations of transmit and receive chains at any frequency from UHF up to X band through component changes (and even Ka band with a small external module). The SBC + RF Card will be a leap forward in reduction of SWaP, with more processing power than and nearly as robust as the heritage Frontier Radio product. Its past, present, and future development demonstrates FR Lite's promising path forward for very high reliability, extremely low SWaP and low NRE space radio systems from JHU/APL.

Acknowledgments

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