Road Map

- Introduction

- Research Overview – Focus Areas
  - Heritage Method Deficiencies
  - Process Improvements

- Verification Methods
  - Component Level
  - System Level

- Future Work

- Conclusion

TBEx satellite CAD model
INTRODUCTION
BACKGROUND

- Solar Panel Lead, Michigan Exploration Laboratory
  - Characterize cells
  - Fabricate & test panels

- Fabricated solar panels for 3 institutions & missions:
  1. **MXL**: CADRE
  2. **CU-Boulder**: QB50
  3. **LASP**: MinXSS, Flight Model 2

- Surveyed common practices → identified areas of improvement

CADRE Flight Model
RESEARCH OVERVIEW
Research: Objective

Goal: Synthesize and refine best practices and procedures for solar panel fabrication to increase subsystem reliability and efficiency
– Target mission: MXL’s TBEx (delivery May 2017)

Focus areas:
– Solar cell tabbing
– Solar cell stringing
– Solar cell adhesion to PCB substrate
– Solar cell coverglass application
Research: Outcome

- Process improvements: increased **reliability, yield, and manufacturability** of solar panel subsystem
  - Reliability: key to use of CubeSats as meaningful tools of science
  - Single-day fabrication: can accommodate tight build schedules
  - To be implemented on MXL’s TBEx mission

*TBEx proto-panels incorporating proposed procedures*
CELL TABBING
Heritage Deficiencies and Process Improvements
Solar Cell Tabbing: Background

- **Cell type:** EMCORE Multi-Junction BTJM, bare
  - Require in-house integration of tabs and coverglass
  - Produce ~1 W per cell (nominal)
  - Bypass diode: prevents cell damage in case of shadowing
  - “M” interconnects: connect cells in series
Solar Cell Tabbing: Deficiencies

- **Low cell yield**
  - Multiple heating cycles (hot plate, reflow gun, soldering iron) → high incidence of cell shorting (10% rate per batch)

- **Required excess time**
  - ~10 min/cell

- **Required excess manpower**
  - 2 fabricators required

- **Required risky elements**
  - Weights on cell faces increased risk of cell fracturing
Solar Cell Tabbing: Improvements

- **High cell yield**
  - Decreased required heating cycles → shorting rate: reduced by 70%

- **Reduced tabbing time**
  - ~10 min/cell to ~3 min/cell

- **Reduced manpower**
  - 1 fabricator required

- **Eliminated risky elements**
  - No pressure on cell faces required
CELL STRINGING
Heritage Deficiencies and Process Improvements
Cell Stringing: Background

- Cells connected in series
  - Smaller power loss => more efficient
    \( P = I^2R \)

- Heritage: cells connected via direct soldering
  - Tabs connect negative pads with positive backside of adjacent cell
  - Design justification: maximize # of cells per PCB

CADRE deployable and body panel
Cell Stringing: Deficiencies

- **Difficult** to manufacture
  - Soldering directly to backside of cells → increased handling and incidence of shorting

- **Difficult** to repair
  - Difficult to de-integrate damaged cells → risk damage to other cells

- **Limited** cell orientation
  - Only vertical

CADRE deployable cell string
Cell Stringing: Improvements

- Easy to manufacture
- Easy to repair
- Versatile cell configuration: horizontal and vertical

Side-by-side comparison of decoupled panel (left) and heritage CADRE panel (right)

TBEx deployable, requires versatile cell placement
CELL ADHESION
Heritage Deficiencies and Process Improvements
Cell Adhesion: Background

- Heritage: cells adhered to PCB with silicon epoxy
Cell Adhesion: Deficiencies

- **High risk** of voiding
  - Uneven adhesive application → adhesive voiding → outgassing → panel damage

- **Lengthy** assembly time
  - Application time: 30-45 min/panel
  - Cure time: 4 hours

- **Prevented** cell de-integration

- Involved **extensive cleanup**

- **Required** **high costs**
  - $300 to populate 6-8 PCBs
Cell Adhesion: Improvements

- **Lower risk** of voiding
  - Demonstrated by IR data

- **Short** assembly time
  - Application time: 15 min/panel
  - Cure time: 0 hours!

- **Enabled** cell de-integration

- **Minimized** cleanup

- **Decreased** costs
  - $45 to populate 8-10 PCBs

*Infrared imaging comparison of cell adhesion with epoxy (left) and Kapton tape (right)*

*De-integrating damaged cell from panel*
COVERGLASS
Heritage Deficiencies and Process Improvements
Coverglass: Deficiencies

Heritage:
We didn’t have a procedure!

- Coverglass desirable because it:
  - Physically protects cells
  - Decreases cell degradation due to UV radiation, atomic oxygen degradation and high-energy particle radiation*

Coverglass: Improvements

- Developed **simple, robust procedure**
  - EPM 2420 Low Volatility General Purpose Silicon Adhesive
  - Application time: 5 min/cell
  - Curing time: 1 hr @ 65C
  - Resulted in power loss of < 2%

![Applying coverglass to cells with EPM 2420 Silicon Adhesive](image)
VERIFICATION METHODS

Component Level
Electroluminescence (EL) Testing

- Visual assessment of cell health
  - Dark regions: diode damage
  - Shorted cells: no electroluminescence

- Supplies voltage to cell in forward bias configuration

- Performed: post-tabbing, post-stringing, and post-integration onto PCB
Illumination Testing

- Characterization of cell performance in on-orbit luminosity conditions

- Measures current produced from cell when exposed to “sun-like” light source
  - Generates IV-curve $\rightarrow$ calculates max power

- Performed: post-tabbing, post-stringing, and post-integration onto PCB
Infrared Testing

- Non-invasive method of detecting adhesive voiding
- Photo-documents heat dissipation in panel
  - Monolight flash = uniform heat source → air pockets (voids) dissipate heat more slowly → visible “hot spots”
- Performed: post-integration
VERIFICATION METHODS

System Level
Vibration Test: Background

- Two panels of six cells tested:
  1. With coverglass
  2. Without coverglass

- Performed: post-integration

- Panels on test pod → accelerometers on panels

- Tests run:
  - Sine sweeps: characterize resonant frequency
  - Random vibration: simulate launch conditions (11 and 22.5 G_{rms})
Vibration Test: EL Analysis

- No panel-wide structural debris/damage produced

Top Cell: Coverglass Panel
- EL testing reveals damage to cell with coverglass. Damage attributable to test set-up failure.
- Cause:
  - Test set-up failure. Accelerometer impacted cell face.
  - Coverglass prevented debris production

Top Cell: Non-Coverglass Panel
- EL testing reveals damage to cell without coverglass. Cause unknown.
- Cause:
  - Unconfirmed. Hypotheses:
    - Cell mishandling prior to vibe
    - Cell voiding near tabs
  - Requires further testing
Vibration Test: Illumination Analysis

- Confirmation of damage: 1 cell/panel
  - Step-like feature: indicative of bypass diode activation
  - Power output: ~1 W lost

Illumination Analysis

Post-vibration IV-curve, coverglass panel

Power Analysis

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AIAA/USU Conference on Small Satellites

Sandberg
Thermal Vacuum Testing

- Results: Panels survived with 0.01W loss in power \(\rightarrow\) negligible

- Same test panels as vibration testing
  - Cells with damage replaced \(\rightarrow\) demonstration of de-integration feasibility

- Test conditions
  - Eight thermal cycles
  - Temperature: -45C to 60C
  - Vacuum: \(1 \times 10^{-6}\) torr
FUTURE WORK
Future Work

- Resolve non-coverglass cell fracturing cause
  - Observed post-vibration testing

Plan:
1. Construct design model of solar subsystem for TBEx (using same “as-built” procedures)
2. Subject panel to same vibration conditions
3. Assess reproducibility of damage
CONCLUSION
Conclusion

- Process improvements: increased **reliability**, **yield**, and **manufacturability** of solar panel subsystem
  - Reliability: key to use of CubeSats as meaningful tools of science
  - Single-day fabrication: can accommodate tight build schedules
  - To be implemented on MXL’s TBEx mission

*TBEx proto-panels incorporating proposed procedures*
Acknowledgements

- Dr. James Cutler: Michigan Exploration Laboratory Director
- Dr. Tim Smith: Faculty Advisor
- Emanuela Della Bosca, Brian Shaw, Gregorio Lopez, and Andrew Plave: Fabrication and test assistants
- Andrew Dahir: CU-Boulder QB50 Project Manager
- James Mason: LASP MinXSS Project Manager
BACK-UP SLIDES
Tape Integration Work Flow

Integrating cells with Kapton adhesion method
Why Do We Need Bypass Diodes?

- Bypass diodes prevent panel damage in case of shadowing

Shadowing scenario. Credit: PVEducation.

- Shadowed cell “current limits” string → excess power dissipates in shadowed cell, damages string
  - Bypass diode provides alternative current path
The Scoop on Solar IV-Curves

- **Open-circuit voltage** \((V_{oc})\): max voltage, array not connected to load
- **Short-circuit current** \((I_{sc})\): max current, output connectors shorted
- **Max power point**: \(I_{mp} \times V_{mp}\), normal operating conditions
- **Fill factor**: relationship between max power under normal operating conditions and \(V_{oc} \times I_{sc}\)
  - Reflects quality of array

*Credit: Alternate Energy Tutorials*
More Future Work

Resolve cell warping around side tab
- Observed post-vacuum bagging
- Suspected cause: localized height offset due to stacking of side tab on Kapton → potential voiding vulnerability

Possible remedy: cut away Kapton beneath tab
- Plan: Prepare & examine sample panel
Sneak Preview

Test panel with Kapton cut away beneath side tabs