Model Based Design and Auto Coding of an FPGA Based Satellite Control System

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What is Model Based Design?

Model-Based Design

- Supervisory Logic
- Algorithms

IMPLEMENTATION

- C, C++
- VHDL, Verilog

INTEGRATION

RESEARCH

REQUIREMENTS

TEST & VERIFICATION
Traditional design process

1. An expert creates a high level computer simulation: Control system, commutation, etc.

2. Engage with a firmware developer/expert to code model to FPGA hardware.

3. Lots of back and forth between these two experts.
FPGA Implementation

- Simulink is often used to model the spacecraft system
- Instrument control
- ADCS subsystem
- The programmer often creates diagrams of the FPGA functionality required
- Text entry of the system in a descriptive language like HDL
- Synthesis tools take HDL code and place on an FPGA
Model Direct Implementation

Model Based Auto coding

1. Expert creates a model.
2. Expert generates FPGA code from model.
3. Expert deploys code to hardware.
4. Expert confirms that model is working properly on hardware.
Why FPGA for Small Sats?

- Ease of Parallel and real time processing.
- Low power.
- Radiation Tolerance.
- Advanced Computational Capabilities.
Simulink/HDL Coder

- Simulink
  - Block level design
  - Arithmetic functions (filters, FFT’s)
- State flow
  - Logic flow (if then else)
  - State Machines
- HDL Encoder
  - Auto codes both to HDL
HDL Coder Blocks
Where we are using this process

ADCS

Ion Drift Meter
Ion Drift Meter Hardware

- FPGA Microsemi Igloo
- Control Instrument
- Packetizes Data

Ion Drift Meter
- Designed to measure currents down to femto amps
The Drift Meter Simulink Model

Uart Controller and Command Parser

Data Packetizer and Uart Output
Inside Look at the DDC FSM

DDC Chart

State Flow Diagram
LIBRARY IEEE;
USE IEEE.std_logic_1164.ALL;
USE IEEE.numeric_std.ALL;

ENTITY DDC_FSM IS
PORT ( clk : IN std_logic;
reset : IN std_logic;
DATA_IN : IN std_logic;
DATA_VALID_L : IN std_logic;
DDC_side : IN std_logic;
start : IN std_logic;
bits : OUT std_logic_vector(70 DOWNTO 0);-- ufix80
CONV_DONE : OUT std_logic;
DCLK : OUT std_logic;
CONV_Out : OUT std_logic_vector(7 DOWNTO 0);-- uint8
CONV_CNT : OUT std_logic_vector(31 DOWNTO 0);-- uint32
);
END DDC_FSM;

ARCHITECTURE rtl OF DDC_FSM IS
Outputs From Scopes

Simulink Scope

Bit Scope
Synthesized Model
Results

- We were able to use Simulink and HDL coder to talk to low level hardware.
- We were able to use Simulink to quickly generate HDL code to packetize our data.
ADCS

- Full simulation of Attitude Determination and Control System
- Full orbit simulation of ADCS
- Hardware in the loop
ADCS Model
Conclusions

- A really good option for faster development
- Produces well optimized HDL Code
- Self Documenting
Questions?