Iris Deep-Space Transponder for SLS EM-1 CubeSat Missions

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ABSTRACT

Several key design upgrades have been recently made to the Iris Deep-Space Transponder baselined to be used on secondary payload missions of the upcoming Space Launch System Exploration Mission One (SLS EM-1). The Iris Transponder is a reconfigurable software-defined radio (SDR) designed for missions requiring interoperability with NASA's Deep Space Network (DSN) on X-band frequencies (7.2 GHz uplink, 8.4 GHz downlink). The transponder provides radiometric tracking support with the DSN to provide navigational products for precise orbit determination while performing standard uplink and downlink communications in a CubeSat/SmallSat-applicable package size. The recent hardware changes include a volume reduction of 30% from previous models, with the main transponder unit weighing less than 1.0 kg, while maintaining total ionizing dose (TID) radiation tolerance of >23 krads (Si) for deep-space missions. Lab tests indicate maximum downlink rates of up to 6.25 Msps can be supported by the transponder in conventional BPSK modulation, but most SLS EM-1 CubeSat missions are link-performance limited to less than 256 kbps. A prototype unit of the flight production units has been assembled and various performance and characterization tests are underway. This talk discusses the key design aspects and specifications of the Iris Transponder and presents preliminary results from early testing of the assembled transponder.

INTRODUCTION

A new class of CubeSat missions aiming beyond Low Earth Orbit (LEO) are on the rise to explore and provide valuable new science data from the moon and beyond. A key device that enables such lunar and deep-space missions is a deep-space transponder capable of providing the traditional telecommunications features, and also provides radiometric tracking support for orbit determination outside the effective range of Global Positioning System (GPS) satellites. The Jet Propulsion Laboratory (JPL) developed the Iris Transponder as a new product line to support such CubeSat/SmallSat missions starting with the INSPIRE mission,[1] and further developed and matured for the Mars Cube One (MarCO) mission to Mars.[2]

CubeSat concept missions are now shifting from teaching tools and technology demonstration missions to missions with clear science goals to fill strategic knowledge gaps[3]. Several secondary payloads of the upcoming Space Launch System Exploration Mission One (SLS EM-1) launch are in development to explore the moon in search of water and ice, and others are in development to explore asteroids, characterize space weather, and investigate the biological effect of space radiation using yeast. Table 1 depicts the concept missions that have baselined the Iris Transponder as their main telecom and navigation unit, along with their destination and maximum topocentric range along its trajectory.

Table 1: SLS EM-1 CubeSat Missions with Iris

Mission Name	Destination	Max Range
LunaH-Map	Lunar	~1 Mkm
Lunar IceCube	Lunar	~1 Mkm
Lunar Flashlight	Lunar	~1 Mkm
Cubesat for Solar Particles	Heliocentric	~15 Mkm
BioSentinel	Heliocentric	~84 Mkm
Near Earth Asteroid Scout	Asteroid	~180 Mkm

Some design updates have been made to the Iris Transponder, making it the 3rd generation transponder (V2.1 shown in Figure 1) in order to support the various EM-1 secondary payload missions. Such updates will be discussed in this paper along with current test data from the various performance and characterization tests underway.

Figure 1: Iris V2.1 Transponder Stack

IRIS ARCHITECTURE

Iris is a Software Defined Radio (SDR) based on other JPL radio products like the Electra Proximity Radio[4] and the Universal Space Transponder (UST)[5]. The rapid development of Iris is aided by direct inheritance of the majority of previously-flown firmware signal processing algorithms like tracking loop algorithms, forward-error correction channel coding schemes, error detection and correction (EDAC) modules, and the phase shift key (PSK) modem. The modular radio architecture allows configuring the radio for mission-specific needs with interchangeable RF front-end slices. The EM-1 units are all configured for DSN interoperability in the X-band Space Research frequencies occupying 7.2 GHz uplink and 8.4 GHz downlink.

The tracking loops implemented on Iris are fully digital second-order phased-lock loops with configurable loop bandwidth settings. The coherent turn-around approach takes the derived frequency from the carrier tracking loop and feeds this to a direct digital synthesizer (DDS) generator to tune the X-band phased-lock oscillator (PLO). This approach provides a simplistic method with fewer components that allows miniaturization while maintaining the necessary frequency agility from the transponder. The main oscillator is a 50 MHz Temperature Compensated Crystal Oscillator (TCXO) which is used directly to derive the X-band LO frequency for block downconversion, and also provides the main clock reference to the entire radio. A simplified block diagram of this architecture is shown in Figure 2.

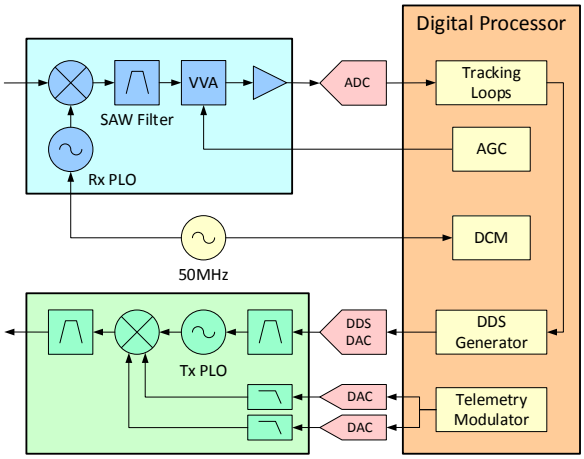

Figure 2: Iris Simplified Block Diagram

The initial design iteration of the clock management in the FPGA used an internal PLL to generate 100 MHz from the main oscillator in order to clock the digital-to-analog converters (DAC) at a higher frequency to keep spurious outputs low. However, the phase noise degradation from the internal PLLs were too high for deep-space telecom applications. It was noted that the dynamic power increase in the FPGA was minor and a future version of the Iris Transponder may consider a 100 MHz TCXO instead. Measured downlink carrier phase noise is presented in a later section.

KEY SPECIFICATIONS

Table 2: Iris V2.1 Specifications

Specification	Value
Downlink Frequencies	8400 – 8500 MHz
Uplink Frequencies	7145 – 7235 MHz
Turn-around Ratio	880/749
Downlink Symbol Rates	62.5 bps – 6.25 Msps
Uplink Data Rates	62.5 bps – 8 kbps
Modulation Waveforms	PCM/PSK/PM w/ subcarrier, PCM/PM w/ biphase-L, BPSK
Telemetry Encoding	Convolutional (r=1/2, k=7), Reed-Solomon (255,223) I=1 or 5, Turbo (1/2, 1/3, 1/6), Concatenated codes
Receiver Noise Figure	< 3.5 dB
Carrier Tracking Threshold	-151 dBm @ 20 Hz LBW
RF Output Power	> 3.8 W
Navigation	Sequential/Pseudo-noise Ranging, Delta-DOR
Transmit Phase Noise (one-way non-coherent)	-110 dBc/Hz; Δf = 100 Hz -117 dBc/Hz; Δf = 1 kHz -126 dBc/Hz; Δf = 10 kHz -127 dBc/Hz; Δf = 100 kHz
Oscillator Stability	0.001 ppm at Δt = 1 sec
Mass	< 1 kg (X/X only)
Volume	0.56 U (excl. SSPA/LNA)
Power Consumption	12.0 W Rx-only 33.7 W full Tx/Rx
Cmd/Tlm Interface	1 MHz SPI
Power Interface	9 – 28 Vdc
AFT	-20°C to +50°C
Dynamics	14.1 grms random vibration
Radiation	> 23.0 krad(Si); 37 MeV-cm^2/mg

TRANSPONDER DESIGN

Digital Processor Module (RaDiX)

The core of the SDR is the digital processor module that carries the main reprogrammable processing element (Xilinx Virtex-6 FPGA) which performs the signal processing for modulation and demodulation functions, as well as radio configuration, health status reporting, and link-layer protocol handling through an

embedded SPARC-based Leon3-FT softcore processor. The Virtex-6 defense-grade FPGA was chosen as an improvement from Iris V1 which used a smaller Virtex-5 FPGA that lacked room for an embedded processor. The V6 FPGA was screened for heavy-ion induced Single-Event Latch-up (SEL) at the Texas A&M Cyclotron Institute and no SEL event was observed at a linear energy transfer (LET) of 37 MeV-cm^2/mg. Rad-hard memory devices are used for program memory (2 MB SRAM, EDAC protected) along with a rad-hard 32 MB NOR FLASH for storing bit stream configuration files and application software builds.

The main interface to the spacecraft is via a Serial Peripheral Interface (SPI) running at 1 MHz line rate, but hardware elements are in place to allow high-rate data input via a SpaceWire over LVDS link with minimal NRE. SPI commands are used to configure the Iris software and various modem parameters, as well as transfer downlink data from the C&DH to Iris asynchronously. Internally, the Iris software forms standard CCSDS AOS Transfer Frames for downlinking to the ground station.

Figure 3: RaDiX Assembly (Top Side)

Modem Processor Overview

Large portions of the Modem Processor signal-processing chain are heritage design from the Electra product line of JPL SDRs. This synergistic development has proven extremely valuable bi-directionally to all JPL radio product lines where improvements from one product can be directly incorporated to other JPL SDRs. Previous research and development tasks had taken this platform and further expanded its capabilities to include deep-space navigational support for the UST platform. A simplified functional diagram of the Iris Modem Processor is depicted in Figure 4.

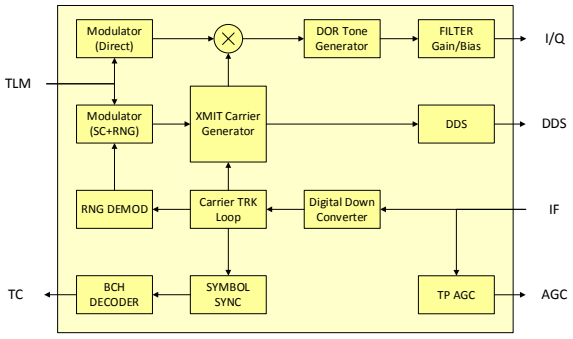

Figure 4: Modem Processor Functional Diagram

The modulated uplink signal at the 112.5 MHz IF is sampled by the ADC and the wideband Automatic Gain Controller (AGC) adjusts to maintain optimal signal power. The level-tuned signal is internally down-converted and decimated, and is fed to a fully-configurable Carrier Tracking Loop (CTL) to track frequency and phase of the uplink carrier. In coherent mode, the frequency word output from the CTL is fed to the transmit carrier generator to maintain the 880/749 turn-around ratio on the downlink carrier.

For low data rates typically encountered in deep-space applications, the uplink data needs to be modulated on a subcarrier to prevent data power from falling within the CTL bandwidth of the carrier it is trying to track. The DSN thus typically modulates uplink data on a 16 kHz sine-wave subcarrier, and the spacecraft radio must be able to track and demodulate. Iris employs a similar fully-configurable subcarrier tracking loop (SCTL) as the CTL. After acquisition of the carrier and subcarrier, an early-late gate symbol synchronizer demodulates the BPSK or QPSK modulated waveforms. Before the recovered symbols are passed to the uplink handler in the Telecom Interface, single-bit error correction and double-bit error detection is performed by decoding the CCSDS-recommended BCH encoding on the uplink code blocks.

Navigational support can be provided by either turn-around of sequential or pseudo-noise ranging tones and/or the generation of Differential One-way Ranging (DOR) tones. Ranging tones are modulated onto the downlink after filtering the complex baseband output from the CTL with a 1500 kHz low-pass ranging filter to reduce the coupled noise. Two DOR tones, typically at 1 MHz and $2f_0$ (f_0 is the base frequency of the DSN link, approximately 9.6 MHz; downlink is at $880f_0$ and uplink is at $749f_0$) are modulated onto the carrier when delta-DOR navigation is necessary.

Telemetry data for downlinking are modulated by generating in-phase and quadrature components which are complex multiplied to the carrier waveform. The signal is then filtered and conditioned to minimize spurious products fed to the DACs.

Telecom Interface Overview

A unique feature of Iris that separates it from other JPL radio products is the Telecom Interface module that performs command detection and forward error correction (FEC) of the downlink data. Traditional radios accept a synchronous stream of encoded data provided by the Command and Data Handling (C&DH) subsystem, but in CubeSat and SmallSat applications where limited processing power is available, the move towards a "smart radio" reduces the burden and resource needs in the C&DH. The Iris Telecom Interface depicted in Figure 5 is largely inherited from the JPL-developed Multi-mission System Architectural Platform (MSAP) which has been used in various flight projects like Mars Science Laboratory, Soil Moisture Active Passive, and the upcoming NASA-ISRO Synthetic Aperture Radar (NISAR) mission.

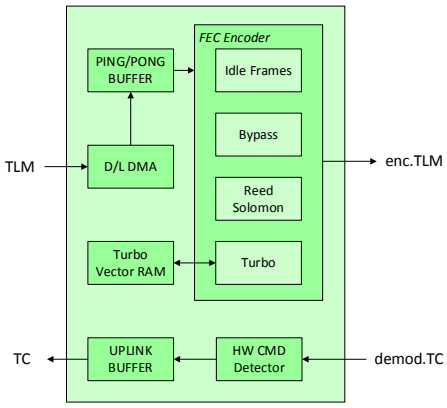

Figure 5: Telecom Interface Functional Diagram

The MSAP Telecom Interface module provides FEC encoding of the downlink telemetry data with Reed-Solomon (255, 223) code with interleave 1 or 5, or with Turbo codes at rates 1/2, 1/3, or 1/6 using block lengths of 1784 bits or 8920 bits. The encoder also appends the appropriate Attached Sync Marker (ASM) bit patterns per the CCSDS. Concatenated coding with NASA standard convolutional code (k = 7, r = 1/2) or pseudo-randomization can be done to any FEC encoding by the Modem Processor prior to transmission to the ground.

The demodulated uplink frames are also passed through a hardware command detector, capable of detecting specialized uplink frames intended for direct interpretation and execution by the radio hardware. Examples include hardware commands to enable the downlink carrier, or providing a discrete signal output for the flight system to interpret and execute, such as a back-door "fire code" to reset the entire CubeSat in case of a fault.

Power Supply Board (PSB)

One the major design updates for the EM-1 missions was the redesign of the power supply board (PSB) to increase the radiation tolerance. The original design was intended for a Mars mission with a total ionizing dose (TID) requirement of 2.9 krad(Si) with a radiation design factor of 2 behind 100 mils of aluminum. The NEA Scout mission has a long primary mission duration of 2.5 years with an expected TID level exceeding 20 krad(Si), which necessitated a design change.

Space-grade, radiation hardened DC/DC converters are typically bulky hybrid devices that would occupy large volume and mass, so alternate parts were sought. Bipolar COTS converters were chosen for their SEL immunity, but TID tolerance was typically unknown. Selected candidate devices were then radiation tested for high-dose rate (48 rad/s) TID with a Cobalt-60 source at JPL up to 50 krad(Si) with a sample size of at least three devices. Table 3 lists the devices tested and their results.

Table 3: TID HDR Testing of COTS Regulators

Part No.	HDR Test Result
LMZ34002	Hard failures at 14-16 krads (biased) Unbiased devices show slight changes at 50 krads
LT1964	Output increased 20% at 26 krads, 30% at 38 krads Total functional failure by 50 krads
LT3082	No degradation/failures up thru 50 krads
LT3433	Functional failures at 17-21 krads (biased) Unbiased devices func. failure at 10-12 krads
LT8570	Output degraded 2% at 7 krads
LT8610	No degradation/failures up thru 50 krads
LT8613	No degradation/failures up thru 50 krads

Most secondary voltages on Iris are lower than the minimum bus input voltage to the PSB, and hence synchronous buck regulators and low dropout linear regulators could be used, except for the TCXO bias circuitry that needs +13.5 V at 30 mA. Given the buck/boost LT3433 and the boost/SEPIC/inverting LT8570 devices failed radiation testing, a custom flyback converter using a rad-hard Intersil ISL78845 PWM chip was designed. The final design of the PSB utilizes the custom flyback converter, along with LT8610, LT8613, and LT3082 COTS converters as shown in Figure 6.

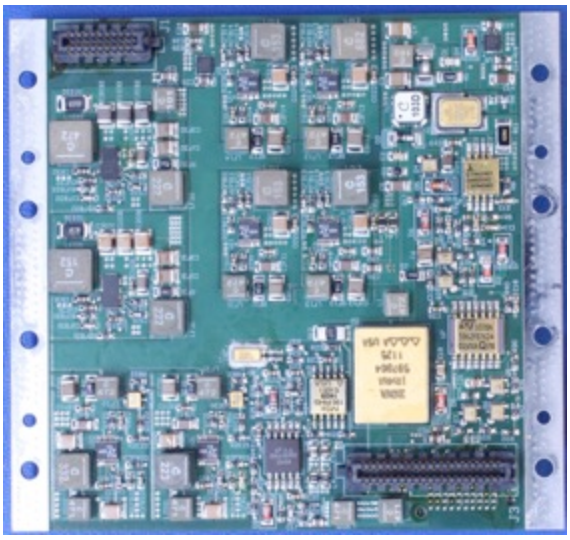

Figure 6: PSB Assembly (Top Side)

X-band Receiver

The receiver shown in Figure 7 is a standard superheterodyne architecture with a single down-conversion from DSN/NEN X-band frequencies (7145 to 7235 MHz) to an IF of 112.5 MHz. All X-band amplification is performed by an external Low Noise Amplifier (LNA) block to reduce the overall gain in the receiver slice. This allows easier control of potential unwanted oscillations. After the front-end pre-select filter, low-side LO injection from 7032.5 to 7122.5 MHz is performed with an image-reject mixer (IRM) having > 40 dB of image rejection.

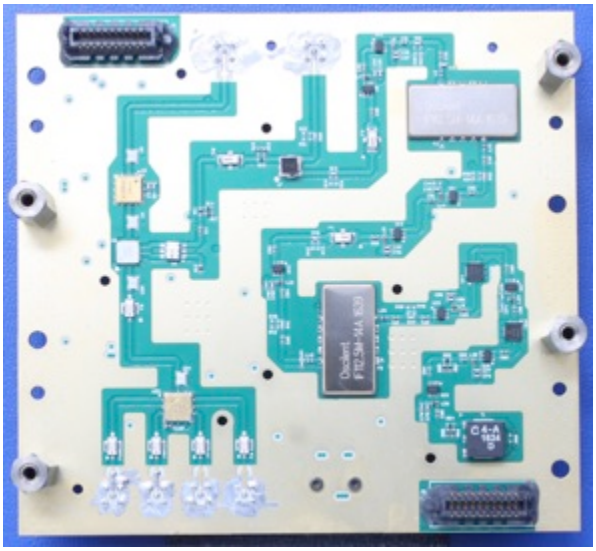

Figure 7: X-band Receiver Assembly (RF Side)

In the IF chain, several SAW filters, IF amplifiers, and voltage-variable attenuators are used to set the noise bandwidth, reject additional mixer spurious outputs, and provide a nominal 0 dBm input power level to the ADC on the digital processor. The IF bandwidth is set by two SAW filters with a bandwidth of 14 MHz.

X-band Exciter

The exciter board acts as the modulator as well as the frequency synthesizer for the entire radio by housing the 50 MHz TCXO and phased-locked oscillators (PLO). A space-grade TCXO is used on Iris to provide excellent thermal stability as well as low phase noise. The PLO circuit uses an Integer-N phase-locked loop (PLL) chip with an active loop filter that feeds an X-band voltage-controlled oscillator (VCO). The PLL is closed by the aid of a divide-by-2 pre-scaler chip. The two PLOs (one for receive LO and one for the transmit carrier) are nearly identical except for the VCO chip and loop filter bandwidth settings. As it can be seen in Figure 8, the frequency synthesis portion occupies a large amount of the board real estate (> 50%).

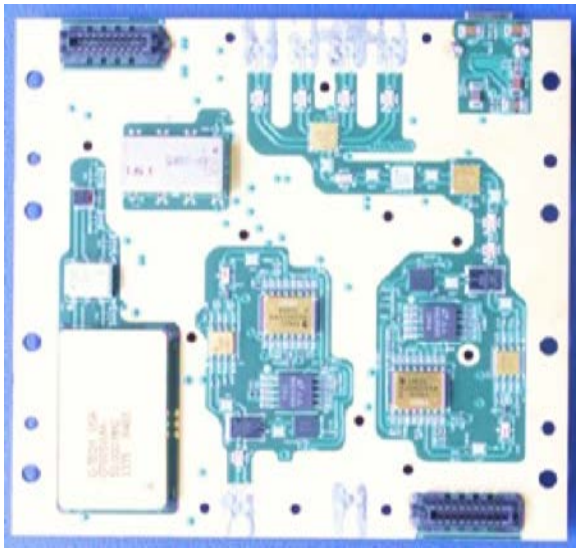

Figure 8: X-band Exciter Assembly (RF Side)

The modulator on Iris uses an I/Q mixer to directly modulate the X-band carrier with the waveform supplied from the digital processor. 25 MHz low-pass I/Q filters provide baseband filtering of the modulated waveform, and bandpass filtering is provided at the modulated X-band output to limit spurious outputs and provide suppression of the modulation tapers.

X-band Low Noise Amplifier (LNA)

An external LNA assembly must be used alongside the Iris Transponder to provide the front-end X-band amplification of the uplink signal. Noise figure impact can be reduced with a separate unit by minimizing the front-end circuit loss between the receiving antenna and

the LNA by placing the unit physically close to the antenna.

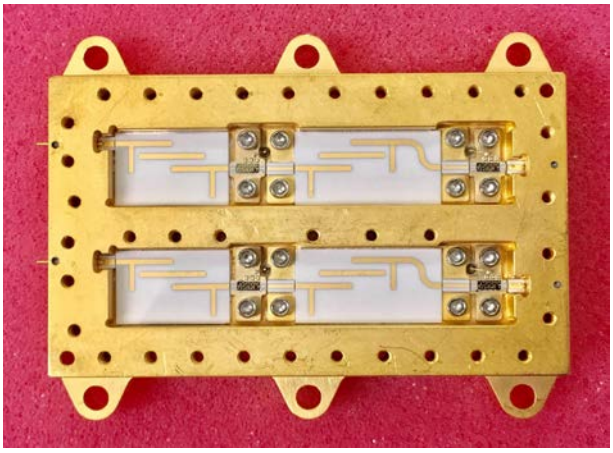

Figure 9: X-band LNA Assembly (RF Side)

As shown in Figure 9, the LNA is assembled as chip-and-wire circuitry using MMIC bare-die amplifiers and ceramic microstrip elements to reduce the packaging size and also reduce losses. The ceramic bandpass filters provide pre-selection of the uplink signal as well as transmit rejection of the downlink signal 1.2 GHz away to allow full duplex communications without incurring receiver deafening. The LNA assemblies for the EM-1 missions carry two identical amplification chains to allow up to two connections to receiving antennas.

X-band Solid State Power Amplifier (SSPA)

The external SSPA assembly is also a chip-and-wire assembly with three identical chains as shown in Figure 10. The primary advantage and motivation for an external SSPA unit is not only to reduce the circuit loss from the SSPA to the transmit antenna, but mainly driven by thermal performance.

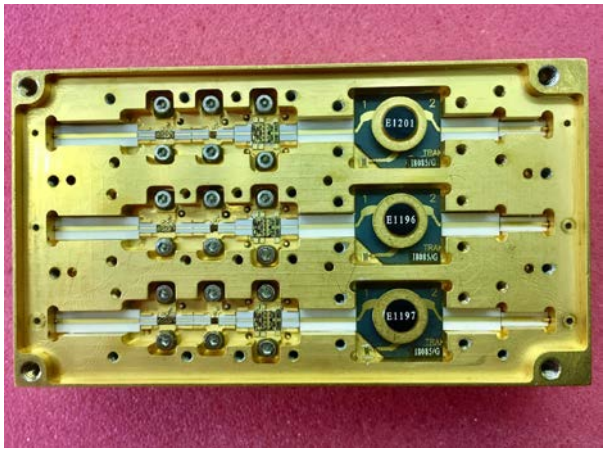

Figure 10: X-band SSPA Assembly (RF Side)

The SSPA is designed for 4 watts of RF output using GaAs technology, yielding approximately 30% drain efficiency. Careful attention to the thermal packaging design is made so that a good conductive thermal path can be provided to the spacecraft structure to dissipate approximately 12 watts of waste heat. The final-stage amplifier MMIC is bonded to a copper-tungsten carrier using high thermal conductivity silver-loaded epoxy, and directly under are threaded holes in the aluminum chassis that provide the conductive thermal path.

The RF design is a cascaded amplifier design with two driver MMICs followed by the final-stage MMIC. An output isolator is installed to provide a good output match to the amplifier as well as protect the circuitry in case of a fault condition at the amplifier output.

Packaging Overview

The Iris Transponder stack which comprises of the digital processing board, power supply board, X-band receiver, and X-band exciter are designed to be modular stackable slices. The use of coaxial interconnect cables is minimized to only the X-band LO signal, and all other signal lines like the main 50 MHz clock, digital I/Q waveforms, secondary regulated voltages, and control lines are interconnected using high-speed board-to-board stacking connectors. Each individual slice is designed for optimized thermal transfer from the device junctions to the chassis walls using minimum 1 oz. ground layers in the printed wiring board (PWB), or a dedicated heatsink with low-outgas thermal adhesive. The PWBs all have a 7-mm track of exposed ground plane with thermal vias to allow the dissipated heat to be extracted to the aluminum chassis. The chassis is made flush to the PWB board, which allowed a 30% volume reduction from previous Iris units.

MEASURED RESULTS

All slice elements have now been assembled and rigorously tested. Some select test data results are presented here.

Figure 11 shows the measured gain from the LNA assembly. In the uplink band from 7145 to 7235 MHz, the LNA has strong small-signal gain at 43 dB, and exhibits over 100 dB of transmit isolation in the 8400 to 8500 MHz band. The large isolation helps keep the receiver chain from saturating due to the transmit power, but the filter does not prevent the side skirts of the modulated waveform from presenting itself as wideband noise in the uplink receive band. Careful system engineering must be done to prevent unintended degraded performance. An external bandpass filter may be required with high data rates.

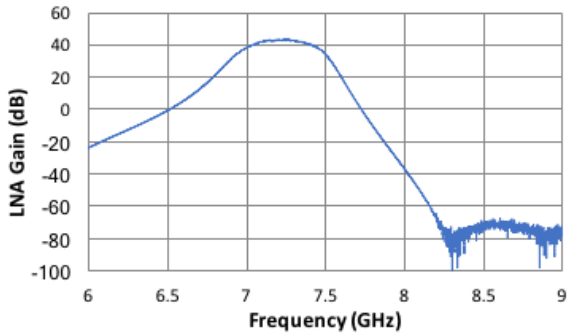

Figure 11: X-band LNA Gain

Figure 12 shows the measured power transfer curve of the SSPA over temperature. The X-band exciter output is approximately -15 dBm, and keeps the SSPA in the saturated region for high efficiency and low output power variation over temperature. The SSPA generates greater than 4 watts of RF output comfortably with 30% efficiency. Software control can also be employed to reduce the exciter output based on unit temperature.

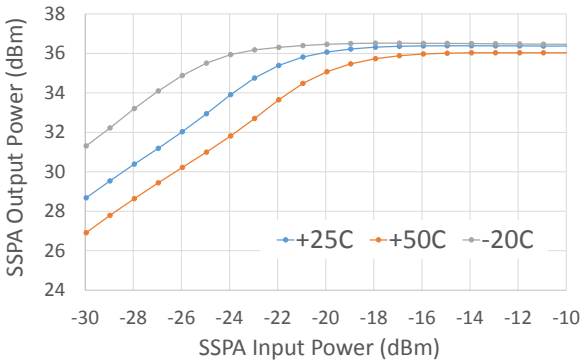

Figure 12: X-band SSPA Power Transfer Curve

The PSB is designed for a full load of 40 watts power delivery. Measured results show good power supply regulation of all secondary voltages with a total efficiency of approximately 88% in typical 6U bus voltage range of 10-16 Vdc (Figure 13).

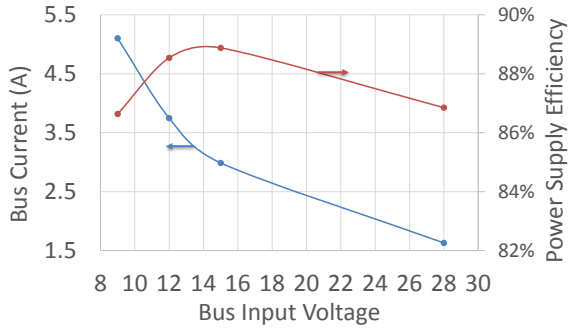

Figure 13: PSB Full Load Performance

In Figure 14, the receiver IF spectrum with a single-tone input with high Signal-to-Noise (SNR) ratio is shown. Here, the 14 MHz IF noise bandwidth is clearly visible around the carrier, and harmonics of the 112.5 MHz IF signal can be seen. These image tones are removed digitally once sampled by the ADC.

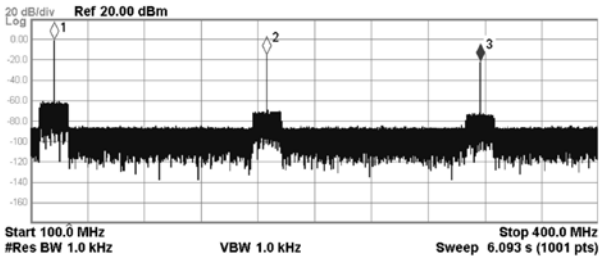

Figure 14: Receiver IF Spectrum at High SNR

The performance from the TCXO show excellent phase noise with -150 dBc/Hz by 1 kHz offset from the 50 MHz carrier and RMS jitter of 0.3175 ps (Figure 15).

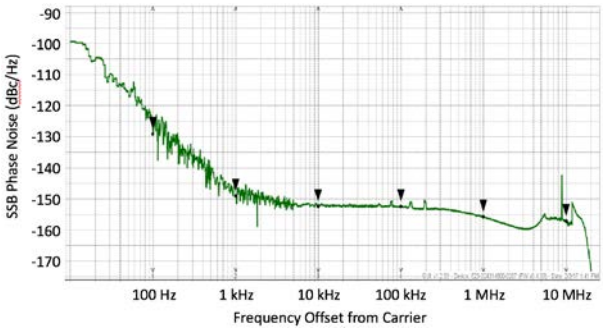

Figure 15: TCXO Output Phase Noise

The phased-locked oscillators on the exciter board also performs well with reasonable phase noise performance as shown in Figure 16. The calculated rms phase jitter over 100 Hz to 1 MHz is 12.1 fs.

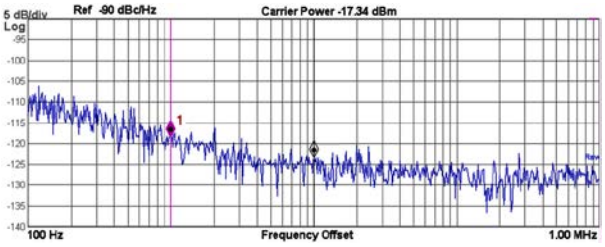

Figure 16: X-band Carrier Phase Noise

TYPICAL TRANSPONDER PERFORMANCE

The carrier tracking threshold is a critical performance measurement of the receiver that allows the telecom system engineer to determine the maximum range of communications possible. Noise introduced from the antenna, passive elements, and the LNA are all

integrated within the loop bandwidth ($P_N = k_BTB$), so narrower tracking loop bandwidth are desired. However, narrow loop bandwidth results in slower dynamic response and the radio may have difficulty tracking the carrier signal in high-Doppler situations. In Figure 17, measured carrier tracking threshold matches closely to the 6 dB SNR limit line of a PLL-based carrier tracking loop. The configurability of a software-defined radio provides the adaptability to different mission phases and needs. For instance, the MarCO receiver loop bandwidth is set to approximately 70 Hz for most of the mission, but for the reception of InSight's Entry, Descent, and Landing (EDL) signal, the bandwidth is increased to 200 Hz to be able to maintain carrier lock throughout the high Doppler dynamics of InSight's parachute deployment.

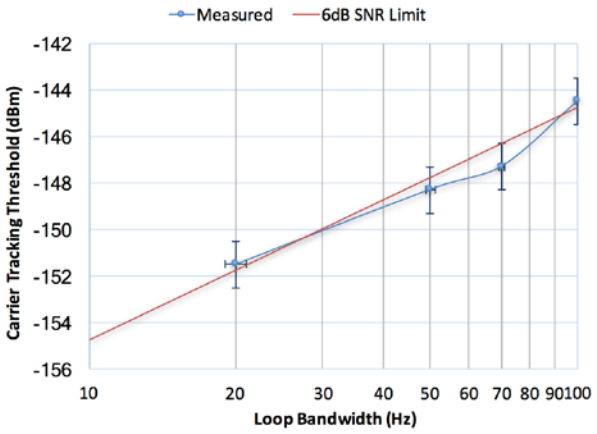

Figure 17: Carrier Tracking Threshold

Typical bit error rate curves of an uncoded uplink signal at modulation index of 1.5 radians is plotted in Figure 18 for several data rates.

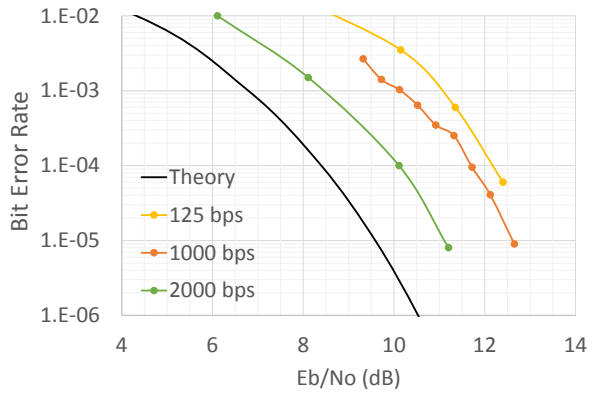

Figure 18: Receiver Bit Error Rate Curves

Figure 19 shows the measured transmit spectrum of a pseudo-random bit sequence in residual-carrier mode with biphase-L at 6.25 Msps from an experimental unit.

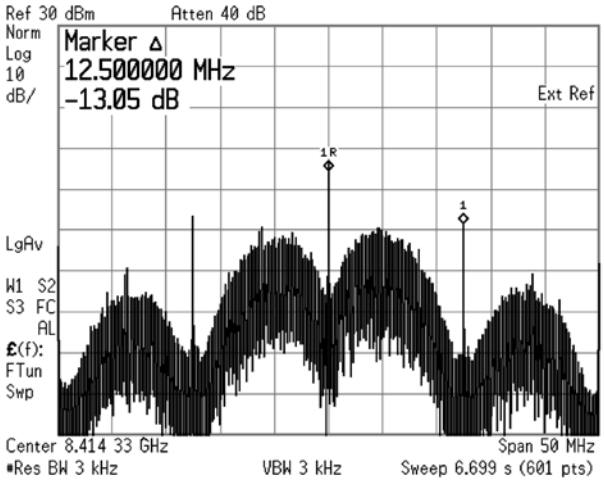

Figure 19: High-Rate Downlink Spectrum

Some residual I/Q imbalance can be seen as spurious outputs at the BPSK waveform nulls which can be suppressed by software configuration. The unit is calibrated for deep-space use for EM-1 missions that have a maximum data rate of 256 kbps.

CONCLUSIONS AND FUTURE PLANS

A thorough description of the Iris Transponder for CubeSat/SmallSat applications has been presented from the hardware design of each slice element to the firmware and software elements that build up the software-defined radio. Some select measured values of typical radio performance is presented and discussed.

The EM-1 Iris Transponder units are currently in testing and characterization. Qualification tests (random vibration, thermal vacuum, EMI/EMC compatibility) are planned to be completed by the summer of 2017, and compatibility tests against the DSN is planned to take place at the DTF-21 facility as well.

Additional research and development efforts are underway, such as radio occultation study of the Martian atmosphere, improved quality of service with support for Delay Tolerant Networking, and improved channel coding gain with Low Density Parity Check (LDPC) codes. The hardware platform can also be reconfigured and adapted as a radar instrument. The modular architecture of JPL radio product lines provide adaptability to mission requirements for various radio service needs.

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