FPGA-based Automatic Modulation Recognition System for Small Satellite Communication Systems

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ABSTRACT

Automatic Modulation Recognition (AMR) is considered one of the important applications in Software Defined Radio (SDR) receivers that gives the ability to change the demodulator of the receiver system according to the recognition of the received modulated. Most of the modern satellite communication systems are using Quadrature Phase Shift Keying (QPSK) for their signals modulation purpose. In this paper, VHDL implementation of Binary Phase Shift Keying (BPSK) and QPSK modulations generator and the AMR are done using Vivado 2015.2. BPSK and QPSK are implemented using Numerical Controlled Oscillator (NCO), and AMR which consists of two modules; features extraction and classification modules. Features are extracted using Discrete Wavelet Transform (DWT), and Support Vector Machine (SVM) is used to classify the received modulation. The code is implemented on Kintex-7 FPGA and the results show the good performance of the system in addition to low power consumption.

INTRODUCTION

SDR is the basis of universal wireless systems and it is defined as radio in which some or all of the physical layer functions are software defined. SDR performs the most of signal processing in the digital domain based on FPGAs. One of the applications based SDR is AMR.

AMR is the automatic modulation classification of the received modulation signal. i.e., it has to identify the modulation scheme of received signal. So it has important role between detection and demodulation stages.

AMR is the key role in the implementation of advanced wireless communication system especially for satellite communication system. AMR can be categorized in two main approaches; the Decision-Theoretic (DT) approach based on likelihood function, and the Pattern Recognition (PR) approach based on extracting unique measurable values (features) of the signal [1]. DT approach Based on multiple hypothesis testing and has high performance in terms of correct classification percentage (optimal) but the drawbacks of this approach are high computational complexity which leads to that the classifier is impractical, and high sensitivity to impairments as frequency and phase offset. On the other hand, PR approach based on pattern matching is suboptimal, simple to implement, and robust.

In recent years, AMR has become the dominant research point in wireless communication system. Classification system based on features that are extracted from different modulations using Stockwell-transform and classified using different classification techniques such as ANN, and SVM have been studied in [1]. AMR system is implemented using DWT to extract the transient characteristics of the modulation and based on a threshold value, the modulation type is being recognized [2]. AMR system is implemented using two stages; energy detection (spectrum sensing) and modulation classification stages. Principle Component Analysis (PCA), and Artificial Neural Network (ANN) were used for the classification stage [3]. A classification system is implemented using predefined templates in Wavelet Domain (WD) stored in receiver side for several modulations which has been generated using DWT then matching these templates with the one initiated during real-time [4]. New technique using 8PSK demodulator output as features extraction and Bayes classifier for classification [5]. Cumulants and ANN are used for features extraction and classification in AMR system [6]. Other have studied using features extracted from FFT then compare them with some threshold values to make the decision [7], and using higher order cumulants as features and K- Nearest Neighbor as a classifier [8].

In this paper, FPGA based AMR system is described. AMR system consists of two stages; First, is generation of M-array Phase Shift Keying (M-PSK) modulations that used in satellite communication system. BPSK and QPSK are used for simplicity and proof the concept. Second is recognition stage that has two modules; features extraction, and classification modules.

DWT is used for extracting the features of M-PSK, and for classification, SVM is used as a binary classifier.

This paper is organized as follows; Section 2 introduces the principle of the AMR system, Section 3 describes FPGA based M-PSK generator, Section 4 describes FPGA based recognition system. Section 5 presents the simulations and results, and Section 6 concludes the paper.

AMR SYSTEM

features based AMR system has to perform offline (training) and online (classification) processes. In offline process, training database has to be created based on features that extracted from received signal. And according to the trained database, some parameters are used by the classifier to classify the received signal. Figure 1, explain the principle of AMR system [9].

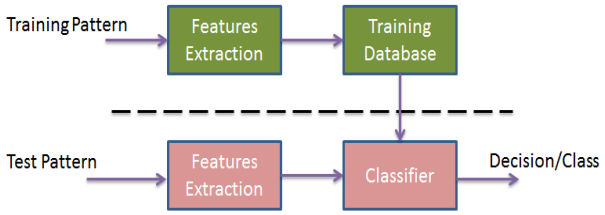

Figure 1: AMR Principle

In this paper, AMR system consists of M-PSK generator and recognition stages (see Figure 2).

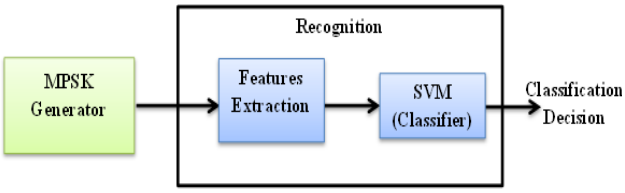

Figure 2: AMR System

M-PSK Generation Stage

M-PSK generator generates BPSK and QPSK modulation using Numerical Controlled Oscillator (NCO) principle to generate four sinewaves signals with different phases; 0, 90, 180, 270. Two phases represent BPSK; 0, and 180. Four phases represent QPSK; 0, 90, 180, 270 as in Table 1. According to the selector value BPSK or QPSK signal is generated. The generated PSK modulation feeds the input of the recognition stage.

Recognition Stage

Recognition stage consists of two modules; features extraction and classification modules which describe as follows;

Table 1: BPSK and QPSK Phases

Selector Value	BPSK Phase	Selector Value	QPSK Phase
0	0	00	0
		01	90
1	180	10	180
		11	270

Features Extraction Module

The generated PSK modulation from the first stage is received by features extraction module of the second stage. Three stages of DWT are used to extract features of the received signal then the extracted features become the input of the classification module.

Different stages numbers of Low Pass Filters (LPF) and High Pass Filters (HPF) with decimation factors are used to implement DWT function [10]. Figure 3, shows Two Stages of DWT.

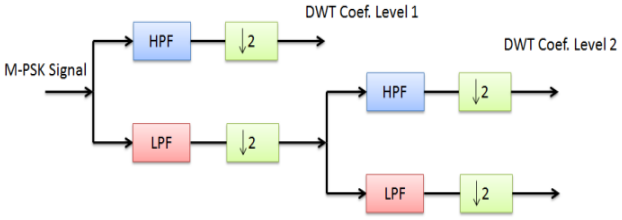

Figure 3: Two Stages DWT

The output of LPF is the approximation coefficients and the output from HPF is the details coefficients which are the required features.

Classification Module

To classify the received modulation, pre-determined parameters are calculated by training the classifier in offline mode then these parameters are used to construct the classifier to classify the modulation in run time.

SVM is one of the classifiers that used in classification process. The first objective of SVM is to maximize the margin between the closest data points of two different classes. The second objective is to be sure that all data points belong to their correct classes. SVM classifies the points from two linearly separable sets in two classes by solving a quadratic optimization problem in order to find the optimal separating hyper-plane between these two classes, Where it can classify data points from two linearly separable sets into their corresponding classes, also expanded to be used for the nonlinear cases by transforming the input data into a nonlinear space using Kernel functions [11].

SVM classification equation for nonlinear classification problems can be expressed mathematically as in Eq. 1 [12].

$$g(x) = W.\ K(X_i\ .X_j) + b \qquad (1)$$

Where g(X) is classification function, W is the normal to hyper plane $K(X_i\ .\ X_j)$ is Kernel function, b is the bias.

Kernel function is considered dot product that transforms nonlinear classification problems from input space to linear features space where the classification can become easier (see Figure. 4 [12]).

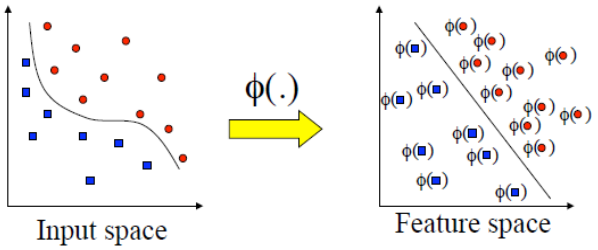

Figure 4: Kernel Function Transformation

FPGA BASED M-PSK GENERATOR DESIGN

To implement M-PSK modulation generator stage in VHDL using Vivado, there are many methods can be used as coordinate rotational digital computer (CORDIC), Direct Digital Synthesizer (DDS), and NCO principle. In this paper, NCO principle is used to generate the required signals for BPSK and QPSK modulations.

M-PSK modulation generator stage consists of serial data generator module, serial to parallel module, NCO module, and multiplexer (see Figure 5).

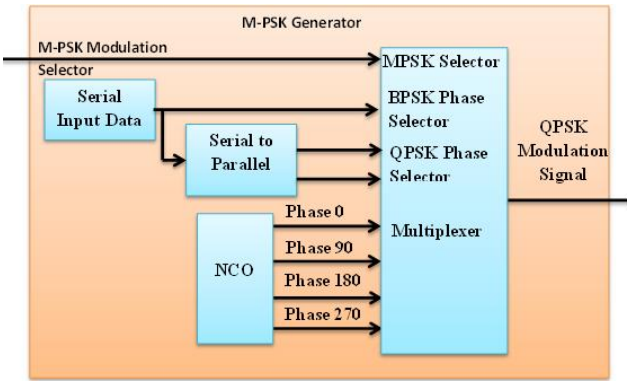

Figure 5: M-PSK Stage Block Diagram

Serial data generator simulates serial data required to be transmitted. These serial data feeds the input of multiplexer module directly, for BPSK modulation, and feeds the serial to parallel module for QPSK modulation.

NCO module generates four sinewaves signal with different phases 0, 90, 180, 270. These phases feed the inputs of the multiplexer module.

NCO consists of phase constant, phase offset, phase accumulator, sinewave look-up table. The phase offset is responsible to generate the four sinewaves with the required phases, i.e. it is the pointer that determine from which location in the LUT the generation of sinewave will start (see Figure 6).

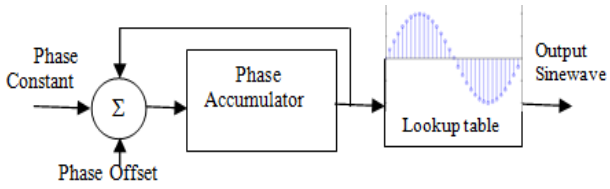

Figure 6: NCO Module Block Diagram

To build the NCO module, some parameters should be estimated according to the required output frequency; phase accumulator capacity, the step between each sample of the sinewave samples in LUT, and operating clock frequency. The mathematical representation of NCO module to determine the parameters of phase generation module is in Eq. (2).

$$fout = \frac{Sinewave\ \ Step \times\ Clock\ \ Frequency}{Accumulator\ \ Capacity} \qquad (2)$$

In this paper, for simplicity the parameters are chosen to be as shown in Table 2.

Table 2: NCO Parameters

Parameters	Values
Output Frequency (fout)	6.25 MHz
Clock Frequency	50 MHz
Accumulator Size	8 Values
Step Size	1

Multiplexer module is controlled by three inputs from the outputs of; serial data module, serial to parallel module, and the M-PSK selector. So, according to the M-PSK selector value, one of other controlling signal is used to control the multiplexer output, BPSK or QPSK.

FPGA BASED RECOGNITION SYSTEM DESIGN

Recognition stage is the one that have to be implemented in the receiver module for a satellite communication system.

Recognition stage consists of two modules; features extraction module and classification module. Where a received M-PSK signal becomes the input to DWT features extraction module and the output of this module feeds the input of the classifier to obtain the classification decision or to know which M-PSK type is received (see Figure. 7).

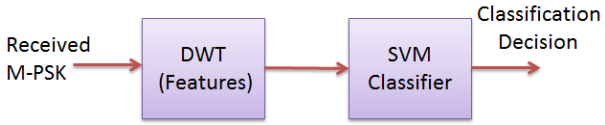

Figure 7: Recognition Stages

Features Extraction Module

Three stages of DWT are used to extract features of the BPSK and QPSK modulation signals. To implement DWT, three stages of Finite Impulse Response (FIR) IP core filter are used (see Figure 8).

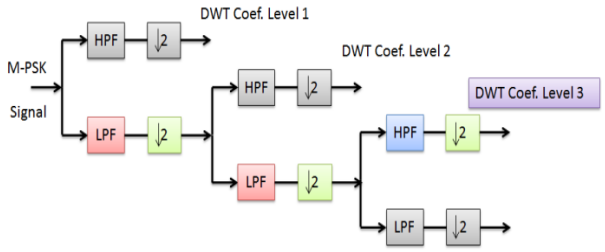

Figure 8: Three stages DWT

According to this paper purpose, it is not practical to implement the whole blocks in Fig. 7, just the coloured path is required to obtain the DWT coefficients (features). Two LPF filters followed by one HPF are required to obtain the required level of DWT features. The implementation of complete DWT system is mandatory for reconstruction of images in imaging processing projects.

Filter coefficients can be obtained from MATLAB tool according to the type of the wavelet. In this paper, daubechies wavelet type (db5) is used. After obtaining the coefficients from MATLAB tool, the filters become ready to extract the features.

Classification Module

SVM principle is used to classify the received features from features extraction module into two classes; BPSK class and QPSK class.

Before the classification, there is a training process that have done using MATLAB tool to training SVM on the features that extracted from DWT to label these features with the correct class. The purpose of doing this process in MATLAB is to obtain the required parameters for the classifier in recognition module and in the same time, to reduce the complexity of AMR system.

To classify BPSK and QPSK modulation it is required to select the proper kernel function that gives the best classification accuracy, many tests have done on the available kernel function with the extracted features, and the one with highest accuracy will be used.

Four kernel functions have been tested using MATLAB Tool; Linear, Quadratic, Polynomial, and Radial Base Function (RBF) (as shown in Table 3).

The results show that using RBF as kernel function is the accurate choice to get high classification percentage comparing to the others kernel functions.

From the, RBF is selected to be the suitable kernel function because of its high classification accuracy.

Table 3: Kernel Functions Accuracy

Kernel Function	Accuracy (%)
Linear	Xi . Xj
Quadratic	((Xi . Xj) + 1)
Polynomial	((Xi . Xj) + 1)d
Radial Base Function	$-\frac{\|\|x_i - x_j\|\|^2}{2\sigma^2}$

According to Eq. 1, it is required to implement RBF kernel in VHDL, so RBF function (as shown in Table 3) can be implemented as follows (see Figure. 9).

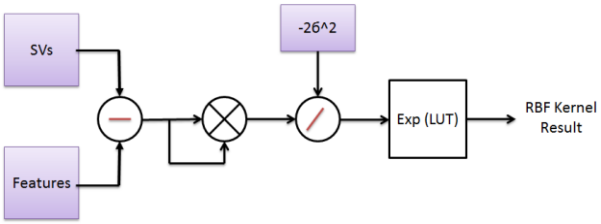

Figure 9: RBF function block

Where SVs are the support vectors that obtained from the training process using MATLAB tool and features are the out of DWT module. To reduce the complexity of exponential function and to save FPGA resources, a

LUT is used instead of implementing exponential function. σ (Sigma) parameter is selected to be 0.1.

After implementing RBF function, the classification function (Eq. 2) can be implemented as follows (see Figure 10) where SVM Alphas and bias are obtained during the training process.

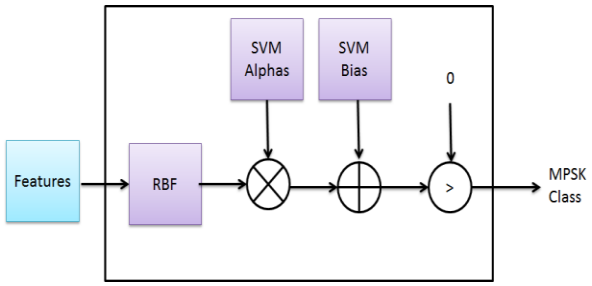

Figure 10: Classification Equation Functional Block

The correct classification decision can be obtained by a comparison between the classification function result and zero (0), if the result is greater than 0 the decision is BPSK class and if else the decision is QPSK class.

SIMULATIONS AND RESULTS

In this section, the simulations and results of some of the system parts will illustrate. The simulation and results are obtained using Vivado 2015.2 tool and kintex-7 FPGA kit and according to the system configuration (as shown in Table 4) for MPSK generator stage and recognition stage.

Table 4: System Configuration

Module	Clock Rate (MHz)
Main Clock	50.00
Serial data	12.5
MPSK Signal	6.25
Recognition Rate	6.25

The first three parameters in Table 4 in addition to the value of M-PSK modulation selector are used to produce Simulation result of M-PSK generator block (Figure 11).

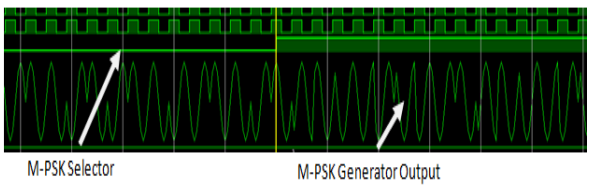

Figure 11: M-PSK Simulation Output

From the above figure, it is clear that according to the value of M-PSK modulation selector, one of the modulation schemes is produces (as shown in Table 5).

Table 5: M-PSK Output vs. M-PSK Selector Value

M-PSK Selector Value	M-PSK Modulation Output
0	BPSK
1	QPSK

In figure 12, the simulation of output from the three DWT stages illustrates as the output of the first stage is half the input of this stage, and so on for the second and third stages where the decimation value is equal 2.

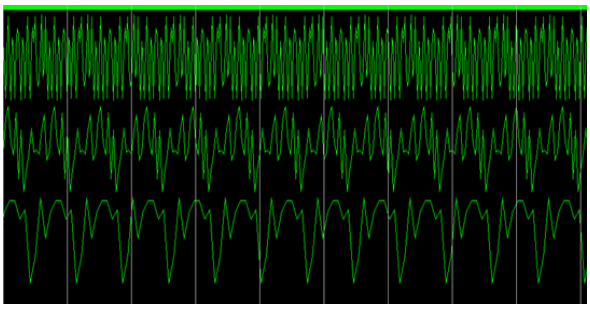

Figure 12: Simulation Output of DWT Stages

The selection of SVM kernel function is based on the test results obtained by testing different kernel function with the extracted DWT features and comparing the accuracy of each one. The comparison result is described as shown in Table 6 and Figure 13.

Table 6: Comparison among Different kernel Functions

Kernel Function	Accuracy (%)
Linear	50.5
Quadratic	61.66
Polynomial	72.70
Radial Base Function	94.44

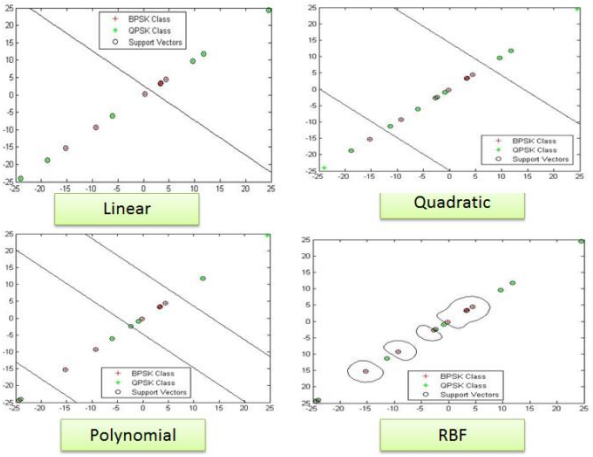

Figure 13: Kernel Functions Comparison Result.

According to Table 6 and Fig. 13, RBF is selected to be the kernel function for the SVM. The sigma parameter of RBF kernel is selected to 0.3.

The simulation result of the implemented classification system using SVM is as seen in Figure 14.

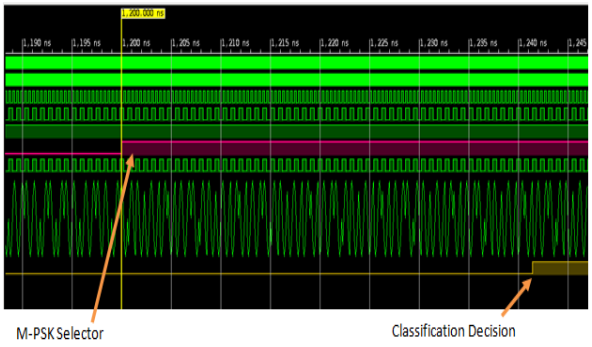

Figure 14: Classification Decision Timing.

The time that taken from pressing the switching key on the board to the classification decision output is about 42 ns, and the time that taken by the classifier (SVM) to get the classification decision is 10 ns.

For small satellites, it is important to implement AMR system with less power consumption and resources utilization as shown in Table 7 and Figure 15.

Table 7: Resources Utilization

Resource	Utilization	Available	Utilization%
FF	1215	202800	0.60
LUT	1309	101400	1.92
Memory LUT	132	35000	0.38
I/O	5	285	1.75
DSP 48	42	600	7.00
BUFG	4	32	12.50
MMCM	1	8	12.50

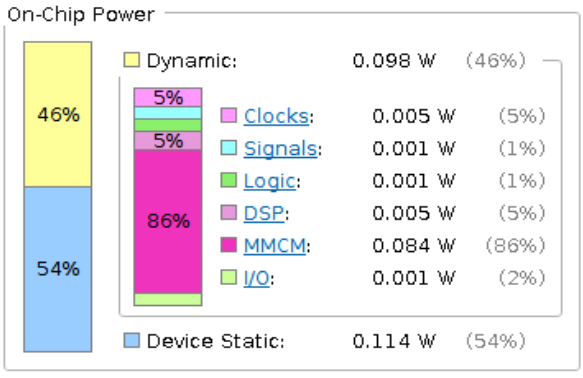

Figure 15: AMR System Power Consumption.

From Figure 15, the total power of the whole AMR system is the summation of device static power and dynamic power which is equal 212 mW. So, it can be used for small satellite applications.

Using MATLAB tool, 100 samples from BPSK and QPSK modulations are used to test the performance of AMR system, 4 sets of 100 samples for each modulation samples are used to determine the recognition rate of both modulations with Signal to Noise Ratio (SNR) from -10 to 20 dB.

The recognition rate can be determined by the following equation Eq. (3).

$$\text{Recognition Rate (RR)} = \frac{\text{Number of correct recognition trails}}{\text{total trails Numbers}} \quad (3)$$

According to Eq. (3), the result of the recognition system is as seen in Fig. 16.

The results are compared to previous studied to evaluate the performance of the AMR system. (as shown in Table [8,9])

Table 8: Comparison between AMR System and other studies for BPSK

BPSK							
	-10 dB	-5 dB	0 dB	2 dB	4 dB	8 dB	10 dB
[1]	98.8	99.9	98	-	100		
[2]	98	-	-	-	-	-	100 (at 30 dB)
[3]	-	-	-	91	-	100	100
[4]	-	-	86.3		93	98.2	100 (at 15 dB)
Proposed	98.7	99.8	100	100	100	100	100

Table 9: Comparison between AMR System and other studies for QPSK

QPSK							
	-10 dB	-5 dB	0 dB	2 dB	4 dB	8 dB	10 dB
[3]	-	-	-	84	-	96	100 (at 15 dB)
[4]	-	-	85.1	-	92.8	97.3	100 (at 20 dB)
[5]	-	-	1	-	98.5		97.4
[6]	0	-	0	0	47	100 (at 6 dB)	100
Proposed	0	1	18	47	70	94.5	100

DISCUSSION

Recently, AMR system is used in military and civilian application. It gives the ability to change/ detect different types of modulated signal then demodulate it using the corresponding demodulator using the same configuration without the need for using many Receivers or increase the complexity of the communication system. In this paper, FPGA based AMR system is implemented using Vivado 2015.2 and Kintex-7 FPGA kit. Many points have to be considered when designing such system as classification timing, resources utilization, power consumption, and recognition rate. From simulation section, the power consumption and resources utilization is considered low and can be used in small satellite application. And the classification timing is considered fast and suitable for this kind of application. For more accuracy, test has done on received modulations signal in addition to SNR from -10 to 20 dB. The purpose of this test is to get the recognition rate of BPSK and QPSK modulation signals, this test shows high classification rate for BPSK signal at 0 dB, for QPSK at 6 dB.

CONCLUSIONS

For more flexibility in satellite communication system and to overcome communication link problem, one of the solutions is the implementation of AMR system. FPGA base AMR system is implemented using Kintex-7 and Vivado 2015.2 Tool. AMR system consists of two stages; M-PSK generator and recognition stages. Two modulation schemes are implemented BPSK and QPSK for simplicity using NCO. Recognition stage consists of three stages of DWT as features extractor, and SVM as a binary classifier. This system achieves fast classification time about 42 ns, and low resources utilization and power consumption. I.e. the system is suitable even for small satellites. Recognition test is done using MATLAB tool to measure the classification probability under the existence of SNR from -10 to 20 dB. High recognition rate (100%) is obtained for BPSK and QPSK at -6 dB and 10 dB respectively.

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