

Concept and Feasibility of One-Embedded System Payload Including Baseband Communication

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ABSTRACT

Traditional approach of payload design develops modules separately such as control, compression and communication. Due to increasing demand of shorter development cycles and lower cost, we shall develop a highly adaptive approach for payload implementation so that we can update it in a short time according to the need of a new mission. Besides, the optimization of payload performance and communication link together becomes possible. Based on these, we propose a “one-embedded system” payload approach. All the control, file management, processing such as compression, and communications are implemented in one built-in embedded system. In other words, after the sensor signal is converted as digital data (after ADC, analog-to-digital-converter), the data gets into the proposed embedded system. And the system “does everything” and then outputs data to DAC (digital-to-analog-converter) and then transmitted it in analog form.

The proposed embedded system includes a FPGA implementing a processor IP. Due to the programmable characteristic of FPGA, hardware interfaces can be adjusted quickly according to various mission requirements. Besides, because of the flexibility and adaptability of software, code can be updated to optimize performance according to various tasks during flight. In this work, we provide concept, guideline of optimization, structure, feasibility, benefits and risks of one-embedded system payload approach. An example of implementation for optical remotes sensing payload including interfaces will be investigated.

1. MOTIVATION

Due to the need of diversity and flexibility of future missions, we plan to develop a highly adaptive approach for payload design and implementation in CubeSat. Compared with the traditional approach, the baseband communication such as channel coding and modulation are also incorporated into the proposed embedded system as shown in Figure 1. From Figure 1, the design principle can be interpreted as placing the embedded system as near ADC as possible and so does to the DAC. In this case, the embedded system does everything including command management, compression, interface control and baseband communications. By doing so, the optimization of payload performance and communications become possible which will be introduced in Section 3. In addition, the promising progress of silicon technology makes the whole idea feasible for space applications and will be explained in Section 4 to Section 6.

2. STRUCTURE

As we take optical remote sensing payload as example, the functional block diagram is shown in Figure 2. In Figure 2, an optical sensor takes the image and convert optical signal into electrical digital data. Through focal plan assembly (FPA), the data goes to the proposed embedded system. The system controls camera and data flow as well as command and telemetry management with on-board computer (OBC). In the first module of data flow, the data is processed. For optical remote sensing, it usually means “compression”, and sometimes it includes on-board calibration or compensation. Next, data is stored in an external mass storage. According to mission requirement, the real-time simultaneous recording and downlink may be implemented. Finally, the baseband communications is included so that channel coding, randomization and data framing are implemented in the proposed embedded system [3]. Ideally, DAC is also included in the system and the analog signal is outputted to RF component.

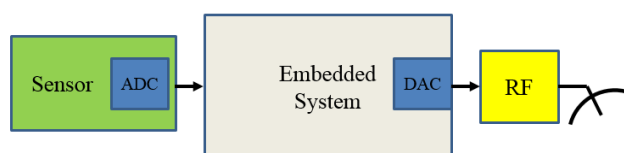


Figure 1 Block diagram of one-embedded system payload including baseband communications.

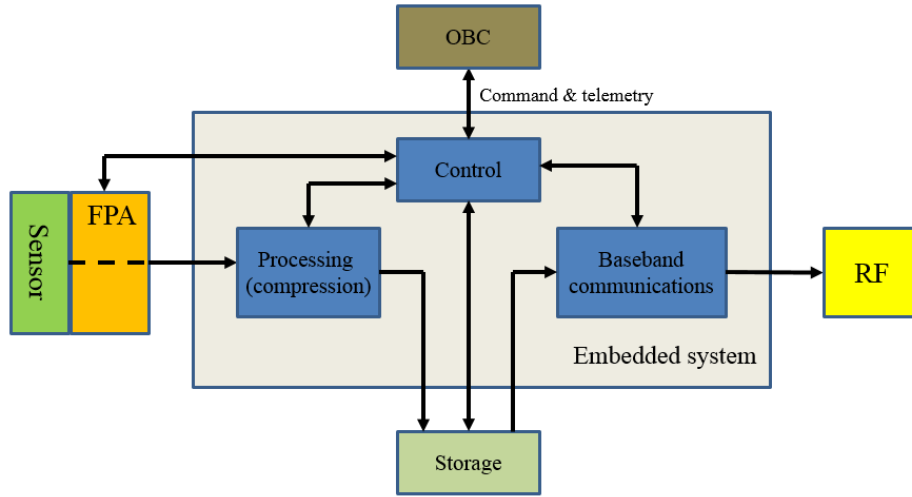


Figure 2 Block diagram of one-embedded system payload.

3. OPTIMIZATION

Traditional approach deals with onboard payload data processing (e. g., compression) and baseband communication separately. However, due to the flexibility of software and the all-in-one design of our approach, the proposed embedded system can optimize the overall performance according to different situations. It can be characterized by the following formula maximizing the performance index.

$$\max_{\substack{\text{algorithms,} \\ \text{parameters}}} \text{Index}(\text{compression}, \text{communication}) \quad (1)$$

In order to understand the idea concretely, we consider an optical remote sensing application requiring simultaneous imaging and downlink. First, let peak-signal-to-noise-ratio (PSNR) be the overall image performance index, compression ratio (CR) as the adjusted compression parameter, and variable coding and modulation (VCM) and adaptive coding and modulation (ACM) as the adjusted baseband communication schemes. In rate-control case, the formula (1) can be specified as

$$\max_{CR, VCM, ACM} \text{PSNR}(CR, VCM, ACM) \quad (2)$$

subject to $\text{BER} \leq \text{threshold}$

and image data rate \leq information downlink rate

In modern data compression for space applications, such as CCSDS122x0B [1], the CR can be adjusted simply by a cut of a bit stream and thus easily to be implemented according to the predicted complexity of imaging scene. Besides, modern telemetry communication for spacecraft downlink incorporates VCM and ACM

scheme with serial concatenated convolutional code (SCCC) such as CCSDS131x2B [2]. Advances in both technology of compression and communications, respectively, make the onboard optimization in (2) become possible. The idea can be explained in Figure 3, when we try to reduce CR to attain a higher PSNR, i. e., compression bit rate (CBR) increases from CBR_1 to CBR_2 , the information bit rate (IBR) in communication increases from IBR_1 to IBR_2 . Because a satellite transmitter always operates at a constant maximal available power, the maximal available bit energy reduces from $(E_b/N_0)_1$ to $(E_b/N_0)_2$. Hence bit error rate (BER) increases. In this case, among various coding and modulation options, we choose the one whose BER lower than the required threshold and meanwhile the resultant information downlink rate is still greater than the information bit rate, i. e.,

$$R \cdot R_c \geq \text{IBR}_2 \quad (3)$$

where R is the overall downlink rate and R_c is code rate. For example in Figure 3, as we assume the rate $R \cdot R_c$ of VCM3/ACM3 is less than IBR_2 , we have only one choice VCM4/ACM4 which meets both requirements. Furthermore, if more than one options meeting both requirements, we need to make a tradeoff. Note that not only parameters, but also the selection of algorithms can be considered in optimization. For example, if the channel (communication) condition is worse and loss of line is intolerable, CCSDS122x0B may not be a good choice because an error bit might induce large propagated damage. In this case, a traditional compression algorithm such as JPEG can be selected. Of course the pre-assumption is the realization of various compression algorithms in the proposed embedded system.

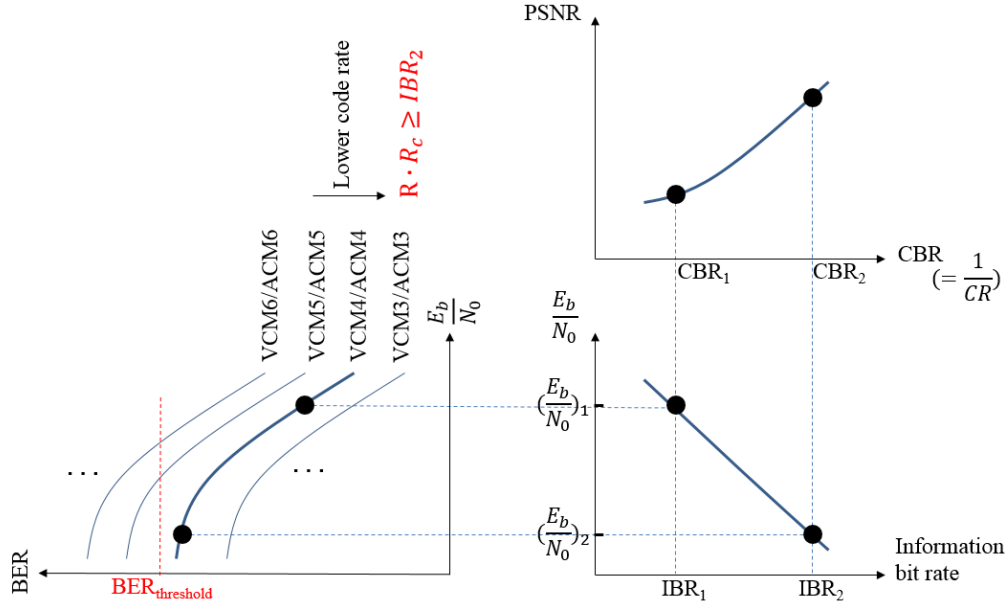


Figure 3 Schematic plot of selections of CR, VCM and ACM to attain maximal PSNR.

4. IMPLEMENTATION

The implementation structure is provided in Figure 4. The proposed system mainly consists of controller modules, processing modules and interface-related modules. Controller modules consists of payload controller (TMTC & house keeping), memory controller for mass storage, downlink controller for baseband communication (CCSDS131x0b2), and sensor timing controller for externally triggering sensor. Next, processing modules consists of compression which may consume most logic and computational resource and digital baseband modulation. Finally, interface-related modules consists of serial-to-parallel dealing with the incoming sensor data to our embedded system, UART between satellite OBC and payload controller, SPI for controlling sensor, SATA, UART and DDR3 memory interface controller. The remaining module, soft error mitigation (SEM) is for the protection of configuration in a space environment. Note that in Figure 4, the payload controller connects to all the components of the embedded system.

5. PROTECTION SCHEME FOR SPACE APPLICATIONS

We consider SRAM-type FPGA, e. g., Xilinx Kintex-7, to implement our proposed embedded system. In this case, it is important to do scrubbing and error

detection and correction (EDAC) to against single-event-upset (SEU) on memory. The configuration SRAM of FPGA may upset in a space radiation environment. Xilinx has developed SEM IP in order to scrub and implement error-detection-and-correction (EDAC) efficiently and repeatedly regarding configuration. With this IP, we can reduce error probability induced by single-event functional interrupt (SEFI).

Another important method reducing single-event errors is to implement Triple-Module-Redundancy (TMR) scheme on FPGA logic because FPGA flip-flop might have SEU. Currently 3rd-party synthesis tool has TMR option when synthesizing FPGA netlist file. Due to simplifying design and reducing required FPGA resource, we do TMR on SPI, command handler, UART IP sensor, timing and downlink controller in order to strengthen system control in space environment. These components are marked “green” in Figure 4. Note that due to speed limit and resource constraint, memory controller does not adopt cell-level TMR.

6. FEASIBILITY

The resource estimation of FPGA (K7-325) is listed in Table 1. Note that because we use an external DDR3 as a supportive memory, we do not need to concern block RAM (BRAM) resource and hence neglect it in Table 1.

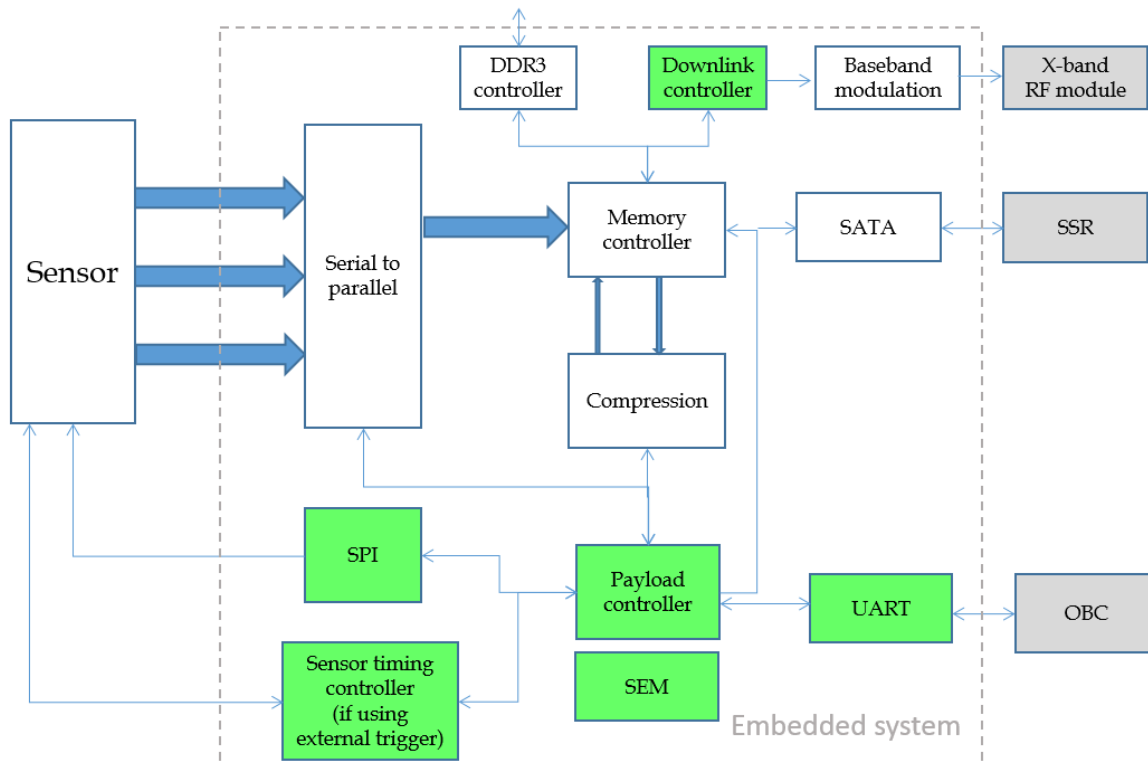


Figure 4 Components of the proposed embedded system.

Table 1: Resource estimation of the proposed embedded system regarding Xilinx K7-325.

	LUT	Flip-flop	DSP
CCSDS122B compression	53%	28%	30%
Payload controller +UART + SPI +sensor timing	4.6%	<1%	<1%
Memory controller	10.4%	5%	<1%
DDR3 controller	8%	2%	<1%
CCSDS downlink (including contorl)	5%	2%	5%
Serial to parallel	3%	<1%	<1%
SATA	3%	2%	<1%

Baseband communications	<1%	<1%	12%
SEM	<1%	<1%	<1%
Accumulated resource required	88%	42%	47%

DISCUSSIONS AND CONCLUSION

We have introduced one-embedded system payload including baseband communications. The flexibility and adaptability of software make onboard optimization according to various tasks become feasible. The concept of optimization is illustrated by optical remote sensing satellite with simultaneous imaging and downlink. The formula in (2) and schematic plot in Figure 3 provides a guideline of optimization. The benefit of incorporating baseband modulation into the payload is revealed in this case.

In addition, we consider Xilinx FPGA, K7-325, to implement our proposed one-embedded system. The protected scheme including scrubbing, EDAC and TMR are described. The feasibility is verified by resource estimation and provided in Table 1. The risk of incorporating as many components as possible into one-embedded system can also be seen here since the resource, i. e., LUT logic cells, become tight.

Finally, it is worth to mention that one-embedded system payload approach greatly reduces hardware requirements and effort when designing payloads for different missions. The eliminated hardware and interface is typically potential difficulties, e. g., parts replacement, interface update and connectors limitations, when adjusting a heritage design to fit a new mission.

Acknowledgments

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