
Contributors

Nicholas Franconi¹,², Sebastian Sabogal¹,², Alan George¹, Munther Hassouneh², Jason Mitchell², Christopher Wilson²

¹University of Pittsburgh, Pittsburgh, PA, USA
²NASA Goddard Space Flight Center, Greenbelt, MD, USA
Overview

- Motivations
- Architectures
- Proposed Architecture
- Developed Approach
- FPGA Resilience
- Conclusions
Motivations

- Rapid growth of SmallSat and CubeSat missions has necessitated re-evaluation of large satellite RF architectures.

- Slow adoption of new technology has limited Software-Defined Radio (SDR) for space applications where commercial world has seen widespread adoption:
  - 4G/5G cellular networks
  - Internet of Things
  - Remote sensing

- Robust, reliable, high-performance, and efficient radios have been specifically identified as enabling NASA technology for future development:
  - Small Satellite Missions for Planetary Science
  - Visions and Voyages planetary science decadal
  - 2015 Technology Roadmap & 2020 Technology Taxonomy
Large satellites have complicated bus architectures with high power requirements resulting from multiple payloads, long mission durations, and internal redundancy.

Communication and remote-sensing systems share common functionality but are designed independently due to disaggregated architecture that leads to sub-optimal SWaP-C.
SmallSat Architectures

- Rapid growth of SmallSat and CubeSat missions has necessitated re-evaluation of large satellite systems.

- Single-Board Computers (SBC) enable substantial computing resources to service multiple functions within CubeSat:
  - S-band and X-band communication
  - Remote Sensing
  - Navigation and Ranging
  - Beamforming Applications

- RF systems can be replaced by software-defined radio (SDR) modules and provide comparable functionality and performance.

- Modular Architecture for Resilient Extensible SmallSats (MARES) developed at NASA Goddard:
  - Highly reliable and flexible architecture to support 3U, 6U and 12U bus configurations
  - Cornerstone is large Xilinx Kintex UltraScale FPGA for instrument processing, communication, and navigation.
Hybrid Space Processors

- Removing on-board processors and FPGAs from individual subsystems allows for **hardware-agnostic designs**

- FPGA partial reconfiguration provides single interface between front-end RF systems and enable broad range of applications

- Enables optimal SDR layout without complications resulting from onboard processor
  - Noisy Regulators
  - Increased Power Efficiency
  - Higher Reliability Components

- Spacecraft designers can fine tune accompanying SBC to best meet mission requirements
  - Multi-card backplane interface
  - Onboard FMC interface

<table>
<thead>
<tr>
<th>Form Factor</th>
<th>Connectivity</th>
<th>Power</th>
<th>Cost</th>
<th>Reconfigurability</th>
</tr>
</thead>
<tbody>
<tr>
<td>3U SpaceVPX</td>
<td>Backplane / FMC+</td>
<td>+++</td>
<td>+++</td>
<td>+++</td>
</tr>
<tr>
<td>CubeSat Card</td>
<td>Backplane</td>
<td>++</td>
<td>++</td>
<td>++</td>
</tr>
<tr>
<td>Standard (CS2)</td>
<td>Lane</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1U</td>
<td>Backplane</td>
<td></td>
<td>++</td>
<td>+</td>
</tr>
</tbody>
</table>

- 48 GB
- 32 GB
- 4 GB
- 4 GB DDR3
- 2 GB DDR3
- 1 GB
- Quad ARM Cortex-A53
- MicroBlaze / RISC-V
- Dual ARM Cortex-A9
- 40 Lanes (12.5 Gbps / Lane)
- 12 Lanes (12.5 Gbps / Lane)
- 8 Lanes (10 Gbps / Lane)

**Benefits**
- Removing on-board processors and FPGAs from individual subsystems allows for hardware-agnostic designs.
- FPGA partial reconfiguration provides single interface between front-end RF systems and enables broad range of applications.
- Enables optimal SDR layout without complications resulting from onboard processor:
  - Noisy Regulators
  - Increased Power Efficiency
  - Higher Reliability Components
- Spacecraft designers can fine-tune accompanying SBC to best meet mission requirements:
  - Multi-card backplane interface
  - Onboard FMC interface

**Features**
- Form Factor: 3U SpaceVPX, CubeSat Card Standard (CS2), 1U
- Storage: 48 GB, 32 GB, 4 GB
- Memory: 4 GB DDR3, 2 GB DDR3, 1 GB
- Processor: Quad ARM Cortex-A53, MicroBlaze / RISC-V, Dual ARM Cortex-A9
- MGTs: 40 Lanes (12.5 Gbps / Lane), 12 Lanes (12.5 Gbps / Lane), 8 Lanes (10 Gbps / Lane)
- Connectivity: Backplane / FMC+, Backplane, Backplane
- Reconfigurability: ++++, ++, +
- Power: ++++, ++, +
- Cost: ++++, ++, +
## Evaluating SDRs and Radios

- Industry has adopted disaggregated communication architecture
  - Many SDRs not suitable outside LEO orbit or have non-optimal noise performance
  - Radios provide higher reliability with limited reprogrammability

- Next generation of SmallSat missions require both reprogrammability and reliability

<table>
<thead>
<tr>
<th>SDR/Radio</th>
<th>Frequency</th>
<th>Bandwidth</th>
<th>Resolution</th>
<th>MIMO TX × RX</th>
<th>Radiation (Estimated)</th>
<th>Processor</th>
<th>Size / Weight</th>
<th>Peak Power RF Transmit</th>
</tr>
</thead>
<tbody>
<tr>
<td>GOMspace NanoCom</td>
<td>70 MHz - 6.0 GHz</td>
<td>56 MHz</td>
<td>TX: 12-bit</td>
<td>4 × 4</td>
<td>20 krad</td>
<td>Zynq 7030</td>
<td>9.0 × 6.6 × 3.1 cm³</td>
<td>15.1 W 8 dBm</td>
</tr>
<tr>
<td>Rincon AstroSDR</td>
<td>70 MHz - 6.0 GHz</td>
<td>56 MHz</td>
<td>TX: 12-bit</td>
<td>2 × 2</td>
<td>25 – 50 krad</td>
<td>Zynq 7045</td>
<td>9.0 × 9.0 × 1.6 cm³</td>
<td>30 W 8 dBm</td>
</tr>
<tr>
<td>Cesium SDR-1001</td>
<td>300 MHz - 6.0 GHz</td>
<td>100 MHz</td>
<td>TX: 14-bit</td>
<td>4 × 4</td>
<td>20 krad</td>
<td>Not Listed (FPGA)</td>
<td>8.7 × 5.0 × 1.3 cm³</td>
<td>14.0 W 7 dBm</td>
</tr>
<tr>
<td>SpaceMicro µSDR-C</td>
<td>150 MHz - 6.0 GHz</td>
<td>56 MHz</td>
<td>TX: 12-bit</td>
<td>1 × 1</td>
<td>50 / 100 krad</td>
<td>Zynq 7020</td>
<td>10.0 × 10.0 × 5.0 cm³</td>
<td>15.5 W 8 dBm</td>
</tr>
<tr>
<td>JPL Iris V2.1</td>
<td>X-band</td>
<td>TX: 256 kbps</td>
<td>3 × 2</td>
<td>5 krad / 15 krad</td>
<td>Virtex 6 (LEON3)</td>
<td>10.0 × 10.0 × 5.6 cm³</td>
<td>35 W 36 dBm</td>
<td></td>
</tr>
<tr>
<td>IQ SpaceCOM X-Link</td>
<td>X-band</td>
<td>TX: 25 Mbps</td>
<td>2 × 2</td>
<td>-</td>
<td>-</td>
<td>9.5 × 6.5 × 2.8 cm³</td>
<td>15 W 27 dBm</td>
<td></td>
</tr>
<tr>
<td>Vulcan NSR-SDR-S/S</td>
<td>S-band</td>
<td>TX: 2 Mbps</td>
<td>1 × 1</td>
<td>-</td>
<td>-</td>
<td>9.2 × 8.2 × 3.4 cm³</td>
<td>15 W 36 dBm</td>
<td></td>
</tr>
<tr>
<td>SDL Cadet Plus</td>
<td>S-band</td>
<td>TX: 3.2Mbps</td>
<td>1 × 1</td>
<td>-</td>
<td>-</td>
<td>10.0 × 10.0 × 2.8 cm³</td>
<td>8 W 33 dBm</td>
<td></td>
</tr>
</tbody>
</table>

- Industry has adopted disaggregated communication architecture
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- Next generation of SmallSat missions require both reprogrammability and reliability
Approach
SDR Specifications

- Dual phase-synchronized Analog AD9361
  - Internal, on-board, and external wideband fractional-N PLL synthesizer
  - 4 × 4 MIMO configuration and simultaneous control of individual channels

- Operating frequency from 70 MHz to 6 GHz
  - 12-bit ADC and DACs
  - Up to 56 MHz channel bandwidth

- High-efficiency noise-optimized power system
  - Remote Sensing: 12W
  - Communication: 5W

- 1U CubeSat Card Standard (CS²) form-factor
  - FMC and backplane connector options
  - Modular capability with wide range of processors

- High-reliability component selection and extensive TID and SEL radiation testing
**SDR and Synthesizers**

- **Hybrid SDR Architecture**
  - 4×4 MIMO architecture with baluns and SMAs with RF loopback for phase coherence
  - Communication to each AD9361 through 18 LVDS pairs providing highest throughput

- **Baseband and RF Synthesizer**
  - Baseband operation from 715 MHz to 1.43 GHz
  - Selectable internal and external synthesizer configurations to allow synchronization depending on mission requirements
Power and PCB

- **Power System**
  - SmallSat bus architecture must be considered in its entirety and commercially available bus architectures providing 12V, 5V, and 3.3V rails
  - Mixture of linear and point-of-load regulators provide efficient conversion and low-noise on supply voltages
  - **Selective regulator population** with rad-hard or rad-tolerant components enables variety of mission environments and cost constraints

- **CS² Standard and Connector**
  - **1U (10 cm × 10 cm) PCB** and connector pinout from CS² for modular system level design
  - Mechanical mount to chassis through either Wedge-Lok or Wedge-Tainer options
  - Class 3DS 22-layer PCB stackup with blind vias
  - Selective connector population for testing and flight capabilities on same hardware
  - FMC provides test-as-you-fly functionality to increase confidence in SW/HW stack
HW/SW Stack

- Operation of each AD9361 requires full hardware / software (HW/SW) stack
  - Integration of System-on-Chip (SoC) architecture provides required performance and reconfigurability
  - Development platforms based on Xilinx Zynq-7000 SoC and Zynq UltraScale+ MPSoC
  - FPGAs implementation through SW stack on softcore processor including MicroBlaze or RISC-V

- FPGA HW stack includes:
  - AXI bus for AD9361 control
    - ADC/DAC processing
    - Delay and TDD
    - Device status and control
  - ADC/DAC DMA, packing, and FIFOs
  - Configurable modulation schemes
FPGA Resilience

- FPGA mitigation of radiation effects
  - Apply **Triple-Modular Redundancy (TMR)** and configuration scrubbing to improve dependability of HW stack

- Procedure
  - Modify reference design to remove non-essential logic
  - Leverage BL-TMR tool for selectively replication of designs at post-synthesis stage to apply fine-grain TMR to modified design
  - Validate operation of SDR with TMR design

- Evaluation framework
  - Developing framework and methodology for evaluating FPGA-based SDR designs through fault-injection
  - Enables formulation of trade-space in terms of performance and dependability
  - Enables development of selective and adaptive strategies for efficient mitigation

### Resource Utilization

<table>
<thead>
<tr>
<th></th>
<th>LUTs (218k)</th>
<th>FFs (437k)</th>
<th>BRAM (545)</th>
<th>DSPs (900)</th>
<th>CRAM (846k)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baseline</td>
<td>10.32%</td>
<td>8.56%</td>
<td>1.83%</td>
<td>7.22%</td>
<td>6.47%</td>
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<tr>
<td>Modified</td>
<td>4.99%</td>
<td>4.98%</td>
<td>1.47%</td>
<td>4.44%</td>
<td>3.68%</td>
</tr>
<tr>
<td>TMR</td>
<td>21.87%</td>
<td>14.92%</td>
<td>4.40%</td>
<td>13.33%</td>
<td>13.23%</td>
</tr>
</tbody>
</table>

**ZC706/FMCOMMS5 Reference Design**

- Baseline
- Modified
- TMR

**Related Logic**
- TX
- RX
- DAC DMA
- ADC DMA
- RM
- TDD
- AD9361 AXI
Conclusions
Conclusions

- Rapid growth of SmallSat missions has necessitated **re-evaluation** of large satellite RF systems.

- Proposed SDR architecture leading to **new generation** of SmallSat missions with tightly integrated remote-sensing, communication and navigation capabilities.

- Presented SDR design framework for SWaP-C optimized SmallSat bus.

- Provides **reliability** for current missions and **performance** for future **AI systems**.
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Questions?

Nicholas Franconi, AST Engineer
NASA Goddard Space Flight Center (GSFC)
Science Data Processing Branch (Code 587)
8800 Greenbelt Rd, Building 23, Greenbelt, MD 20771
Email: Nicholas.Franconi@nasa.gov

Dr. Alan D. George, Department Chair, R&H Mickle Endowed Chair,
Professor of ECE, and NSF SHREC Center Director
NSF Center for Space, High-Performance, and Resilient Computing (SHREC)
ECE Department, University of Pittsburgh
1238D Benedum Hall, 3700 O’Hara Street Pittsburgh, PA 15261 412-624-9664
Email: alan.george@pitt.edu

www.nsf-shrec.org