Open-Source Flight Computer Platform for CubeSats

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I Introduction

Background

This open-source flight computer, the BeaverCube Flight Computer (BFC) was developed for the BeaverCube 3U CubeSat mission. A novel fault detection, isolation and response (FDIR) system was designed to improve CubeSat reliability, along with high data rate imaging payload support and the capability to interface with devices and power through standardized connectors including a PC/104 header.

Mission Objectives

- Measure and track sea-surface temperature and color through infrared and visual spectrum imaging of coastal environments to analyze the correlation of these measurements and events such as ocean sediment deposit and regional sea temperature variations
- Demonstrate an experimental CubeSat electrospray propulsion system

Flight Computer Objectives

Mission Requirements

- Survive 90 days in low Earth orbit (LEO)
- Support a primary and backup radio, antenna control board, electrical power system board, thermal control board, attitude control board, GPS, electrospray propulsion module, imaging payload

Communication and Data Handling Requirements

- Computer recovers autonomously from software faults and non-destructive hardware upsets due to radiation environment
- Provide onboard inertial measurement unit (IMU) and real-time clock (RTC)
- Provide data storage for payload image storage
- Run FSW to coordinate systems and data transfer

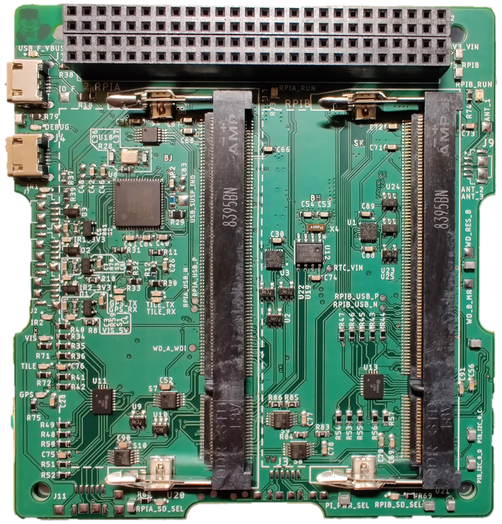

Figure 2: BFC Rev 1.0 top view, T1M series connectors on edge of board not populated

III Key Design Features Implemented

Fault Detection, Isolation and Response

Only one compute module (CM) is running at any time

- Powered-down CM is less susceptible to damage due to radiation bursts
- The primary radio can toggle which CM is running with a command from ground regardless of the flight computer's state

The BFC is single-fault tolerant to a CM or voltage regulator failure

- A non-destructive single event latch-up (SEL) is recoverable autonomously, handled by the watchdog timer on the BFC or electrical power system board
- A destructive failure is recoverable via a ground command

The BFC is triple-fault tolerant to flash memory failure

- Single faults are recoverable autonomously, handled by the watchdog timer and JK flip flop on the BFC
- Multiple faults are recoverable via a ground command

II BeaverCube Flight Computer Block Diagram

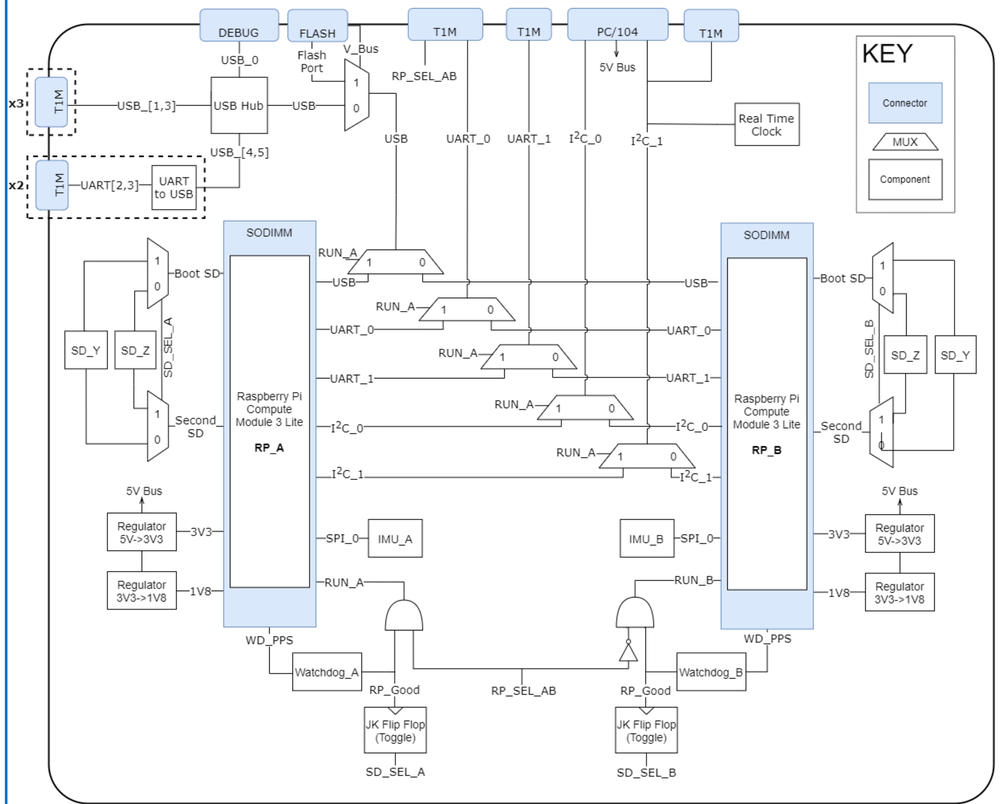

Figure 1: BFC functionality and interfaces, Rev 1.0, April 2020

V Results

BFC Verification

- Testing and verifying the BFC Rev 1.0 against board-level requirements is ongoing as of July 2020
- BeaverCube launch is expected by early 2021

BFC Open-Source Board Files

https://github.com/MIT-STARLab/BeaverCube_Flight_Computer

BFC Specifications	
Processor	BCM2837B0 1.40 GHz
Flash Memory	Micro-SD Card
RAM	1GB LPDDR2
USB Ports	1x Debug
	1x Flash
T1M Connectors	3x USB 2.0
	1x TTL UART -> USB hub
	1x RS-485 UART ->USB hub
	2x TTL UART -> RP GPIO
	1x I2C
PC/104 Connector	2x I2C
	5V, 3.3V, 12V to BFC
Integrated Sensors	1x Real Time Clock
	2x ICM-20948 IMU
Onboard PDU	2x 3.3V Regulator
	2x 1.8V Regulator
Redundancy	2x SD Card per RP
	1x Regulator per RP
	1x IMU per RP

Figure 4: BFC Rev 1.0 specifications

IV FDIR System State Diagram

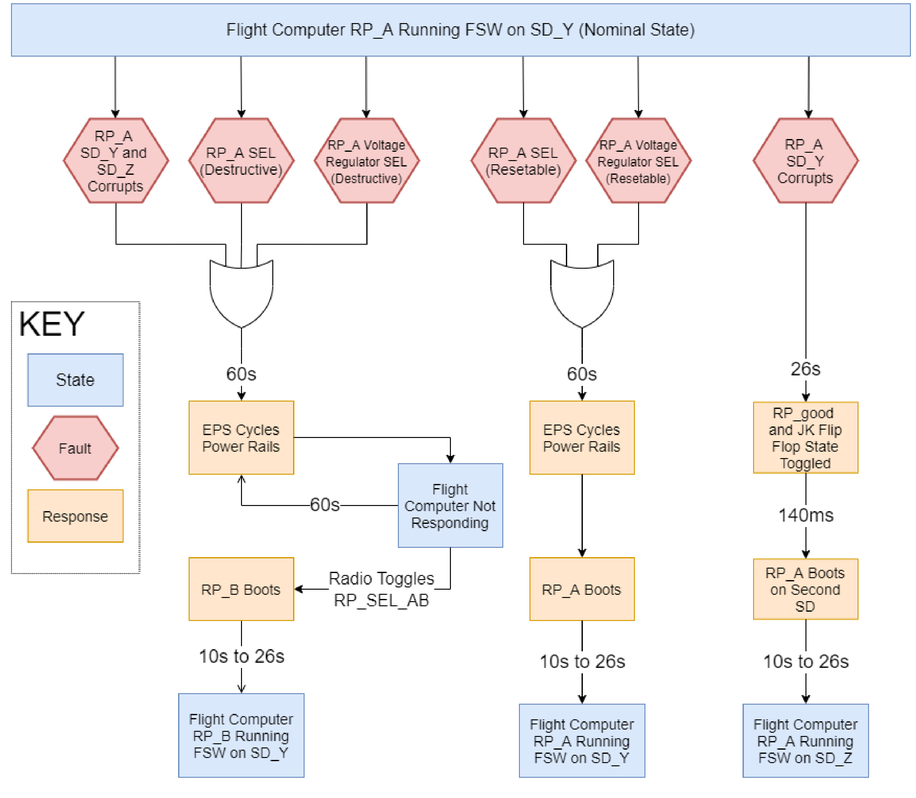

Figure 3: FDIR system overview, with transition time between states indicated in seconds