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Design and Verification of a Clock System for Orbital Radio Interferometry

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ABSTRACT

Radio interferometry using multiple small satellites will enable measurements with high angular resolution for remote sensing and astronomy. The NASA sponsored Auroral Emissions Radio Explorer (AERO) and Vector Interferometry Space Technology using AERO (VISTA) CubeSats will demonstrate orbital interferometry from 0.1 MHz to 15 MHz, frequencies which are largely blocked by the ionosphere. We report on the design and testing of a clock system for radio interferometry between these orbital receivers. We discuss the clock system design up to PCB fabrication, including requirements flow and major hardware trades. The performance of the timing components has been verified using a phase noise test set with a high-quality benchtop crystal. While these results are presented for the AERO-VISTA mission payload, they are more generally applicable to any orbital interferometry platform with multiple satellites.

BACKGROUND

AERO and VISTA Architecture

AERO and VISTA are a pair of identical 6U spacecraft that will measure the radio emissions from Earth's aurora from low earth orbit. The AERO and VISTA spacecraft will operate cooperatively as a pair of interferometric receivers in the HF band by accurately timestamping RF sample data and then downlinking the raw RF data and/or a compressed data product for correlation on the ground.[1,2] This is conceptually similar to the method by which ground based Very Long Baseline Interferometric (VLBI) arrays operate, whereby the data from multiple receivers can be stored and shipped to a different location for correlation and other processing.[8]

The primary payload of each spacecraft is a six-element vector sensor, consisting of three orthogonal loop antennae and two orthogonal dipole antennae, both of which are orthogonal to a monopole. These antennae are deployed from the CubeSat bus on five different booms each about 2 meters in length. These antennae completely sample the electric and magnetic field vector of a propagating RF signal. Despite being electrically small compared to the wavelengths of interest, the phase relationships of the signals on these six elements can be combined to determine polarization and direction of propagation of RF signals that pass over the spacecraft[2,3].

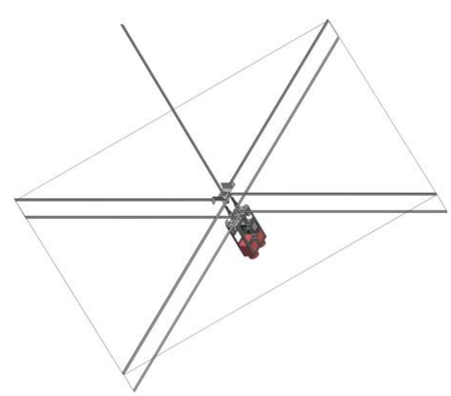

Figure 1: Spacecraft Bus with Deployed Vector Sensor Antennae

Each spacecraft also includes a highly stable reference clock that allows maximization search algorithms to correlate the signals from the two spacecraft on the ground. The correlation of data from multiple receivers increases the vector sensor's ability to resolve multiple sources by increasing the number of independent measurements, and also decreases the angular resolution by increasing the effective receive aperture in one dimension through use of the baseline or separation of the spacecraft.[1-3] This is analogous to how ground based interferometric arrays are resolution limited not by the size of any one receiving antenna, but by the maximum separation of two antennae.[8]

AERO and VISTA Objectives

While AERO and VISTA are identical spacecraft with a strongly overlapping development team, the two spacecraft represent different sets of measurement goals. The objectives of the single AERO spacecraft are closely tied to the space physics of auroral radio emission. The direction-finding and polarimetry capabilities of the vector sensor on AERO allow the spacecraft to measure the radio aurora to answer questions in Space Science. Several primary radio emission targets exist for AERO, including Auroral Kilometric Radiation (AKR), a strong radio source at frequencies up to 750 kHz that is associated with auroral events. AERO will additionally be able to measure and analyze radio emission due to auroral hiss, auroral roar, and medium frequency burst. All of these emission mechanisms are located in the HF bands <= 15 MHz and are spatially complex.[4,5]

The timing requirements for radio interferometry increase with increasing RF frequency, so HF band observations impose a tractable set of requirements. Combined with radio aurora emission qualities of relatively low emission frequencies and spatial complexity, these form an alluring target for measurement by an interferometric array. This match led to the addition of VISTA to the AERO program and its associated interferometric timing requirements. VISTA, together with AERO, will validate vector sensor interferometry in space and will enable vector sensing interferometry of space physics radio emissions that fall below the ionospheric cutoff frequency of about 10 MHz.[1]

INTERFEROMETRIC TIMING

Radio interferometry requires separation in space and synchronization in time. In ground-based interferometry, synchronization is achieved with Hydrogen MASERs, but CubeSats like AERO and VISTA are too small to house Hydrogen MASERs, at least with current technology. Instead a trade is needed between timing requirements and other requirements such as size, weight, and power (SWaP). To intelligently conduct this trade, we analyze here the impacts of timing error on the performance of our interferometric system and further describe how clock source options are characterized.

Characterizing Clock Sources

The two most common methods by which high quality clock sources are characterized are Allan Deviation and the power spectrum of the fractional frequency deviation. The Allan Deviation (σ_y) is a statistical measure which can be understood as the expectation value of the fractional drift of a clock frequency over a given amount of time. The power spectrum of the fractional frequency deviation measures the frequency distribution of phase noise from the oscillator. This measure is given in dBc/Hz at a given frequency and is typically represented as $S_y(f)$, the power at a frequency offset f.[6]

The underlying sources of noise in an oscillator often appear as power law dependencies $\sigma_y^2(\tau) \propto \tau^{\mu}$ where μ is a constant. These dependencies create linear regions when the Allan deviation or spectral power density are plotted on a log-log plot as shown in Figure 2.[6-8]

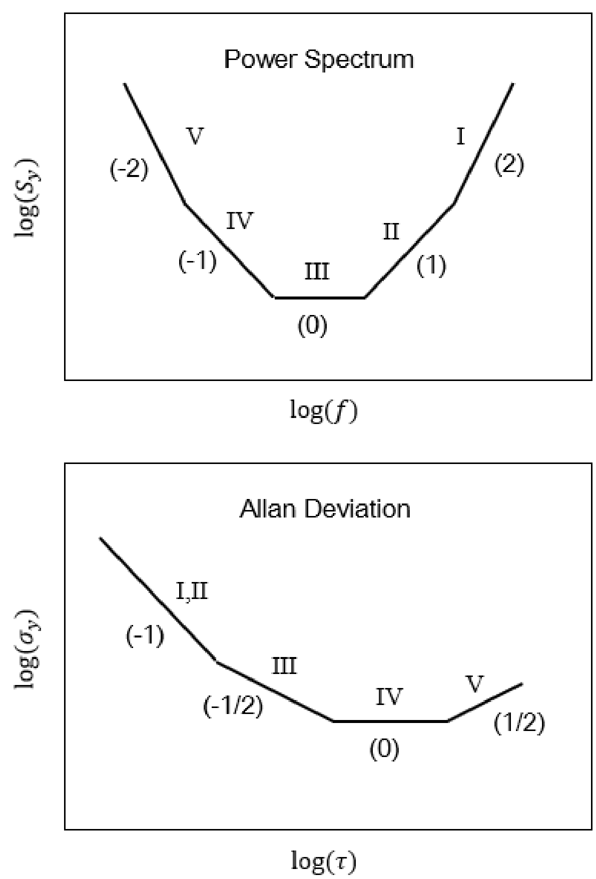

Figure 2: Power Law Linear Regions[8]

The underlying noise processes and scaling relationships are summarized in Table 1.

Table 1: Oscillator Noise Sources

Region	Noise Name	$S_y(f)$ Scaling	$\sigma_y(\tau)$ Scaling
I	White Phase	$\propto f^2$	$\propto \tau^{-2}$
II	Flicker Phase	$\propto f^1$	$\propto \ln(\tau)\tau^{-2}$
III	White Frequency	$\propto$ const.	$\propto \tau^{-1}$
IV	Flicker Frequency	$\propto f^{-1}$	$\propto const.$
V	Random Walk of Frequency	$\propto f^{-2}$	$\propto \tau^1$

Deriving AERO-VISTA Timing Requirements

The AERO-VISTA science team has established high-level requirements that flow into timing system requirements and inform timing system design. The science measurement requires a maximum coherence loss of less than 15%. The worst-case coherence loss occurs for the longest integration time and the highest frequency, defined to be 100 seconds and 15 MHz for AERO-VISTA.

As a zeroth order estimate of the necessary timing requirement we require that the rms phase error be less than one radian of RF phase.[7] This requirement is captured in Equation 1,

$$\sigma_y(T) < \frac{1}{2\pi\nu_0 T} \tag{1}$$

where ν_0 = receive frequency, and T = integration time.

For AERO-VISTA, this expression provides an estimate of 1.06×10^{-10} for the required Allan Deviation at 100 s.

This scaling relationship was used to first estimate the level of effort necessary for the timing system and is a good match to more exhaustive calculations of correlation loss as further described below.

To analyze the impact of the timing source on coherence loss we first must define a model of the clock source. The characterization of frequency stability that follows is defined and well discussed by Barnes et al. (1971);[6] here we only highlight some of the important relationships necessary to estimate timing requirements. Underpinning the entire analysis of frequency stability is the model of an oscillator by

$$V(t) = [V_0 + \epsilon(t)]sin[2\pi\nu_0 t + \varphi(t)] \tag{2}$$

where V_0 and ν_0 are the nominal amplitude and frequency, and $\epsilon(t)$ and $\varphi(t)$ are time dependent amplitude and phase noise sources. When the noise sources are small, the fractional instantaneous frequency deviation from normal is given by:

$$y(t) = \frac{\dot{\varphi}(t)}{2\pi\nu_0} \tag{3}$$

The impact of timing error on correlator performance can be analyzed more precisely by introducing the coherence function defined by Rogers and Moran (1981)[7] as:

$$C(T) = \left|\frac{1}{T}\int_0^T e^{j\varphi(t)}dt\right| \tag{4}$$

Here, $\varphi(t)$ is a characteristic signal of instrument origin caused by the timing error, and is not known a-priori. Accordingly, we will work with the RMS value of this coherence function, which can be calculated from the Allan deviation with the below relation

$$\langle C^2(T)\rangle \simeq \frac{2}{\mathrm{T}}\int_0^T exp\left[-\frac{\omega^2\tau^2}{4}\left(I^2(\tau)\right)\right]\left(1-\frac{\tau}{T}\right)d\tau \tag{5}$$

$$I^2(\tau) = \left(\sigma_y^2(\tau) + \sigma_y^2(2\tau) + \sigma_y^2(4\tau) + \ldots\right) \tag{6}$$

We define the infinite Allan variance series with a function $I^2(\tau)$, the "true variance." Ultimately, the RMS of the correlation function is related to the correlation loss by Equation 7

$$L_C = 1 - \sqrt{\langle C^2(T)\rangle} \tag{7}$$

The Allan variance infinite series in $I^2(\tau)$ converges for the special cases of white phase noise and white frequency noise, and analytic expressions can be used. When the series does not converge, Equation 6 can still be used with a correction to account for post processing of the data products.

In VLBI processing, it is typical to perform a search for maximum correlation, thereby removing static offsets and linear frequency drift from the correlation loss function. The equivalent Allan variation can be approximated as being equal to the real Allan variation up to the averaging time T, with further multiplication of the intrinsic Allan variation by a τ^{-2} high-pass roll-off factor.[7] With this piecewise representation, the infinite series can be evaluated in a tractable manner through numerical integration up to the integration time T, and with analytic evaluation when the series begins to converge at integration times beyond T. This method is limited to cases in which the Allan deviation proportionality is at most linearly increasing with T, but this covers all the major noise sources presented. These equations and resulting possible requirements are shown in Table 2 and the correlation loss functions are plotted in Figure 3.

Table 2: Correlation Loss Analysis

Noise Source	Analysis Type	Analytic Expression for $\langle C^2(T)\rangle$ or $\sigma_y^2(\tau)$ Piecewise Approximation
White Phase	Analytic	$a = 2\pi^2 v_0^2 K_0^2$ (8) $\langle C^2(T)\rangle = \frac{2(e^{-aT} + aT - 1)}{a^2 T^2}$ (9)
Flicker Phase	[b]NA	[b]NA
White Freq.	Analytic	$\langle C^2(T)\rangle = exp\left(-\frac{4\pi^2 v_o^2 K_2^2}{3}\right)$ (10)
Flicker Freq.	Numerical	$\sigma_y^2(\tau) = \begin{cases} \alpha, & \tau < T \\ \alpha T^2 \tau^{-2}, & \tau \geq T \end{cases}$ (11) $\alpha = \sigma_y^2(T)$ (12)
Random Walk of Freq.	Numerical	$\sigma_y^2(\tau) = \begin{cases} \alpha\tau, & \tau < T \\ \alpha T^2 \tau^{-1}, & \tau \geq T \end{cases}$ (13) $\alpha = \frac{\sigma_y^2(T)}{T}$ (14)

[a]Flicker phase differs from white phase only by an log(τ) term and the two are analyzed together

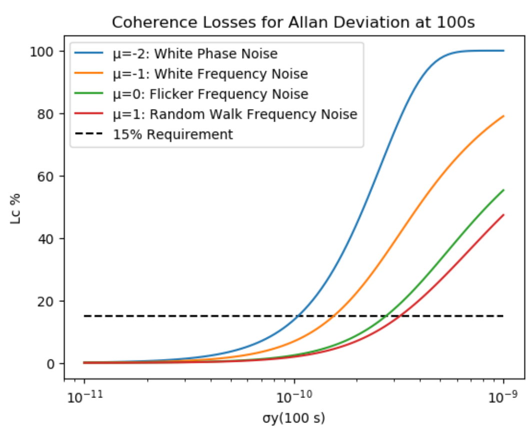

Figure 3: Coherence Loss Allan Deviation Dependence

The exact spectral nature of the oscillator noise among the choices in Table 2 can create up to a factor of 3 deviation in the resulting Allan deviation requirement, from roughly 1×10^{-10} for white phase noise, to roughly 3×10^{-10} for random walk of frequency noise. This does not necessarily mean that a phase noise dominated oscillator is a better oscillator than a frequency walk dominated oscillator, because they are likely to have very different Allan deviations at the integration time of interest. The measured Allan deviations of reference oscillators can vary in practice by many orders of magnitude so the factor of three modification for spectral type is not that significant, and therefore the zeroth order model from earlier is adequate for clock selection in many applications. This analysis together with some input from the AERO-VISTA signal processing team on the impact of the correlation maximization search led to the slightly more relaxed requirement of $\sigma_y(100s) < 5 \times 10^{-10}$.

Table 3: Requirements from Correlation Loss

Noise Source	Resultant Requirement 100 s Allan Deviation
White Phase	$\sigma_y(100s) < 1.06 \times 10^{-10}$
White Frequency	$\sigma_y(100s) < 1.55 \times 10^{-10}$
Flicker Frequency	$\sigma_y(100s) < 2.75 \times 10^{-10}$
Random Walk of Frequency	$\sigma_y(100s) < 3.21 \times 10^{-10}$

Temperature Variation

Most clock sources are measured in a laboratory environment far different than that of a small satellite in low Earth orbit. In particular, the fast temperature variations encountered by the oscillator can add frequency drift that may not be able to be removed by the correlation maximization search. Additionally, the exact frequency dependence of thermally introduced timing error is not characterized in datasheet parameters. To estimate a requirement on the temperature coefficient of the clock source, we can require that the spectral drift caused by temperature variation be less than that of our general clock noise analysis above.

An initial thermal analysis of AERO and VISTA has indicated that a maximum temperature variation over a 100 seconds collection time will be about 1.3 °C. This temperature difference corresponds to moving from eclipse to sun just as a high-power data collection mode is entered. If the resultant frequency drift from thermal variation is to be less than the 5×10^{-10} requirement for oscillator noise, this leads to a required temperature coefficient of $< 6 \times 10^{-10}\ °C^{-1}$.

Jitter and Receiver Noise

In addition to long-term stability requirements, the clock system must exhibit good short-term stability. The clock system is used to discipline an RF analog-to-digital converter (ADC) on each of the antenna channels, and short-term timing error can couple into the signal chain and reduce SNR.[10,11] The short-term error is frequently represented as either phase noise at a frequency offset, or in an integrated time-domain form as jitter. The phase noise plot over offset frequency is a more complete representation of short-term stability as the jitter can be derived from the phase noise, but the opposite is not true.[10]

The requirement for phase noise has been derived from the ADC's SNR degradation with jitter as presented in Figure 4.

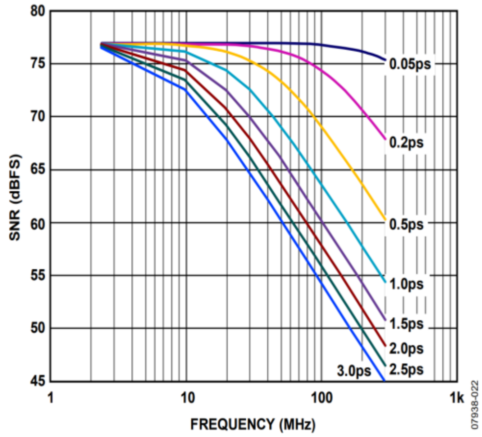

Figure 4: ADC Clock Jitter Impact on SNR[11]

A RF system trade was conducted to determine how much SNR degradation would be acceptable to the signal processing chain at the worst-case frequency of 15 MHz, and the jitter requirement was subsequently set at <1 ps.

Phase noise can also cause problems in Fourier analysis of the incoming signal by causing an otherwise monochromatic source to spread into adjacent frequency bins during the FFT processing. To minimize this effect, an additional requirement of <-110 dBc/Hz at 100 Hz offset was established.

The high-level timing system requirements are summarized in Table 4 for reference in subsequent hardware trade discussions.

Table 4: Clock System Requirements

Parameter	Requirement
Allan Deviation	$\sigma_y^2(100s) < 5 \times 10^{-10}$
Temperature Coefficient	$< 6 \times 10^{-10}\ °C^{-1}$
Integrated Jitter (12 kHz – 20 MHz)	<1 ps
Phase Noise	$< -110\ dBc/Hz$ at 100 Hz offset

CLOCK SYSTEM DESIGN FOR AERO-VISTA

This section details the major development phases in the hardware design of the clock system, including the supporting electronics comprising a vector sensor subsystem known as the Clock Board. The system and board design are broken into the following steps:

1) Selection Trade for major clock system components

2) Supporting Electronics

3) PCB Considerations for High Quality Clocking

4) Expected System Performance

Selection Trade for major clock system components

The major clock system components are a stable reference source and a clock multiplication/distribution device. In very high-performance clock systems, the reference clock source may be directly connected to the sink device to preserve optimal phase noise performance. For AERO-VISTA the phase noise requirements are more modest and multiple clock signals of different frequencies are needed. Therefore, a clock multiplication and distribution component is used to create the system clock from the reference source.

The primary clock reference must meet the timing requirements as well as SWaP constraints typical of Cube Satellites. We start our clock selection processes by looking at some typical Allan Deviation curves for high quality reference clocks.

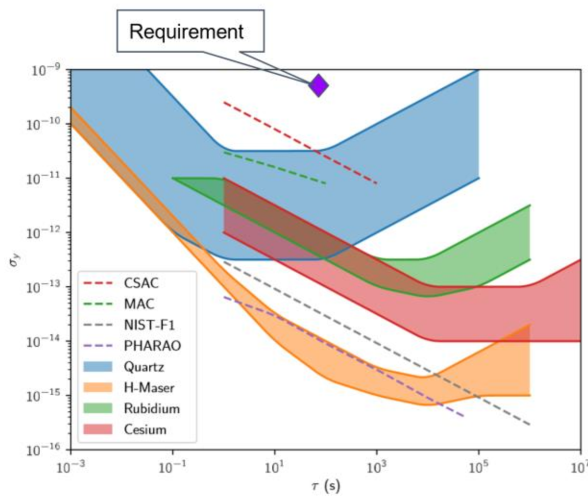

Figure 5: Typical Reference Clock Sources[9]

Here the Allan deviation requirement has been called out with the purple diamond symbol. It is immediately apparent from this plot that all of the high-quality reference clocks presented here could easily meet our Allan Deviation requirement. However, these clocks represent high-quality laboratory reference systems that are generally far too large and power hungry to fly in a small satellite. Additionally, these specifications are collected without regard to temperature variation. Ovenized quartz oscillators can be found in relatively small and low-power packages, but can exhibit adverse temperature coefficients orders of magnitude higher than that of the CSAC.

To meet our temperature stability requirements and fly on a small satellite, two devices were traded early in the design process, the Chip Scale Atomic Clock (CSAC) from MicroSemi[12], and a low-power ovenized oscillator (OCXO) manufactured by Bliley[14].

The critical oscillator parameters based on the datasheets are shown in Table 5: Reference Oscillator Comparison for comparison.

Table 5: Reference Oscillator Comparison

Parameter	CSAC	OCXO
Adev at 100 s	3×10^{-11}	[a]$\sim 8\times 10^{-12} - 8\times 10^{-11}$
Temperature Coefficient	[b]6×10^{-12}	[b,c]6×10^{-10}
Power	120 mW – [d]140 mW	135 mW – [d]350 mW
Volume	16 cm^3	5.9 cm^3

[a]Extrapolated with flicker frequency and random walk frequency noise from Adev at 1s
[b]Linear fit to variation over full temperature range
[c]Corresponds to tightest tolerance available of ±50 ppb
[d]Warmup power

Both devices meet the necessary Allan deviation at 100 s, but the temperature coefficient of the OCXO only marginally meets the derived requirement. The CSAC consumes slightly less power but both devices are comparable in power draw after warmup. The CSAC is significantly larger than the OCXO but slightly shorter in height off the PCB, so may be easier to integrate into a standard payload stack as long as the other components can fit in the remaining PCB area. The CSAC was ultimately selected primarily for its improved stability to temperature variation. The CSAC has the added benefit of being space qualified with flight heritage on a similar CubeSat, the CubeSat Handling of Multisystem Precision Time Transfer (CHOMPTT) mission by the University of Florida in 2018.[15]

The next major component selection involved the clock generation and distribution component. Multiplication of the reference clock signal for the ADC reference frequency requires a PLL with significant programmable controllability since the ADC frequency is not necessarily a multiple of the reference frequency. Additionally, it is desirable to integrate multiple independently programmable output frequencies that are locked to each other with a fixed phase relationship. This is needed to drive the multiple spacecraft clock frequencies in a phase coherent manner to reduce EMI. Finally, the device must achieve low integrated jitter and phase noise. The clock distribution component that meets these requirements is the Analog Devices AD9545. The selection criteria and device parameters are summarized in Table 6: PLL Selection CriteriaTable 6.

Table 6: PLL Selection Criteria

Parameter	Desired Feature	AD9545
Number of Outputs	>2	5 differential or 10 single-ended
Output Configuration	Differential and Single Ended capability	Both Differential and Single Ended capability
Integrated Jitter	<1 ps	< 0.3 ps[a]
Reference Signal Range	Must be driven by 10 MHz, ability to synchronize to 1 PPS desirable	Synchronization to 1 Hz to 750 MHz (including 1 PPS)
Power	Low Power, preferably < 1W	800 mW[b]

[a]Dependant on device configuration and output frequency
[b]Measured with the development kit in the anticipated operating mode

Supporting Electronics

The Clock Board integrates supporting electronics for the control, power, and communication with the major clock system components. Control of the Clock Board is primarily accomplished with a “backplane” SPI bus shared with the rest of the payload electronics. This shared SPI bus is used for low data rate configuration, communication of health and status monitoring data, and power supply domain control. The CSAC uses a UART protocol for configuration so is separate from the backplane SPI.

The Clock Board has three power domains: a block that is always on, a CSAC block, and a PLL block. When not being used as a primary clock source, the PLL block can be turned off to conserve power, and the CSAC can be left on to keep warmed up and keep lock to the GPS reference Pulse Per Second (PPS). Alternatively, the Clock Board can be powered down to all but the health and status electronics by powering down both the PLL and CSAC power domains. This flexibility allows the high-performance clock system to consume less average power but does require careful design and protection of inputs that may be damaged if driven while the component is off. This protection is provided by a simple and low power analog MUX with built-in circuitry to exhibit high input impedance when powered off.

The Clock Board collects health and status monitoring data using circuitry and communications protocols that are standard to all of the AERO-VISTA payload electronics. This data includes voltage of all power domains, current consumption of each independently switchable power domain, and temperature. This data is read over the backplane SPI bus at 10 Hz.

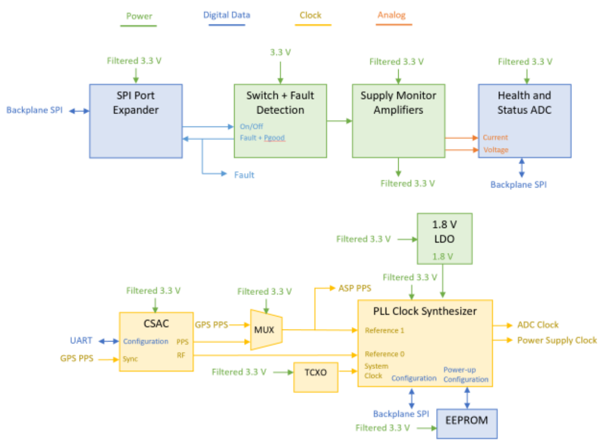

Figure 6: Clock Board Block Diagram

All serial communication with the Clock Board and all transmission of clock signals occurs over a differential pair. Routing serial lines by differential pair reduces EMI from the payload electronics to avoid interference with the primary vector sensor payload. Routing the clock lines as a differential pair helps reduce interference on the vector sensor and also protects the clock lines from noise that may couple from adjacent digital electronics.

PCB Considerations for High Quality Clocking

Once the low jitter and low phase noise clock signal is generated by the AD9545 PLL, it must be protected from degradation by noise and reflections. The clock signal is directly generated by the PLL as a differential pair to eliminate the need for an extra buffer. The clock signal is buffered only once, for distribution at the ADC by a buffer selected specifically for its ultra-low additive clock jitter. In accordance with good mixed-signal practice, the clock signals are routed for maximum signal integrity. The layout of the Clock Board has been specifically optimized for minimum routing length of the clock signals, particularly when single-ended between the CSAC and the PLL.

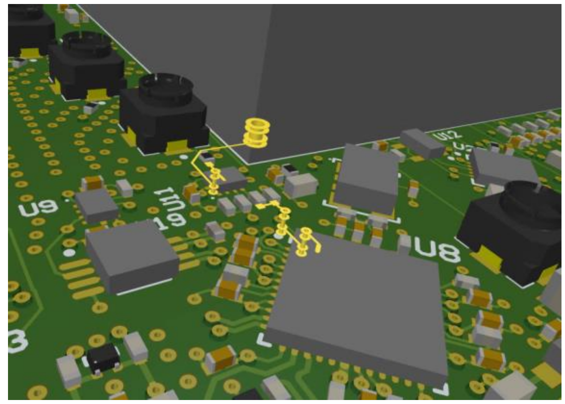

Figure 7: Single Ended Clock Route

In Figure 7 the critical CSAC RF signal is highlighted, before and after the input protection MUX. The total routed electrical length of this signal is 0.8”.

Similarly, the PLL has been placed so that the clock signal is as close as possible to the backplane connector so that the differential route length can be as short as possible as shown in Figure 8.

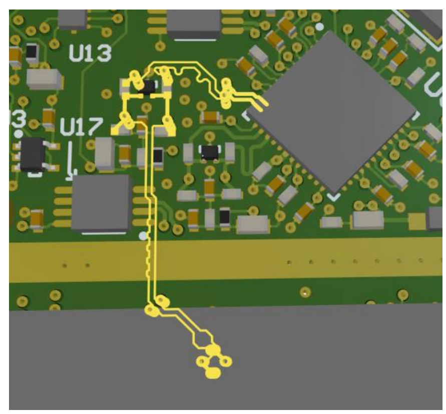

Figure 8: ADC Reference Clock Route

This total electrical length is 1.9” and the differential pair path lengths are matched to within 5 mil or about 0.8 ps.

All mixed-signal routes are placed between two unbroken ground planes with ground plane via stitching and a copper flood fill on the signal layer to shield the clock signals from external interference.

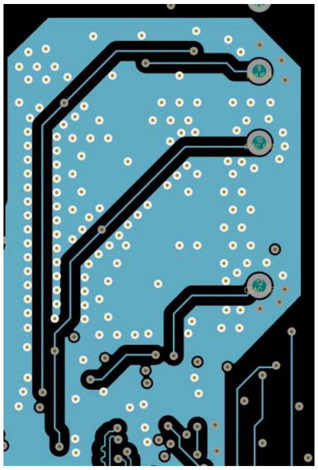

Figure 9: Clock Via Shielding and Flood Fill

Finally, all serial communication signals were routed with minimum plane breaks and always sandwiched between two planes to minimize propagation of electrical noise between board regions.

Expected System Performance

Based on our careful treatment of the clock lines, we can estimate the total system specifications based on the data sheet parameters, and these values are summarized in Table 7. Some of these parameters were estimated with simplifying assumptions or extrapolation of data and will need to be verified with testing.

Table 7: Expected Clock Board Parameters

Parameter	Value
Board Area	50 cm^2
Total Power	1.5 W
Adev (100s)	3×10^{-11}
Tempco	[b]6×10^{-12}
Clock Jitter	0.3 ps
Phase noise at 100 Hz separation	$\sim -110\ dBc/Hz$ at 100 Hz offset

VERIFYING CLOCK SYSTEM PERFORMANCE

Preliminary testing of the major clock system components has been conducted using the CSAC and AD9545 on their respective evaluation boards. The output of the simulated clock system was compared to an ovenized benchtop crystal with a Symmetricom 5115A phase noise measurement test set. This test system is summarized in Figure 10.

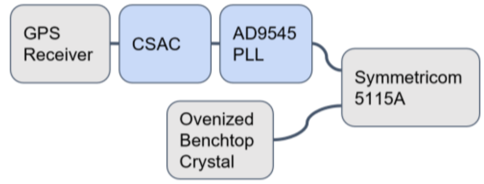

Figure 10: Measurement Block Diagram

To verify the datasheet-advertised long-term stability, Figure 11 plots the observed Allan deviation out to 100 s.

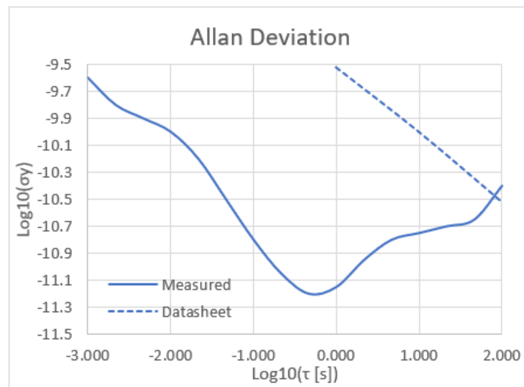

Figure 11: CSAC with PLL Allan Deviation

The plot indicates that the intercept for the white phase noise portion of the Allan deviation plot is nearly two orders of magnitude better than advertised on the datasheet. However, the corner point from white phase noise to random frequency walk occurs at about 1s integration time (0 on the log-scale independent axis), not beyond 1000s as expected.

This behavior is ascribed to the longer time stability of the benchtop crystal, since this test's setup inherently compared one oscillator to another. In particular, as was shown in Figure 5, benchtop crystals can have very low Allan deviations at short integration times but may begin to increase with integration time at about 1 s, similar to the observed test data. Interestingly, despite this inherent reference limitation, we were still able to prove that the Allan deviation at 100 s is better than the required $\sigma_y(100s) < 5 \times 10^{-10}$.

Following the analysis used to derive the timing requirement and using white phase noise for power-law fitting, the expected coherence loss with integration time is plotted in Figure 12. This analysis assumes that the entire frequency spectrum is white noise, which was shown earlier to create the strictest requirements for integration times less than the Allan Deviation measurement period. Conversely, white phase noise is the most best-case assumption for coherence loss at integrations times beyond the Allan Deviation measurement period. Therefore, interpolation beyond 100 s in Figure 12 may be inaccurate, but these results accurately show that the CSAC meets coherence limit requirements up to 100 seconds integration time.

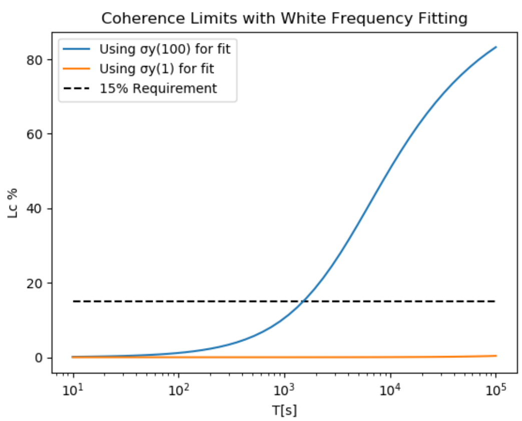

Figure 12: Coherence Limit from Test Results

Future tests will improve on this measurement using the Hydrogen MASER at MIT Haystack Observatory as a frequency reference. Hydrogen MASERs are typically capable of achieving $\sigma_y(100s) < 1 \times 10^{-14}$. This will ultimately allow measurement of the CSAC inherent drift even if our CSAC is operating 100 times more stable than advertised.

The short-term jitter and phase noise at the output of the AD9545 PLL were measured with the same measurement setup in Figure 10, but with the Symmetricom phase noise test set configured to capture phase noise instead of Allan deviation. These results are presented in Figure 13.

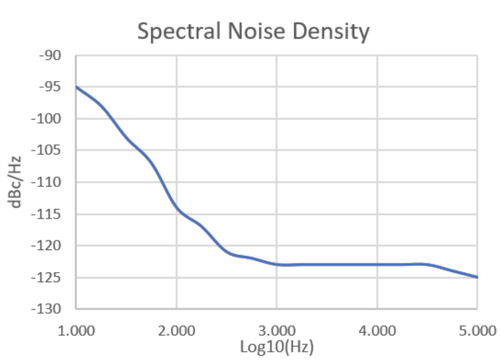

Figure 13: CSAC with PLL Phase Noise

Figure 13 indicates the -110dBc/Hz at 100 Hz spacing requirement has been met. We can integrate the phase noise plot to estimate the time-domain jitter, but this would only represent integrated jitter out to 100 kHz, the bandwidth of the Symmetricom 5115A, a top frequency that is far less than the typical jitter integration bandwidth of 20 MHz. We note that depending on the rate at which phase noise decreases with increasing frequency offset, the integrated jitter can be dominated by close-in phase noise, or could be dominated by broadband frequency noise. Regardless, by integrating the phase noise to 100 kHz, the measured jitter is 0.85 ps. This meets the requirement of <1 ps, but does not leave much margin, particularly when the extra bandwidth must be taken into consideration. This parameter will need to be tested more thoroughly in the future with a wider bandwidth phase noise test set.

Future Verification

A number of future tests are scheduled for the AERO-VISTA Clock Board. Timing performance will be verified before the system is integrated into the full Vector Sensor system for both Allan deviation and phase noise. This test setup will be functionally similar to that shown in Figure 10; however, the CSAC and AD9545 PLL will be integrated onto a single PCB. A test clock output connector has been included on the Clock Card PCB for verification testing. This testing will use a Hydrogen MASER as the reference source and will use a wider bandwidth phase noise test measurement set.

If the Clock Board meets all system requirements, it will be integrated into the rest of the payload for interface testing and full system characterization. If the Clock Board does not meet all timing system requirements, some edits can be made to the PLL configuration for improved phase noise without redesigning the entire system. This is evidenced in the wide range of phase noise plots provided on the AD9545 datasheet for different operating configurations.

CONCLUSION

The timing system for AERO and VISTA will enable a unique demonstration of orbital interferometry with vector sensors. The correlation of data from these spacecraft will enable greater angular resolution measurements for enhanced imaging of the radio aurora.

The timing system requirements have been derived from the science and observation requirements and the selected clock system components are expected to meet these requirements. The unavailability of laboratory equipment in 2020 has prevented full testing of the Clock Board components on the development kits as planned, but data from earlier tests has shown that the Clock Board will likely meet all timing system requirements. Fabrication and full testing of the Clock Board is expected to conclude by the end of Summer 2020, and integration with the rest of the payload and spacecraft bus is expected by the end of calendar year 2020.

The Clock Board is a capable timing system that is stable over both short and long time-scales, and offers a high degree of configurability due to the flexibility of the AD9545. A system similar to the Clock Board could enable other Small Satellite payloads such as Bistatic Radar or precision ranging payloads. Additionally, the lessons learned and design procedure followed for the AERO-VISTA Clock Board will continue to be relevant as higher quality CSACs and PLLs are developed. The development of ever better oscillators in small SWaP payloads will make cooperative swarms of small coherently synchronized satellites an affordable and attractive option for remote sensing and astronomy applications.

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References

1. Lind, F. D. et al., "AERO & VISTA: Demonstrating HF Radio Interferometry with Vector Sensors," 33rd Annual AIAA/USU Conference on Small Satellites, 2019.
2. Erickson, P. J. et al., "AERO: Auroral Emissions Radio Observer," 32nd Annual AIAA/USU Conference on Small Satellites, 2018.
3. Knapp, M. et al., "Vector Antenna and Maximum Likelihood Imaging for Radio Astronomy," IEEE Aerospace, 2016.
4. LaBelle, J., and R. A. Treumann, "Auroral Radio Emissions, 1. Hisses, Roars, and Bursts," Space Sci. Rev., 101, 295--440, 2002.
5. Gurnett, D. A., "The Earth as a radio source: Terrestrial kilometric radiation," J. Geophys. Res., 71, 5599, 1974.
6. Barnes, J. A. et al., "Characterization of Frequency Stability," IEEE Transactions on Instrumentation and Measurement, vol. IM-20, no. 2, pp. 105-120, May 1971.
7. Rogers, A. E. E. and J. M. Moran, "Coherence limits for very-long-baseline interferometry," IEEE Transactions on Instrumentation and Measurement, vol. IM-30, no. 4, pp. 283-286, Dec. 1981.
8. Thompson, A., J. M. Moran and G. Swenson Jr, "Interferometry And Synthesis In Radio Astronomy." 3rd ed. Cham, Switzerland: Springer Open, pp.425-448., 2017.
9. Serra, P., "Integrated, Low-Power Sub-Nanosecond Timing Systems for Space Navigation and Communication" Ph.D. University of Florida. 2018.
10. Kester, W., *Converting Oscillator Phase Noise To Time Jitter*. Analog.com. Available at: https://www.analog.com/media/en/training-seminars/tutorials/MT-008.pdf, 2009.
11. Analog Devices, *AD9269 Datasheet and Product Information*. Available at: https://www.analog.com/media/en/technical-documentation/data-sheets/AD9269.pdf, 2016.
12. Microsemi.com. *SA.45S CSAC And ROHS CSAC Options 001 And 003*. Available at: https://www.microsemi.com/document-portal/doc_download/133305-sa-45s-csac-datasheet, 2019.
13. Analog Devices, *AD9545 Datasheet And Product Information*. Available at: https://www.analog.com/en/products/ad9545 .html, 2018.
14. Bliley Technologies, Inc. *LP-J Low Power OCXO*. Available at: https://resources.bliley.com/lp-j-low-power-oscillator-ocxo
15. Conklin, J. W. et al., "Preliminary results from the CHOMPTT laser time-transfer mission," 33rd Annual AIAA/USU Conference on Small Satellites, 2019.