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SpaceVPX/FMC for Electronics Standardization and Modularity in High-Performance SmallSat Architectures

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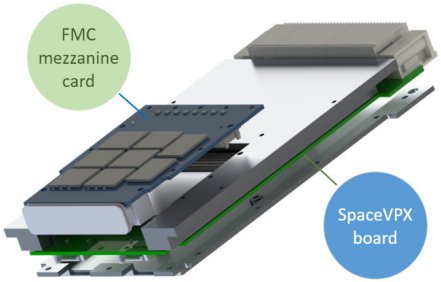
ABSTRACT

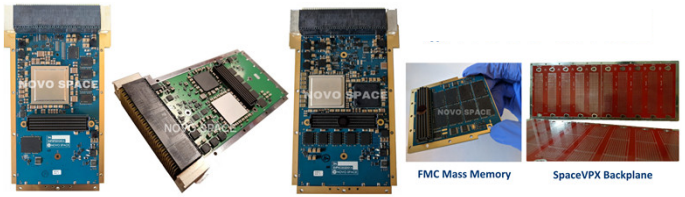
A general-purpose architecture combining the SpaceVPX[1] and FMC[2] open standards is proposed for future high-performance space systems[3] in the 10 to 500 kg range. This modular architecture promotes the reuse of components across subsystems reducing mission risk, cost, and development time. The data throughput of the selected standards supports modern high-bandwidth payloads such as high-resolution cameras, communication systems, and synthetic-aperture radars. This architecture also favors a high level of integration of payload and avionics subsystems enabling high levels of reliability and low SWaP. The small SpaceVPX 3U form factor (100 mm wide) enables high-performance systems with low volume, but the limited User Defined (UD) pins to the Backplane can become a bottleneck in the system. The introduction of the FMC standard makes it possible to circumvent the UD pin limitations and implement Input/Output (IO) mezzanine modules as an alternative to Rear Transition Modules (RTMs). The FMC can also be used for more complex functionalities to provide an extra layer of configurability to the system, implementing functions such as mass storage and digitization. When the FMC is not used for IO and more UD interfaces are needed, unused pins can be repurposed and routed through the Backplane to an IO board.

INTRODUCTION

The modularity defined in the SpaceVPX standard is adequate for the conceptualization of different applications, though the division in sub-functions increases the SWaP and cost of the systems. Combining multiple functions into single modules reduces SWaP, but decreases the flexibility of each module. The number of applications, and hence, the space heritage of the products, would be reduced if the modules are not flexible enough. To reduce SWaP and simultaneously increase both flexibility and modularity, we propose an architecture combining the VITA 78 SpaceVPX standard with the VITA 57 FMC (FPGA Mezzanine Card) standard. This combination will allow rapid deployment with minimum redesigns. Additionally, the FMC standard offers the flexibility to add mission-specific hardware to the system, limiting the non-recurring engineering (NRE) to the mezzanine card.



The photos below show some of the components developed by Novo Space following this configuration.



THE PROBLEM

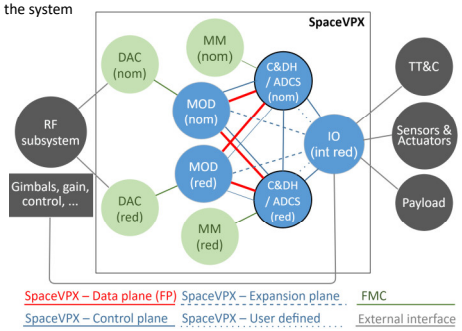
The SpaceVPX standard defines two form factors: 3U cards are 100 mm wide and 6U cards are 200 mm wide. The 3U form factor allows for small SWaP systems. Our initial estimations show that the combination of custom heatsinks with wedge locks provide ample thermal dissipation and does not constrain the processing power of the board for most applications. The main issue with 3U systems is the number of UD pins available in the system. This can be an issue when a system needs a dumb peripheral board or an RTM module on the back of the Backplane connected through these UD pins to the SpaceVPX module. This is the case when cycle accurate synchronism signals are needed or when there is no IO expansion device in the peripheral or RTM module. This could prevent the Controller of the SpaceVPX chassis from implementing any interface beyond the ones defined in the standard, becoming a roadblock in most systems.

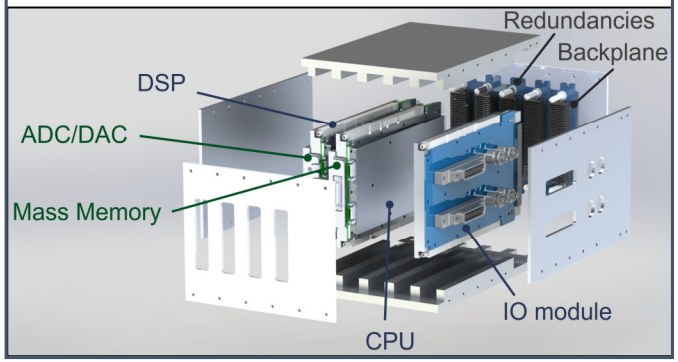
RECOMMENDATIONS

SpaceVPX 3U profiles are preferred over 6U profiles to reduce SWaP; however, there are two issues with this form factor: small number of User Defined pins and limited standard Backplane topologies. The following are recommendations that could be used to address these two concerns:

- ❑ Be open to custom Backplanes
- ❑ Though not considered in the SpaceVPX standard, select single string when risk profile allows it.
- ❑ Select components capable of repurposing the Control Plane signals
- ❑ Use boards capable of splitting the Pipes of the Data Plane
- ❑ Use FMCs to circumvent the limited number of UD pins
- ❑ If needed, add an IO slot to the system

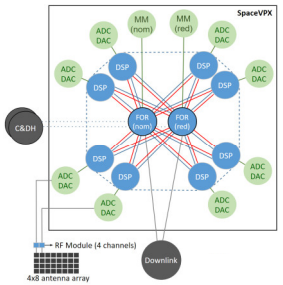
The diagram on the right presents the architecture of a Fully Redundant Avionics Subsystem with integrated downlink following the recommendations listed above and the image below shows a rendering of the same subsystem.



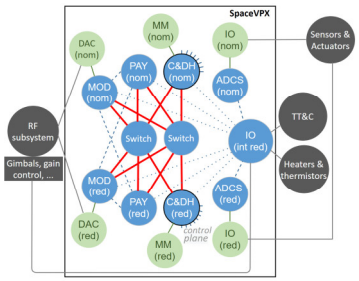


CASE STUDIES

The architecture of the two systems below strictly follow the definitions in the SpaceVPX standard.

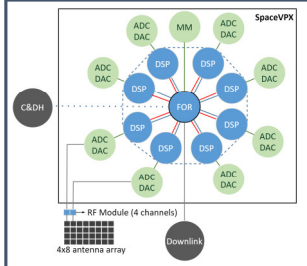


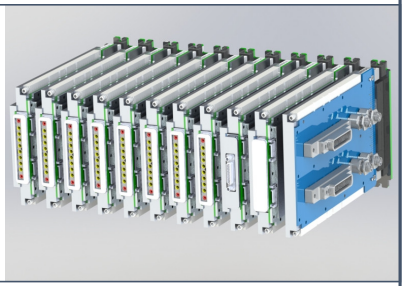
Synthetic-Aperture Radar with Star Topology Backplane and Redundant Controller



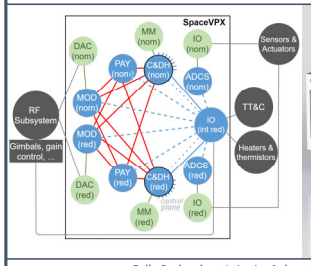
Fully Redundant Avionics Subsystem and Payload with Dual Star Topology Backplane

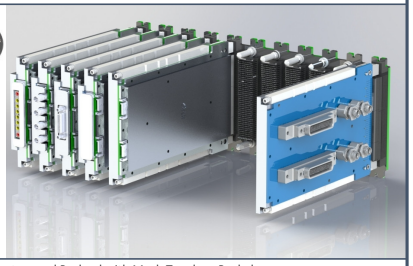
The next two systems follow the recommendations presented in this work. In both cases there is a reduction in complexity and volume when compared with the previous two systems.





Synthetic-Aperture Radar with Star Topology Backplane





Fully Redundant Avionics Subsystem and Payload with Mesh Topology Backplane

REFERENCES

1. "ANSI/VITA 78.00-2015 SpaceVPX System", April 2015
2. "ANSI/VITA 57.1 FPGA Mezzanine Card (FMC) Standard", July 2008 (Revised February 2010)
3. Diez, R, Jorge, F, Cahoy, K, Collier, P, SpaceVPX/FMC for Electronics Standardization and Modularity in High-Performance SmallSat Architectures, SSC20-P1-09, August 2020, 34th Annual Small Satellite Conference