**Introduction**

Argotec HACK OBC offers unprecedented flexibility thanks to its design developed from scratch to be modular and easily reconfigurable. Different standard modules, based on both state-of-the-art SoCs and FPGAs, can be assembled without the need of external harness to face a wide variety of applications, from spacecraft management to hardware acceleration. The design leverages a mix of rad-hard, defense-grade and automotive components carefully selected to enable the execution of demanding edge-computing tasks while ensuring a reliability level significantly higher than standard CubeSat avionics. Each HACK module is designed to be powered by a single +5V DC rail and has standardized thermal and mechanical interfaces, allowing the installation both as single unit or as part of a complex OBC subsystem. The standard configuration, which includes one Core Board and one accelerator Module, has a volume of about 0.5U and offers unmatched performance and interfaces.

**System Description**

The HACK module general block diagram is shown in Figure 1. It shows one of the OBC possible configurations since the subsystem has been designed to be modular and reconfigurable according to mission-specific needs. The OBC design includes two principal hardware units:

- The Core Board (CB), which hosts the main SoC that runs the OSW
- The accelerator Module (aXM), which act as both mass memory controller and chipset in order to supply additional interfaces to the CB; optionally, the aXM FPGA could be used to implement mission-specific hardware accelerators

A third module, labelled as Router Board (RB), has been planned as well. The RB can be used for configurations requiring more than one CB and two aXM.

**Module to Module Connection**

Direct stacking of different HACK Module
- **GPO** - to trigger discrete functions
- **CAN** - to manage board-to-board TM and TC
- **I2C** - restricted to TM collection or CAN bus backup
- **SpaceWire** – point-to-point link between boards

Configured with a Router Board (RB)
- Increase SpaceWire links
- Increase the number of Boards

**Core Board**

- **Volume:** 100x123x23mm (chassis included)
- **Mass:** <300g
- **2x Stackable connectors** (2xSpWr, 1xCAN, 1xI2C, 6xSE input, 10xSE output)
- **7x MicroD connectors** (2xUART, 2xSpWr, 1xI2C, 1xRS232-485, 4xSE input, 4xSE output)
- **Power consumption (nominal configuration):** ≈ 3W
- **1x Processor:** 4x32bit cores, clock 600MHz, 2100 MIPS @600MHz, 900 MFLOPS @600MHz
- **3x DDR2 memory:** 3Gbit, CPU main memory during OSW execution
- **2x Flash memory:** 128Mbit which stores the boot image of the OSW
- **Radiation Hardened SoC + Error Corrected Memories**

**aXelerator Module**

- **Volume:** 100x123x23mm (chassis included)
- **Mass:** <300g
- **2x Stackable connectors**
- **7x MicroD connectors** (2xUART, 3xSpWr, 1xSPI, 1xCAN, 1xUART, 2xI2C, 2xRS232-485, 4xSE input, 4xRS485)
- **Power consumption (nominal configuration):** ≈ 8W
- **1x FPGA:** SRAM based - run time reconfigurable – 1540 DPS slices
- **1600MHz DDR3 memory**
- **1x NOR Flash memory:** 256Mb which stores the FPGA bitstream
- **2x NAND Flash memory:** 256Gbit
- **Defence Grade FPGA (with SEU mitigation) + Radiation Hardened Mass Memories**

**HACK Modular On-Board Computer**

for Edge Computing in Micro-Satellites

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