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Results from Testing Low-Cost, High-Performance Terrestrial Processors for Use in Low-Cost High-Performance Space Missions

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ABSTRACT

There has been a significant and exciting increase in the use of microsatellites and cubesats in the past decade.

However, it has proved difficult to scale up current cubesat avionics systems to enable larger, longer, more complex missions, and challenging to scale down traditional microsatellites to an affordable price point. The need exists for a system that provides the capability of a microsatellite at a cubesat cost; KISPE Space ("KISPE") is developing the Next Generation Microsatellite Platform ("NGMP") to address this need and is releasing the design as an open source resource via the Open Source Satellite Programme ("OSSAT")

A key enabler of developing a robust Next Generation Microsatellite Platform is the identification of a suitable low-cost microprocessor that can be used to form the foundation of an affordable, robust, flexible, performant and autonomous satellite platform avionics system.

Space-qualified, long-lifetime, radiation-tolerant (or hardened) processors do exist, however, these technologies are very expensive and tend to deliver poor mission performance compared to the latest terrestrial Commercial-Off-The-Shelf (COTS) components and are not compatible with the limited resources available from cubesats and smallsats.

We performed a test campaign to identify one or more commercially available microprocessors that leverage the latest innovations in microprocessor technology and which meet a set of system criteria that make them suitable for use as a microsatellite platform processor for a wide range of missions; from single modest spacecraft, through to proliferated architectures requiring autonomous operations.

We are sharing these test results freely with the space community to advance small satellite capabilities and to stimulate the development of the next wave of cost-effective missions, applications and services.

Three COTS processors (SAMV71, STM32H7 and SAMA5D3) were downselected for Total Ionising Dose (electron) radiation testing to characterize their performance in a representative space radiation environment, in partnership with the University of Surrey and with the input of OSSA T collaborators. All three processors were deemed to be candidates for further evaluation and derisking: The devices began to fail at 60kRads, 47kRads and in excess of 120kRads respectively.

INTRODUCTION TO THE OPEN SOURCE SATELLITE PROGRAMME

KISPE Space Systems Limited ("KISPE") is developing the Next Generation Microsatellite Platform (NGMP), to deliver microsatellite-level performance for a cubesat cost – to solve the affordability challenge that exists in the space industry today. In order to stimulate the market and to solve the accessibility challenge, KISPE is releasing the NGMP platform design as an open source resource for all to freely access and utilize, via the Open Source Satellite Programme [1] under the "OSSAT" branding.

The Open Source Satellite Programme is creating a community of individuals, teams and organisations who are contributing to the development of OSSAT [1]

A key enabler of developing a robust, next-generation microsatellite platform is the identification of a suitable microprocessor that can be used to form the foundation of a robust, flexible and performant satellite platform avionics system.

The main task will be to identify one or more commercially available microprocessors that leverage the latest innovations in microprocessor technology and meet a set of criteria that make them suitable for use as the Open Source Satellites platform processor.

THE PURPOSE OF THE TESTING

One of the key components of the Open Source Satellite (OSSAT) command and data handling system is the microprocessor for the On Board Computer (OBC). Microprocessors that have been designed to be radiation-hardened for the harsh space environment are expensive and tend to have poor performance compared to Commercial-Off-The-Shelf (COTS) equivalents that leverage the latest innovations in microprocessor technology. The OSSAT team possesses decades of experience in using COTS components in Low Earth Orbit (LEO) and intends to leverage the capabilities of the latest terrestrial technology in the development of the OSSAT platform computer.

The OSSAT team performed a research and development project to further the understanding of COTS processors, in partnership with the Surrey Space Centre (SSC) at the University of Surrey, UK, with support from Research England's SPRINT programme1. The OSSAT-SSC project team evaluated the latest available COTS microprocessors2 and assessed their suitability in terms of performance with a view to test their resilience to the harsh space radiation environment. Three COTS processors were downselected and subjected to a series of research tests to determine processor performance and space environmental resilience.

PROCESSOR SELECTION

Several quantitative and qualitative criteria were defined in order to evaluate a suitable microprocessor to integrate into the OSSAT platform. These criteria are listed in descending order of importance.

Quantitative Criteria

The following quantitative criteria were used in the evaluation; the results of the evaluation are summarized in Figure 7.

Quantitative Microprocessor Downselection criteria	
Performance	At least 200DMIPS
Program Memory Requirement	At least 50MB
Data Memory Requirement	At least 64MB
Mass Memory Requirement	At least 4GB
Thermal	The processor must be able to fully operate between -40 to +85 degrees C.

Table 1: Quantitative Selection Criteria

Qualitative Criteria

A number of other features and properties are relevant to the platform processor selection, including:

5.2.1 External Memory Interfaces

SEU memory protection can be implemented off-chip in hardware if the chip supports external memory interfaces.

5.2.2 Existing Radiation Tolerance data

Any existing data about the radiation tolerance of the processor would be beneficial. Furthermore, some parts have pin compatible radiation tolerant equivalents. These parts are potentially more relevant because the radiation tolerant equivalent part could be used for "beyond LEO" missions without needing to re-engineer these core elements of the platform software or PCB layout.

5.2.3 Existing SEU Protection

As the feature size of components has reduced, commercial processors have become susceptible to SEUs even when used in terrestrial applications. Therefore, some vendors have introduced error detection or error detection and correction technology into the silicon. Availability of SEU mitigation, such as single bit per word error detection and correction, is an important consideration.

5.2.4 Development Tool Compatibility

The availability of tools to aid the development of software for the processor and to model power

consumption was considered, as was whether the tools are open source, whether support is available for a fee, and how large the userbase is.

5.2.5 RTOS availability

The quantity of Real Time Operating Systems (RTOS's) that support the processor was assessed, as was whether the RTOS's are open source.

5.2.6 Field-Programmable Gate Array (FPGA) configurability

FPGAs offer an extra degree of reconfigurability. FPGAs with embedded processors were therefore preferred and any FPGA hardware noted during the selection.

5.2.7 Cyclic Redundancy Check (CRC) Generation

Existence of hardware acceleration of CRC generation was evaluated because CRC generation will be a common task of the platform processor. It should be noted that the use of CRC protection should be weighed up against error detection and correction for communications interfaces.

5.2.8 Encryption/Decryption AES256

Existence of hardware acceleration to aid cipher/decipher was evaluated in order to satisfy the requirement for encryption to AES256: NOTE: the adoption of encryption must be weighed against power consumption, message sizes and the resulting effect on bit error rate.

5.2.9 Authentication

Whether or not the processor includes hardware acceleration that aids authentication was assessed. This was considered because communications with the ground will need to be authenticated.

5.2.10 Flight Heritage

Previous in-orbit data, and information on the type of mission, if available, was evaluated.

5.2.11 Obsolescence

Production runs of components can be very short. This largely depends upon the industry for which the processor is manufactured. Chips manufactured for the automotive and aerospace industries are attractive because of the very long production runs, allowing the same components to be used across a series of different missions without needing to redesign the system.

5.2.12 Interfacing

The types and quantities of I/O interfaces that are supported by the chip was considered. Should specific technologies not be supported by the chip, supplementary devices.

THE DOWNSELECTED DEVICES

SAMV71 (Part ATSAMV71Q21)

This is a high-end single core micro-controller, manufactured by Microchip Technology Inc. It has a low power ARM Cortex M7 32-bit core and many peripherals. It is a very popular and versatile chip that is designed for the automotive industry and costs approximately $15. This chip is particularly attractive because a radiation tolerant equivalent is also available from Microchip at around $4,000 per chip. Therefore, the commercial part could be used for LEO orbits and the Rad tolerant variant for harsh environments with minimal changes to the software and PCB layout.

NOTE: The SAMV71 can only satisfy the mass memory requirement by using I/O outside of the memory controllers to address enough memory or by incorporating SD memory/MMC memory.

STM32H7 (Part STM32H753ZI)

This is a very high-performance microcontroller with an ARM Cortex M7 core. It boasts 1027 DMIPS, consuming only 155mW during our test. This was one of the fastest processors we analysed for the platform computer that satisfied the criteria. It also has extensive ECC protection and fairly extensive memory interfacing. It satisfies all but the memory criteria.

SAMA5D3 (Part ATSAMA5D35A-CN)

This is a high performance processor that can achieve 800 DMIPS whilst consuming a low amount of power. It incorporates an ARM A5 32 bit core. It has a strong capability with respect to memory interfacing, including a static memory controller with built in ECC. This processor has been baselined for a few space missions include AAReST and at least one Cubesat mission.

TOTAL IONISING DOSE RADIATION TESTING

Test Facility

The Realistic Electron Environment Facility (REEF), located at the University of Surrey, UK, and operated by research colleagues from SSC exposes samples in vacuum to a ~2.5 GBq Sr-90 source. Strontium-90 provides an excellent practical option for the provision of long-duration, low-intensity exposures as it allows

uninterrupted irradiations over the required long periods with an electron spectrum that is appropriately representative of the real space environment.

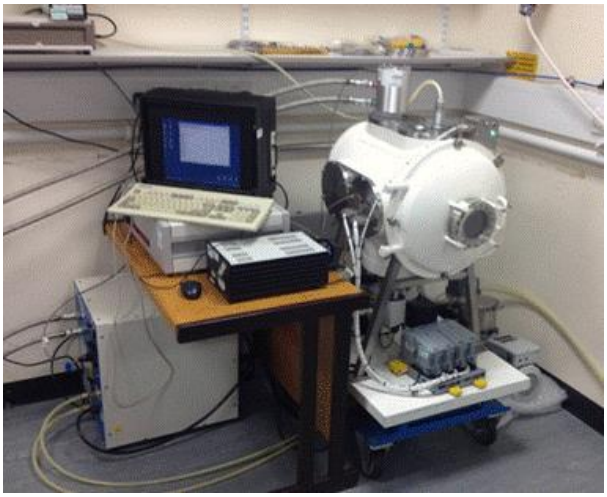

Figure 1: REEF equipment at the University of Surrey

The REEF can be used to test materials and components for their vulnerability to both internal charging and total ionising dose phenomena. The dose rate is proportional to electron current and thus is primarily determined by the source-to-sample separation distance in the experimental setup. Changes to the electron spectrum due change due to component shielding.

The dynamic range of normal incident electron current achievable with REEF is wide, ranging from ~6 pA/cm^2 at low (~3.5 cm) source-sample separation to ~0.3 pA/cm^2 at high source-sample separation (~16 cm). Higher currents can in theory be achieved at even smaller separations, though this would be at the expense of the assumption of normal incidence irradiation. Further reductions in current are achieved by adding planar aluminium shielding in between the source and sample.

The processor components to undergo testing were exposed to radiation equivalent to a 10 year, 800km, sun synchronous LEO mission. Upon completion of the REEF test for each board, any boards that showed forms of damage were tested again outside REEF to test for any potential annealing effects following irradiation.

The Target Under Test

In order to generate statistically relevant information, four evaluation boards per downselected chip (the "Target") were irradiated.

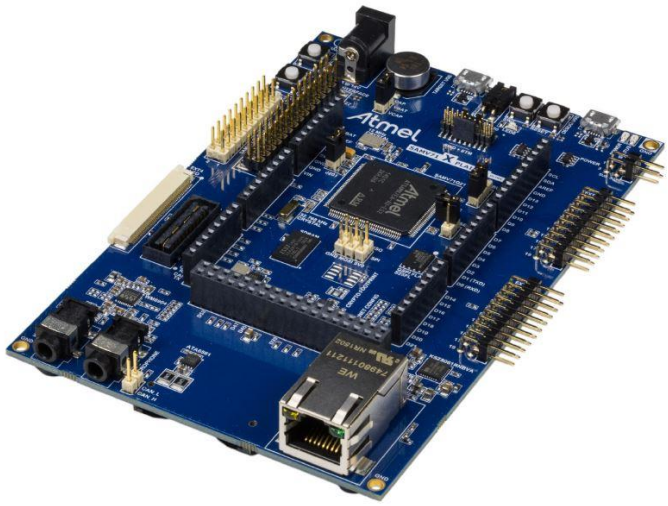

Figure 2: SAMV71 Xplained Eval board. Image Credit: Microchip

The intent of the test was to assess the radiation tolerance of the processor only, therefore the rest of the components were shielded from the radiation source as shown in Figure 3.

Figure 3: SAMV71 behind an aluminium shield

Each evaluation board was placed inside REEF and the radiation source positioned in order to test at a 1 kRad/hr dose rate as shown in Figure 4.

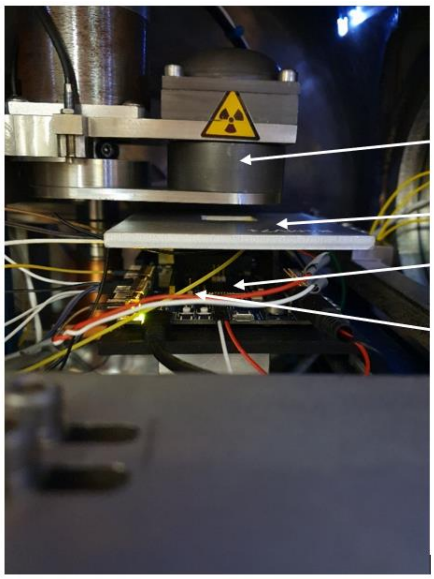

Figure 4: SAMV71 inside REEF

Target Software

The target processor was powered during irradiation. It ran software exercising various I/O interfaces and memories. The Test cycle repeated autonomously as illustrated in Figure 5 (NOTE: the wait between tests was reduced to 3 seconds in contrast to this figure. The original rationale for 30 seconds related to the anticipated time required to ensure a current & voltage measurement during the test. However, the current and voltage measurement mechanism proved faster than anticipated).

The tests were as follows:

- The I/O test for UART, USART, SPI and I2C included signalling at the physical layer which were looped back so that both transmission and reception were tested.
- ADC values were read through from known analogue values into the software through the ADC hardware.
- The data encoding test included a test of known data input and output to and from the crypto hardware peripheral.
- The on chip RAM was tested using a scrub, read, write method.
- The internal Flash memory executed the code to perform all of these tests, a CRC of the Flash image was stored to an SD card and the Flash memory CRC was calculated once per test loop and compared to the value in the SD card.
- The Real Time Clock and other timers & counters were also checked by comparing the time on the target under test with the time on the test rig PC.
- ARM exception handlers were written to output the value of the exception registers should exceptions occur during code execution.

All of the above tests and exception handlers output data were sent across both a CAN bus and a UART to a test PC that collated the information.

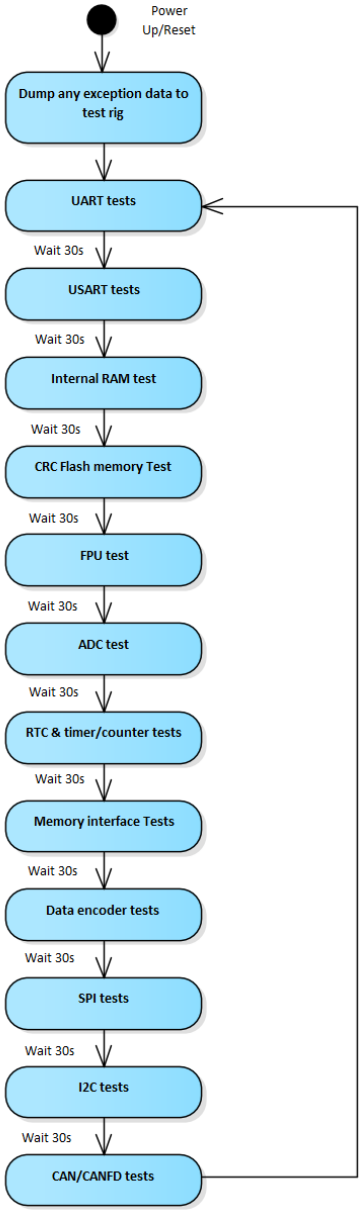

Figure 5: SAMV71 in test software loop

Test Rig Setup

The test rig setup is illustrated as shown below.

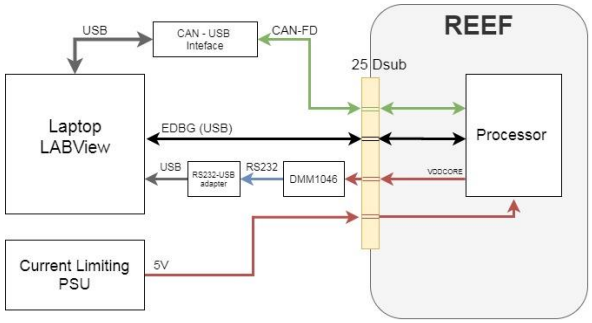

Figure 6: REEF Test rig setup

Test data was transmitted via two channels:

- A UART that the development board multiplexed into a USB channel using Atmels EDGB protocol.
- A Controller Area Network (CAN bus).

Two dissimilar communications channels were chosen in order to mitigate the possibility that the radiation dose affected one of these channels but not the rest of the chip under test. A test was also conducted of the CAN bus integrity (to ensure that the CAN controller was functioning correctly). This CAN test involved both transmission and reception of CAN data to and from the target.

Alongside the above tests, the current and voltage to the chip under test was monitored using a Digital Multi Meter (DMM).

All of the above data was captured to a comma separated text file alongside the current radiation dose using a LABView program that interfaced to the DMMs, the CAN bus and the UART (through EDGB). The LABView program also incorporated a Graphical User Interface (GUI) that gave real time feedback to an operator.

TEST ANALYSIS

A number of environment calculations were performed to plan the experimental work for test board irradiations in REEF. The expected total ionising dose (TID) over the course of a nominal mission, and the dose rate within the test facility at the University of Surrey were calculated.

Orbit Analysis

The Space Environment Information System (SPENVIS) was used for both the radiation environment specification (trapped protons, trapped electrons and solar protons) and the dose-depth calculations. The following inputs were used:

Standard radiation environment tools were used to calculate the total ionising dose for a 10 year mission in 800 km sun-synchronous orbit. The dose has a strong dependency on assumed spacecraft shielding, for example ranging from ~3 kRad[Si] to ~30 kRad[Si] for 4 mm and 1 mm Al-equivalent shielding respectively. In parallel the dose rate in REEF at a particular reference point for incident electron current (~1 kRad[Si] per hour) was calculated Therefore, based upon the specification of 2mm shielding, the expected dose will be ~9 kRad[Si].

The conclusion was that the total mission dose could be achieved in REEF in a timescale of hours to tens of hours of exposure. Significantly higher and lower dose rates are achievable; however, these are unlikely to be necessary unless it is desirable to expose devices under test to doses far in excess of the expected mission dose.

The team tested four targets (from different manufacturing batches) to 10 kRad. This was considered the pass criteria for a 10 year, 800 km sun synchronous mission. Should time allow and the target survives this dose, the plan was to expose one of these four parts to as high a dose as was achievable before observing failures through the test rig utility.

TEST CONCLUSIONS

From these initial tests the following conclusions were made:

SAMV71

The SAMV7 remains a candidate OSSAT processor, both from a performance and radiation tolerance perspective. Further work is needed to validate this further.

It is capable of writing to files at a speed which is fast enough for the needs of the OSSAT platform requirements (with cache enabled consuming approximately. 20% of the processor's processing run time under worst case burst write conditions).

It is also capable of withstanding significant TID without failure. Through analysis, a 10 year 800km sun synchronous orbit would equate to approx. 10 kRads of radiation dose. Under the destruction test, the chip only began to fail somewhere between 60 and 95 kRads. The current increase observed was also negligible.

STM32H7

The STM32H7 remains a candidate OSSAT processor, both from a performance and radiation tolerance

perspective. Further work is needed to validate this further.

It is capable of writing to files at a speed which is fast enough for the needs of the OSSAT platform requirements (with cache enabled consuming approximately. 40% of the processor's processing run time under worst case burst write conditions).

It is also capable of withstanding significant TID without failure. Through analysis, a 10 year 800km sun synchronous orbit would equate to approximately 10 kRads of radiation dose. Under the destruction test, the chip only began to fail at 47 kRads. The current increase observed was reasonably significant but not until the 47kRads failures were observed. An overall increase of 9mA (a 24% increase) was observed at 100 kRads. It should also be noted that annealing had a big impact on the processor's performance; this is another positive sign that the processor is capable of withstanding the radiation dose.

SAMA5D3

The SAMA5D3 remains a candidate OSSAT processor, both from a performance and radiation tolerance perspective. Follow on work is needed to validate this further.

However, we did find that developing "bare metal" software for this processor was not an easy task. The toolsets are setup around a Linux (Yokto) O/S including a U-Boot loader. The processor is also not as feature rich as the other two processors (the Atmel/Microchip SAMV71 and the ST Microelectronics STM32H753) that we evaluated. Despite the fact that this processor seemed very resilient with respect to TID radiation, the OSSAT team found the other two processors much easier to configure and use.

It is capable of writing to files at a speed which is fast enough for the needs of the OSSAT platform requirements (with cache disabled consuming approximately. 70% of the processor's processing run time under worst case burst write conditions).

It is also capable of withstanding significant TID without failure. Through analysis, a 10 year 800km sun synchronous orbit would equate to approximately 10 kRads of radiation dose. None of the samples tested failed in any detectable way, two of these were tested to 120 kRads.

NEXT STEPS

Further work is required in order to further evaluate and derisk the three processors as suitable options for the OSSAT platform. The OSSAT team are therefore planning the following:

SEU/Latch-up testing

The OSSAT team have a test plan drafted for a proton irradiation test campaign to test for tolerance against the Single Event Upset and Latch up effects.

Further performance testing

The design goal is to develop an AOCS system capable of running AOCS loops at up to 12Hz. This would be a major performance requirement on the STM32H7 processor. Therefore, a further task would be to develop representative AOCS software that would exercise the processor and assess its suitability to this task.

ACKNOWLEDGEMENTS

Many thanks to Research England and SPRINT for supporting this project, to the University of Surrey for their contribution and to the growing community of international collaborators who make up the OSSAT team.

REFERENCES

[1] "Open Source Satellite Programme," [Online].

[2] Anita Bernie, John Paffett, "Open Source Satellite Programme Manifesto," [Online]. Available: http://kispe.co.uk/files/KS-DOC-01076-01Manifesto.pdf.

Evaluation Criteria		SAMV71		STM32H7		SAMA5D3	
Criteria	**Target**	**Actual**	**Supplementary Circuitry required**	**Actual**	**Supplementary Circuitry required**	**Actual**	**Supplementary Circuitry required**
Performance	200 DMIPS	640 DMIPS [1]	N/A	1027 DMIPS[1]	N/A	825 DMIPS[1]	N/A
Power Consumption	300mW	250mW during radiation test	N/A	155mW during radiation test	N/A	336mW during radiation test NOTE: During the paper evaluation, power analysis showed this chip consuming 150mW but the actual (test) value was 336mW	N/A
Floating Point	FPU desirable	Double Precision FPU	N/A	Single & Double Precision FPU	N/A	Double Precision FPU	N/A
Program Memory	50MB	2MB (internal)	External program memory[2]	2MB (internal)	External program memory	160kB (internal) – cannot be reprogrammed from a factory delivered bootloader	External program memory
Data Memory	64MB	384kB (internal)	External data memory SD/MMC interface to memory and up to 256MB SDRAM and 64 MB Static memory.	1MB (internal)	External data memory The External Bus Interface can map up to 1GB of external memory (parallel memory e.g. SRAM). It can also support serial memories too.	128kB(internal)	External data memory Lots of options for external memory including ECC protection.
Mass Memory	64GB	None (other than the data memory already mentioned)	SPI/I2C busses can be used as a further memory interface. The capacity of these memories is increasing all the time, a single chip can now hold up to 8GB. [3]	None (other than the data memory already mentioned)	[3]	None (other than the data memory already mentioned)	[3]
Thermal	-40 to +100 degrees C	-40 to +105 degrees C	N/A	-40 to +85 degrees C	N/A	-40 to +105 degrees C	N/A

[1] This assumes the cache memory (which is ECC protected) is enabled.
[2] The processor can run code from external memory also. See https://www.avrfreaks.net/forum/compiling-program-ram-sam-v71-xplained-pro-card
[3] NOTE: SD/MMC memory can be used but this has very high memory densities that presents a risk (small transistor sizes are susceptible to SEU, and memory could be slow).

Figure 7: Summary of evaluation of processors against the qualitative criteria