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Development of a Power-Efficient, Low Cost, and Flash FPGA Based On-Board Computer for Small-Satellites

Anant Kandala[1], Ankit Verma[2], Sanidhya Vijaywat[3], Ansuman Palo[4]
Indian Institute of Space Science and Technology
Thiruvananthapuram, India; [1]+919711101451
[1]278anant@gmail.com
[1,4]Currently at Human Space Flight Center, Indian Space Research Organisation
[2]Currently at U R Rao Satellite Centre, Indian Space Research Organisation
[3]Currently at ISRO Telemetry, Tracking and Command Network

Amal Chandran
Laboratory for Atmospheric and Space Physics
Boulder, Colorado, USA; +1720-240-7727
Amal.Chandran@lasp.colorado.edu

Priyadarshnam Hari, Harsha Simha M S, R Sudharshan Kaarthik
Indian Institute of Space Science and Technology
Thiruvananthapuram, India; +917012972833
priyadarshan.hari@gmail.com

ABSTRACT

On-Board Computers (OBCs) for Small-satellite missions are typically required to be designed using industrial grade Commercial-of-the-shelf (COTS) components due to budget constraints and short mission duration. The OBC must provide a variety of interfaces due to the diverse nature of COTS subsystems having different interface definitions. Traditional OBC designs with standard microcontrollers have fixed interfaces that require modification of the motherboard circuit/layout when the external interfaces require changes. Thus, a possible solution is to have an FPGA in-addition to the micro-controller thereby providing a configurable interface capability. System-on-Chip (SoC) devices that integrate a microcontroller with FPGA fabric provide an ideal solution for reducing the development time. Additionally, the limited availability of power in small satellite missions makes it essential to use power-efficient devices. Furthermore, single event upsets (SEUs) and single event latch-up (SELs) are a major problem for OBCs designed for Low Earth Orbit (LEO) small-satellite missions. Flash memory-based FPGAs provide the benefit of low power consumption and they are more also fault-tolerant due to their intrinsic robustness against induced single event upsets compared to SRAM-based FPGAs. This article describes the OBC developed using the flash-based Microsemi SmartFusion2 SoC FPGA as its key component, for the INSPIRESat-1 and INSPIRESat-2 small-satellite missions. The OBC is designed in two form factors one with 13cm x 10cm dimensions for INSPIRESat-1 and the other with 10cm x 10cm dimensions for INSPIRESat-2. The OBC uses a COTS System-on-Module (SoM) developed by Emcraft containing the SmartFusion2 SoC, which is mounted on a custom-designed motherboard containing other peripherals including flash memory, SD Cards, and an external watchdog timer. The OBC has a total power consumption of approximately 1 W, in the final flight configuration. The article here describes the architecture of the OBC in detail, the key features of which include multiple on-board memories, a multi-level reset methodology, and reconfigurable input/output interfaces. The article concludes with the details of comprehensive performance tests conducted on the INSPIRESat-1 OBC, which has qualified TRL-8 (technology readiness level) status after completing required environmental tests such as the Thermal Vacuum Test (TVAC) and vibration test as a part of the integrated satellite. INSPIRESat-2 was launched in January 2021 and due to the successful working of the OBC in fight it has achieved TRL-9 status through this mission. The OBC developed for INSPIRESat-1 is planned to achieve TRL-9 status after its launch in the third quarter of 2021.

Introduction

This article describes the design and development of the OBC for the INSPIRESat-1 small satellite mission, which contains the Microsemi SmartFusion2 SoC FPGA as it's key component. INSPIRESat-1, like most other small satellite missions, is built using Industrial grade Commercial of the shelf (COTS) components. Hence, since COTS subsystems usually have different interface definitions, the OBC must have the capability to support a variety of interfaces. System on Chip (SoC) devices that integrate a microcontroller with FPGA fabric provide an efficient solution, as they have reconfigurable interfaces unlike traditional microcontroller based designs that have limited interfaces. The use of a FPGA based OBC is further advantageous for small satellites as it allows for incorporation of custom Verilog/VHDL IP (intellectual property) cores.

Another key constraint for small satellite mission is the limited availability of power. Using the power efficient SmartFusion2 SoC device is thus advantageous, and the board has a very low total average power consumption of approximately 0.9 W. The OBC designed contains a commercial System On Module (SOM) that uses the Microsemi SmartFusion SoC FPGA. The SoM is mounted on a flight card as shown in Fig. 1. The OBC was designed in 130cm x 100cm form factor according to the INSPIRESat-1 spacecraft avionics specifications. The various hardware features of this OBC are brought out in this article which have been designed specially for small-satellite applications.

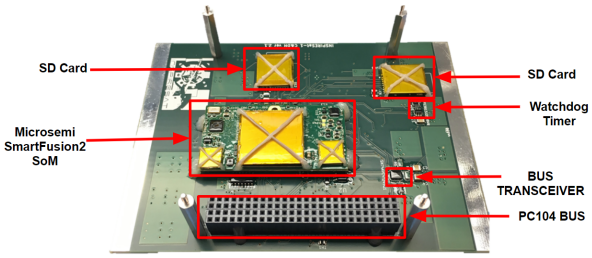

Figure 1: OBC Flight Model

OBC Hardware Architecture

The OBC contains a System on Module (SoM) based on the Microsemi SmartFusion2 SoC FPGA as it's main component. In addition to the SoM, the OBC also contains various other components including a external watchdog timer, SD Cards for data storage, Bus transceivers and RS422 transceivers as shown in the block diagram representation in Fig. 2. A detailed description of the functionalities of each of these components will be given in the subsequent subsections.

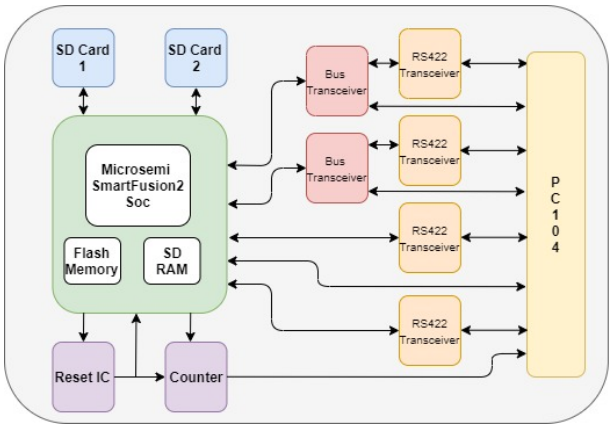

Figure 2: CDH Block Diagram

M2S FG484I System on Module (SoM)

The SmartFusion2 SoM, also referred to as the M2S-FG484I SOM, is a Commercial-of-the-shelf (COTS) compact (30 mm x 57 mm) mezzanine module developed by Emcraft Systems. The SoM includes the SmartFusion2 SoC FPGA from Microsemi Corporation in a FG484 package, on-module clocks and PLLs, a 64 MB LPDDR SDRAm (MT46H32M16) and a 16 MB SPI Flash (S25FL128SDPBHICO) on a single module (Fig. 3). The SoM is mounted on the OBC using a high density 80-pin (0.4 mm-pitch) connectors. These provide a total of 160 I/O pins which include 82 configurable GPIO interfaces in addition to the dedicated pins for UART (Universal Asynchronous Receiver-Transmitter), I^2C (Inter-Integrated Circuit) and SPI (Serial Peripheral Bus) interfaces. These user configurable interfaces provide flexibility in the design of the On-board computer, which is useful for small satellite missions which are characterized by fluid interface definitions. The SoM can be powered from a single 3.3V supply and contains internal regulators and power sequencers to power the FPGA and the other peripherals. Using a SoM with such integrated features is advantageous for small satellite mission, as it helps to reduce the cost and development time. For the OBC development, the M2S060-FG484I device was chosen, as it provides industrial grade temperature range (-40°C to 85°C), access to 60,000 (approx.) logic elements that provide enough resources to implement various custom FPGA IP cores typically required for small satellite missions.

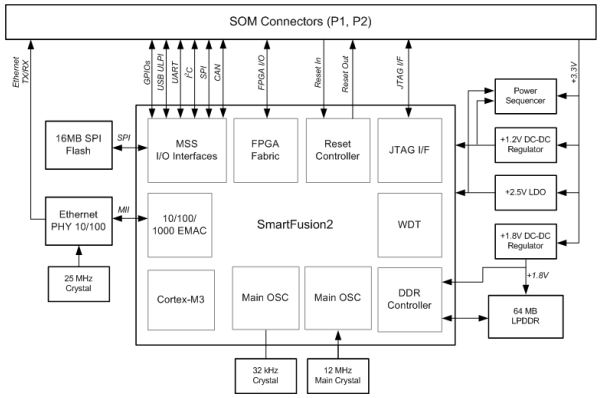

Figure 3: M2S FG484I Block Diagram, Source: EmCraft Systems[1]

Microsemi SmartFusion 2 System on Chip (SoC) FPGA

Microsemi SmartFusion2 SoC FPGAs contains a fourth-generation, flash-based FPGA fabric, an ARM Cortex-M3 processor, and high-performance communications interfaces integrated onto a single chip.[2] The reconfigurability offered by the FPGA is very useful feature for a Small-satellite OBC, as custom verilog IP cores such as Real Time Counters (RTCs), additional I/O interfaces etc., can be easily incorporated into the design. The 166-MHz 32-Bit ARM Cortex-M3 processor offers a 1.25 DMIPS/MHz Dhrystone benchmark, which shows that it is capable enough to run typical small-satellite onboard computations. The SoC also contains a 64 KB embedded SRAM (eSRAM), 512 KB embedded nonvolatile memory (eNVM), Two SPI ports, two I^2C ports, and multi-mode UARTs (MMUART) peripherals, a hardware-based watchdog timer and two general purpose 32 bit timers.

External On-Board Memory

The OBC contains two 128 Gb SD Cards, which are used to store science and housekeeping data before they can be downlinked. The two SD cards are connected to the SoM using separate SPI buses, that ensures that failure of one doesn't lead to the failure of the other. Using two also provides redundancy in case one of them fails. The power to the SD Cards are controlled by a Solid State Relays (G3VM41-HR). This is important as SD cards have a tendency of faulty behaviour, specially during the initialization procedure command sequence, which can only be corrected by a power reset. Thus, having the solid state relay switches provides the capability to reset the SD Cards in-case of a SD card failure.

Multilevel Reset Mechanism

One of the main highlight features of this OBC is it's multilevel reset mechanism. Having a robust reset mechanism is a crucial requirement for small satellite OBCs, as it helps recover from any undefined and unwanted anomalies in the flight software, as well as to solve any problems caused because of Single Event Upsets (SEUs). In order to develop a robust mechanism for small-satellite missions, resets were first classified into the following categories:

1. An **autonomous reset of the OBC's SoM** that is generated whenever the operating system is stuck in any software routine.
2. An **autonomous reset of the complete spacecraft** which would involve sending a signal to the Electrical Power System of the satellite in order to generate the reset.
3. A **ground-station command based reset** of the complete spacecraft, which would require having a special hardware and software routine that can be used to generate a spacecraft reset using a telecommand.

In order to implement all the three aforementioned reset methodologies a unique reset mechanism was designed as depicted in Fig. 4.

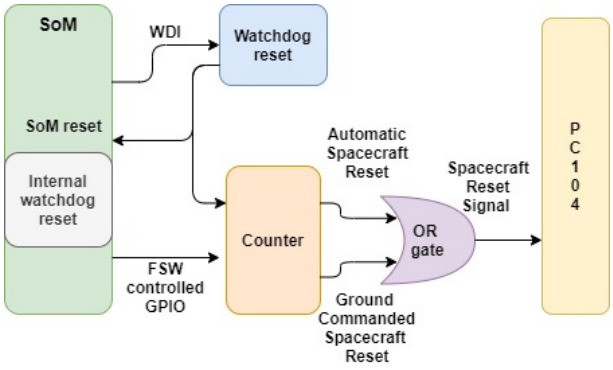

Figure 4: OBC Reset Mechanism

A processor supervisory IC (TPS3813J25DBVR) containing a watchdog timer is connected to the SoM module providing the first level of reset. The watchdog timer in this IC generates a reset of the SoM if it doesn't receive a toggle signal from the SoM within a programmable watchdog window. In case a reset of only the SoM fails to bring back the spacecraft in a recognisable state, the next step would be to generate a reset of the entire spacecraft.

In order implement this, a dual 4-bit counter(SN74HC393) has been added to the reset mechanism. The reset output of the processor supervisory IC is connected to the first clock input

of the dual 4-bit counter. The MSB output of the counter is used to signal the Electrical Power System (EPS) of the satellite to generate a spacecraft reset. Thus, after counting a total of eight internal resets, a complete spacecraft reset will be automatically generated.

Lastly, in order to provide a spacecraft reset from ground-station command, a dedicated GPIO line from the SoM is connected to the 4-bit counter IC. A software routine is written in the flight software that can be triggered from ground to toggle this GPIO eight times. The GPIO is not directly used to trigger the EPS, so as to prevent a false trigger that could happen as a result of a permanent latch up of this line. Both reset trigger signals to the EPS are passed through an OR gate, so that a spacecraft reset can be triggered autonomously or via a command from the ground-station.

Satellite Interfaces: Bus Transceivers and RS422 Transceivers

One of the main tasks of the On-board computer for small satellites is to interface with the different subsystems of the satellite. The OBC contains a standard cubesat PC104 bus to connect to the different subsystems. According to the interface requirements of the INSPIRESat-1 mission, four RS422 Converter ICs (MAX3488) have been added which, convert UART lines to RS422 logic levels. Further, the interface lines to different subsystems pass through bus transceivers (SN74AVC4T245-Q1). This IC provides a hardware control to tri-state any interface to external subsystems. The VCC isolation feature of this IC also ensures that if either VCC input is at GND, then both ports are in the high-impedance state. This helps to protect the the SoM from any kind of anomalous behavior of other subsystems.

Power Consumption Analysis and Testing

During design of the OBC, one of the main reasons for choosing the Microsemi SmartFusion2 (SF2) SoM, was its low power consumption. Analysis conducted using the SF2 power estimator, show that the M2S060 device consumes a maximum of 1097 mW (under 100% LUT, LSRAM, uSRAM and math block utilisation.) However, it was observed that for the FPGA configuration of INSPIRESat-1, much lesser percentage of the SoCs logic elements were utilized. Thus, during design it was estimated that the OBC would consume less than 1W of power even during peak operations. During the long duration environmental tests (which are described in more detail in the next section), the average power consumed by the OBC was 845.26 mW and the peak power consumed was 938.336 mW (Fig. 5(b)), thus satisfying the design criterion.

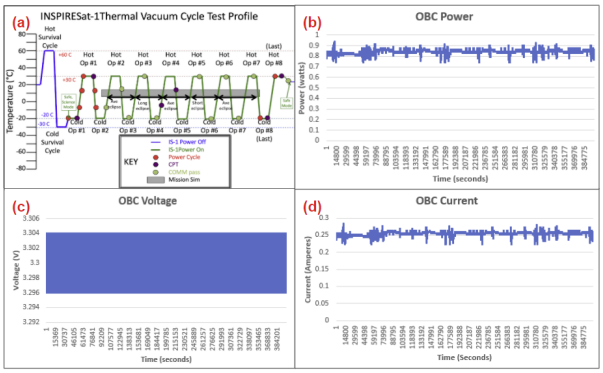

Figure 5: (a) TVAC Test Profile (b) OBC Power Consumption during TVAC test (c) OBC Supply Voltage (d)OBC Current Consumption

Environmental Testing

The environmental tests were carried on the flight model of On-Board Computer as a part of the integrated INSPIRESat-1 small satellite.[3] The tests performed on the satellite include vibration testing and thermal vacuum chamber testing. One of the points of concern was that the SoM mounted on the OBC using the high density connectors, might have problems surviving the vibration tests. In order to make the connection rigid, the SoM was secured on the OBC using a 3M Scotch-weld 2216 epoxy adhesive (Fig. 6(a)). To provide enhanced insulation and environmental protection of the OBC PCB, a Urethane conformal coating was also applied on the PCB. The spacecraft was then subject to vibration test at levels suggested by the launch vehicle on a vibration table (Fig. 6(b)). On completion of the vibration test, comprehensive performance tests were successfully carried out on the spacecraft to ensure proper functioning of the On Board Computer.

The spacecraft was also subject to thermal vacuum cycling test, to ensure proper functionality in the space temperature and vacuum conditions(Fig. 6(c)). The OBC was turned on during the thermal cycling, which also acted as a long duration test of the OBC in space like conditions. Various telemetry values, including OBC voltage, current, and temperature were logged from the OBC throughout the thermal cycles which verified proper functioning of the on-board computer.

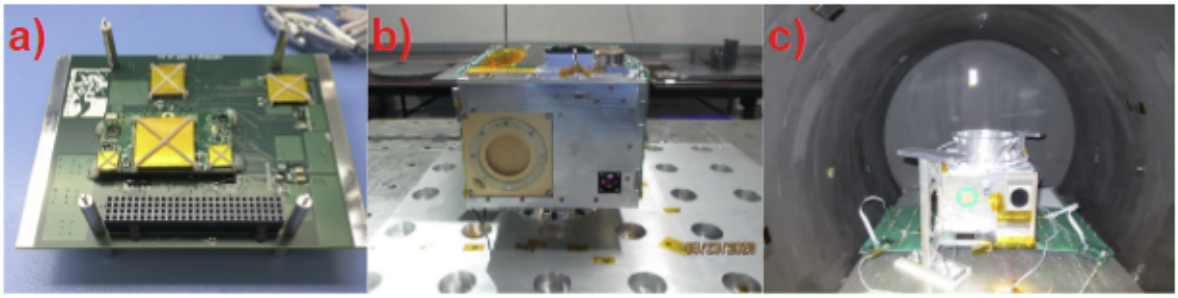

Figure 6: (a) Flight Model of OBC with Epoxy applied (b) IS-1 Spacecraft during vibration tests (c) IS-1 Spacecraft during TVAC tests

Radiation Tolerance

Since the Microsemi SmartFusion2 SoC FPGAs and IGLOO2 FPGAs are 65nm, non-volatile, **flash-based FPGAs**, they exhibit intrinsic robustness against radiation induced single event upsets. This is in direct contrast to SRAM-based which exhibit single event upsets in the SRAM configuration memory that configures the function of logic cells and connects routing tracks together. This can lead to unpredictable behaviour that can be very harmful for the small satellite system. In order to demonstrate absence in configuration upsets due to radiation, Microsemi has conducted radiation testing on the M2S050 SmartFusion2 FPGAs. Forty-eight units of Microsemi M2S050 SmartFusion2 FPGAs were exposed to heavy ions at LET levels up to 90.3 $MeV - cm^2/mg$ and no configuration upsets were detected during testing on a total of 48 parts in a total influence of 2.83 x 10^9 heavy ions.[4]

Conclusion

The article describes the design and development of a flash-FPGA based OBC for small satellites. A smaller form factor (10 cm x 10 cm)[5] of this OBC, achieved TRL-9 status after the successful launch of the INSPIRESat-2 IDEASSat mission.[6] The OBC functioned properly and no anomalies in the OBC were detected during flight. The OBC designed for INSPIRESat-1 has successfully completed all environmental tests and comprehensive performance tests, and is planned to be launched in Q3 of 2021.

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