



INTRODUCTION

Over the last 10 years the number satellites launched into space have risen exponentially, reaching a record 2588 registered satellites in 2023¹. A large portion of these are mega-constellations that inherently have very short development cycles, driving the sub-system manufacturing lead times down to several months.

At VEOWARE, the aim is to offer a lead time of 3 months for the CMG products. This desire triggered several developments for the production chain optimization, especially when it comes to automatization infrastructure, including:

- Automated flywheel balancing
- Automated motor control calibration
- Automated avionics functional test

This poster summarizes the development methodology, architecture choices and avionic Design for Test (DfT) considerations that took place when developing VEOWARE's automated avionics' test system. It also shows the manufactured system and describes this test system's validation results.

DfT of Future Developments

As an outcome of this project, a list of best practices was conceived for Design for Test of future avionics, including:

- DfT requirement incorporation at an early design stage
- DfT check for each function and circuit block
- Verify if the existing test infrastructure allows performance validation (if not, trade-off analysis)
- Prioritize re-use of existing (automated test friendly) circuits

MODULARITY & SCALABILITY

Modularity considerations when developing the test system:

- Modular DUT interface for a versatile Test Platform
- Over 10 generic interfaces added for future features, addons (current/voltage ADC, GPIO, load interfaces)
- Multiple test platforms can be connected to run in parallel

Easy servicing:

- COTS based
- LEDs indicating hardware status
- Easily replaceable parts:
 - Relays
 - Connector Savers
 - Interface PCB

ACRONYMS

ADC: Analog-to-Digital Converter COTS: Commercial Off-The-Shelf CMG: Control Moment Gyroscope DfT: Design for Test GPIO: General Purpose Input/Output

DUT: Device Under Test MCU: Microcontroller Unit PSU: Power Supply Unit PCB: Printed Circuit Board **RPI: Raspberry Pi**

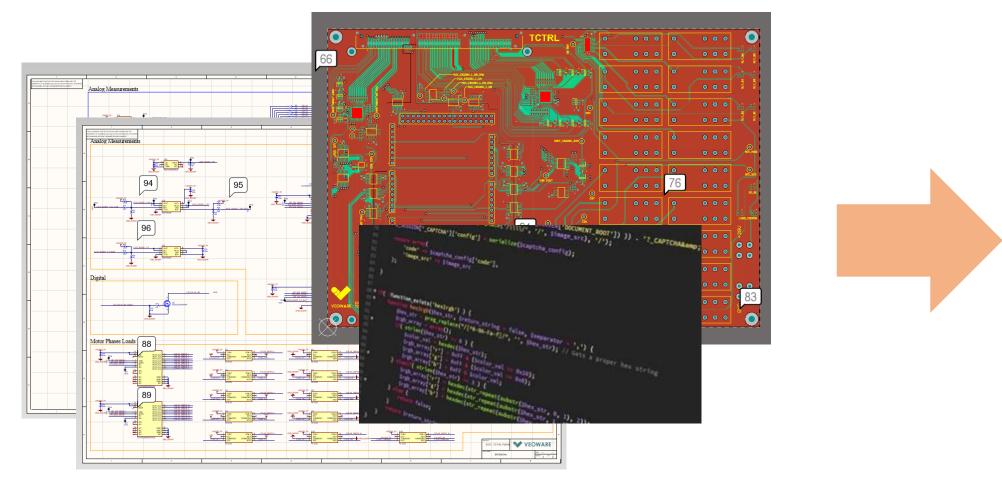
Automated Test Conception for Next Generation CMG Avionics Slashing Lead Time and Improving Reliability for the Next Generation CMGs

DEVELOPMENT

The automated test development was two-pronged: on one side the test system was developed through VEOWARE standard system engineering practices, on the other side, the avionics had to be adapted to expose the necessary interfaces. Avionics verification was-also re-assessed with a new set of pass/fail criteria. A trade-off analysis was performed between an in-house custom development (custom microcontroller-based ADC system) and industrial automation approach (Labview or similar). The in-house development was selected due to price, flexibility and scalability reasons.

Objective Definition	Operator Time < 0.5h	Scalable – up to 10 DUT	Easy to us
System Requirement Definition	Interface Board	Measurement chain	Equipmer (PSU, harness
Architecture Definition	Modular	Future (design) proof	Cost- effective
System Design	Hardware selection	Custom Board Design	DUT "Test Applicatio
System Manufacturing	PCB Production	Hardware Procurement	PCB Checkou Debug
System Validation, Delivery	Measurement Chain Calibration	Test suite development	Stress Testin / Bug Findin
DUT re-DfT	Verification Requirements	Additional Test Interfaces	Pass/fail Criteria Definition

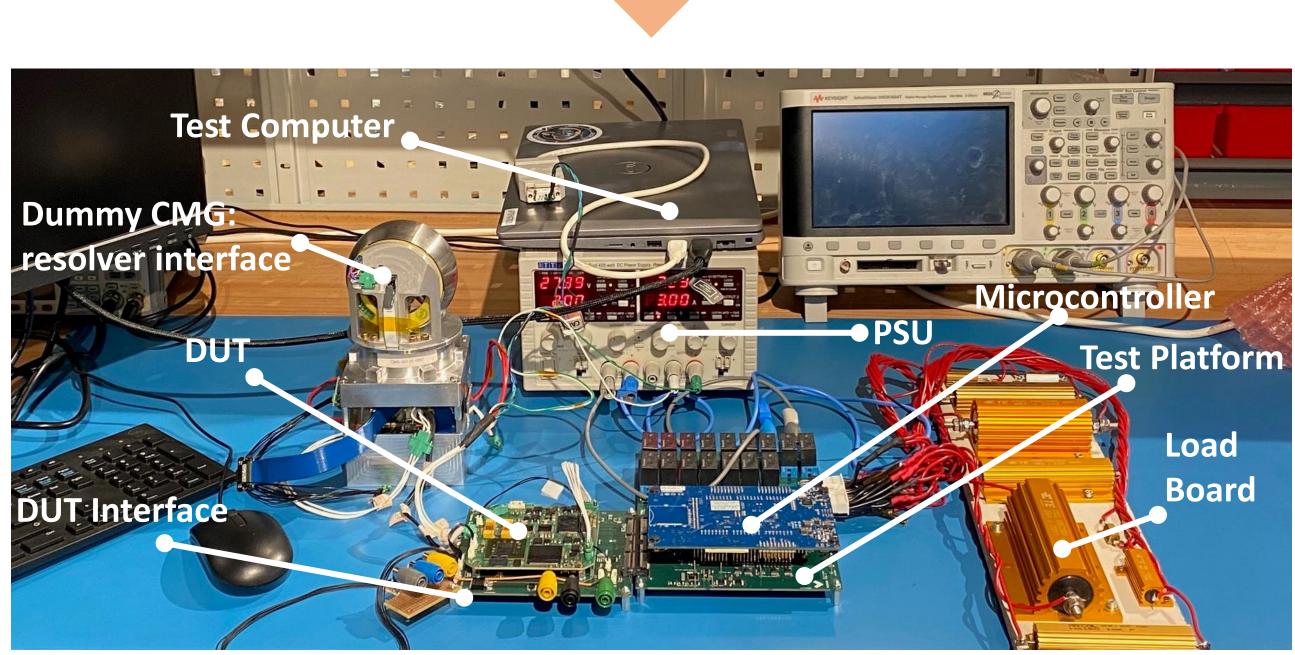
Modular Automated Requirement Testing Assembly (MARTA)

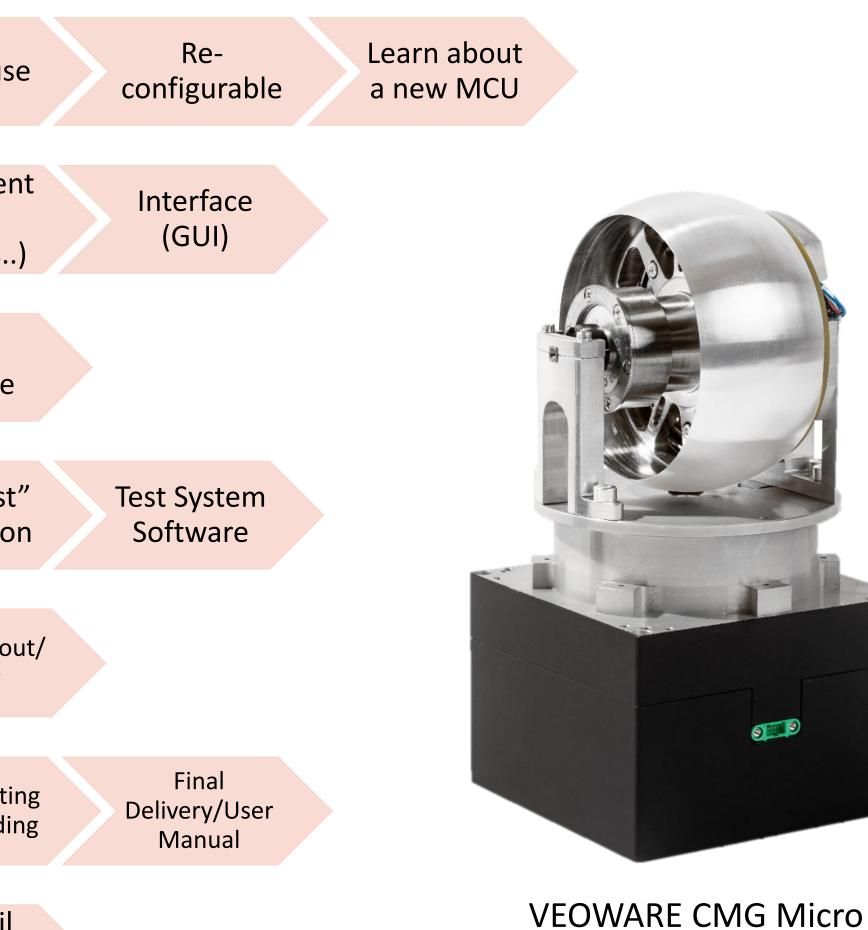


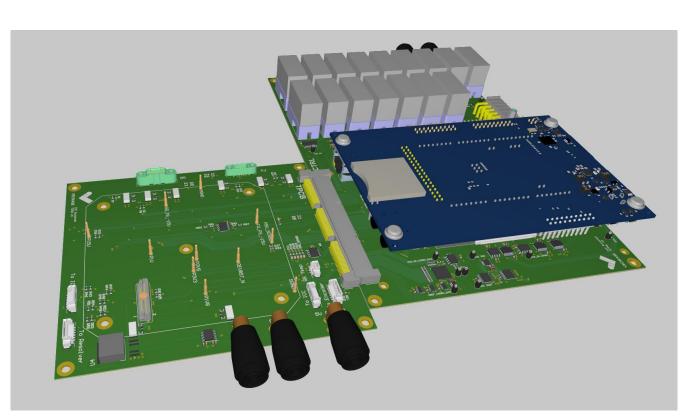
Results

- All interfaces checked operational + calibrated.
- Test suites still in development, preliminary results show test time < 10 min per DUT (compared to 2 FTE days).
- Measurement system accuracy:
 - < 100 mV for 0-40V range,
 - < 15mV for 0-10V range,
 - < 50mA for -12-12A range,
 - < 5mA for 1A range.

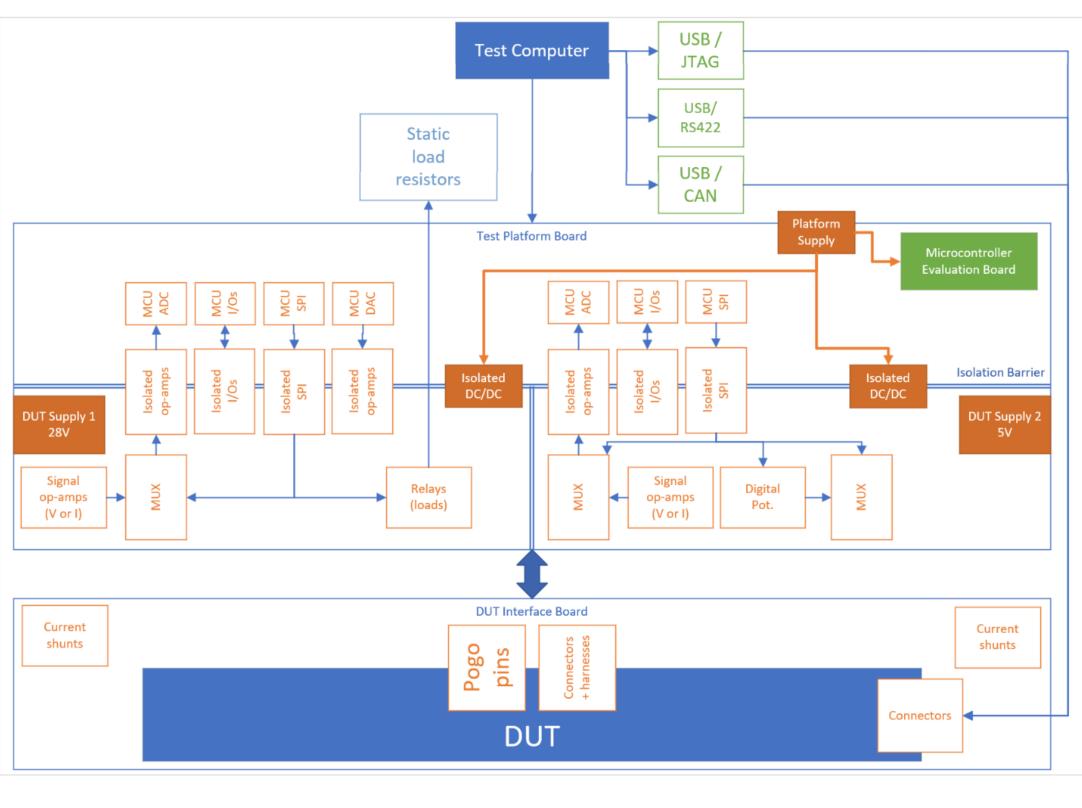
 Challenges: Limited sampling rate (50ksps) for simultaneous dual channel acquisition (due to architectural choices).

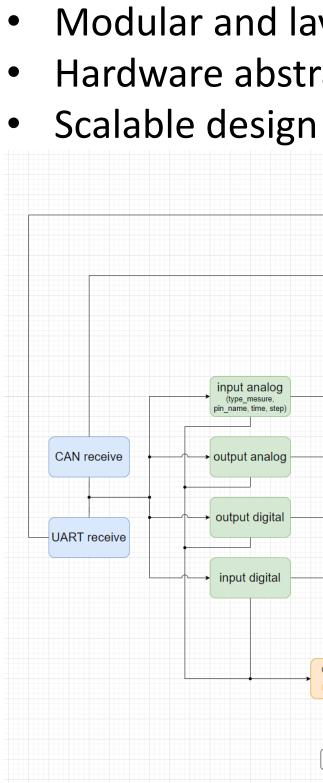






- Microcontroller based test platform • Operator Interface: computer (laptop or RPI) • Galvanically isolated measurement system • Common Test Platform + replaceable DUT interface board





The system engineering approach focused on modularity and scalability also facilitates a very structured design and validation phase for the tester system. Despite a high number of interfaces and interconnected equipment, the debugging phase was only a couple of weeks. Future steps include extending the test system to other VEOWARE avionics systems, standardizing the 3rd party equipment and miniaturizing for better transport/setup (at manufacturer facilities).

First Version of MARTA





Edgars Pavlovskis, Xavier Gillard VEOWARE. E2Smart <u>edgars.pavlovskis@veowarespace.com, xavier.gillard@e2smart.com</u>

Electrical Architecture

Software Architecture

Modular and layered Hardware abstraction

HAL CAN HAL Timer HAL ADC HAL DAC HAL peripheral HAL SPI External peripheral Internal peripheral HAL 12C

CONCLUSION & FUTURE STEPS

REFERENCES

1. UNOOSA Annual Report 2023

