EEETester: Development of CubeSat platform for space heritage of Korean manufactured Electrical, Electronics, and Electromechanical part

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Introduction

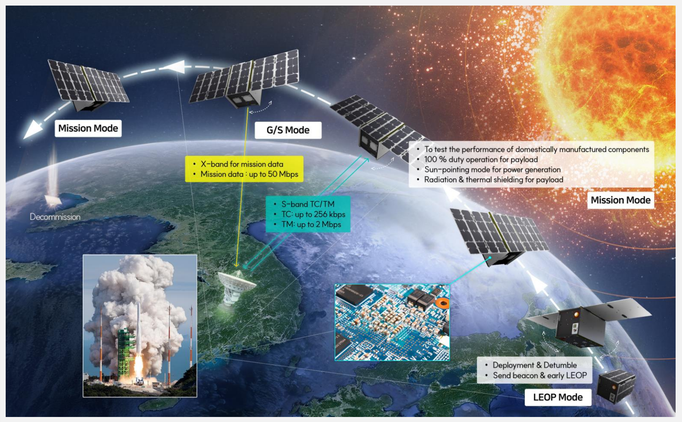
❖ Electrical, Electronics, and Electromechanical part Tester (EEETester)

◆Development of CubeSat platform to get the space heritage of Korean manufactured electrical and electronic equipment

- ➢ To get the space heritage of Korean manufactured EEE part (TRL 6)
- ➢ To expend the ecosystem of space industry using of semi conductor based EEE part for improving reliability
- ➢ To get the space core technology to use KSLV-II

❖Concept of Operations

◆ I. LEOP (Launch & Early Orbit Phase) : Detumbling & early operation
◆ II. Mission mode : 100 % duty operation of the payload at sun pointing
◆ III. G/S mode : Send the payload data from the payload & SOH



<Concept of Operations for the EEETester>

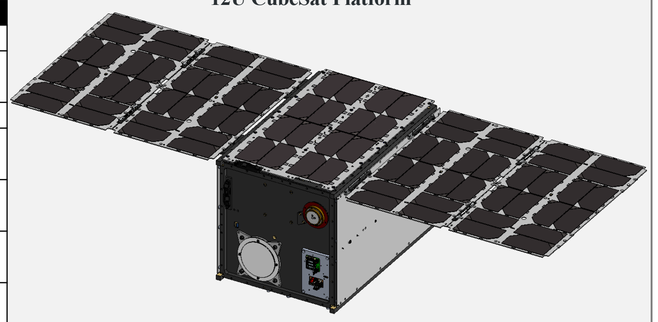
Parameter		EEETester #1	EEETester #2	EEETester #3
Orbit	Altitude	600 km	500 km	500 km
	Inc.	97.79°	97.41°	97.41°
	LTAN/ LTDN	12:30	10:30	13:30
Mission life		12 Months	12 Months	12 Months
Launcher		KSLV-II	KSLV-II	KSLV-II
Launch date		2025 4Q	2026 4Q	2027 4Q
Payloads		Samsung Memory	TBD	TBD
		Korean manufactured electronic components		
		AD/DA ASIC		

< EEETester program>

EEETester Specification

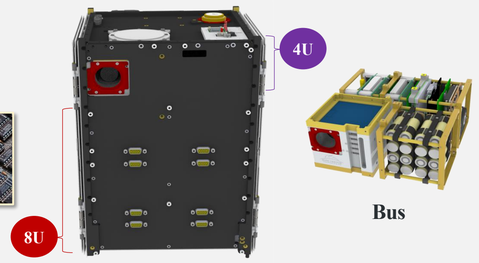
Parameter			Specification
Payload	Mass		Up to 14 kg
	Size		Up to 8U (200 mm x 200 mm x 200 mm)
	Power		20 W (100 % duty)
	Power channel		3.3V(4ch), 5V(3ch), 12V(3ch), VBAT(1ch)
	Protocol I/F		CAN(1ch), I2C(1ch), RS422(4ch), SpW(1ch), RS232(1ch), SPI(2ch)
Bus	Attitude Control	Mode	Detumble, Sun pointing, and G/S tracking
		Pointing Accuracy	0.05 deg.
		Off nadir	20 deg.
	Power	Power Generation	97.29 W
		Power Consumption	35.39 W (Inc. Payload 20 W)
		Battery	186 Wh
		DoD	Up to 30 %
	Comm.	S-band Uplink	Up to 256 kbps
		S-band Downlink	Up to 2 Mbps
		X-band Downlink	Up to 50 Mbps

12U CubeSat Platform



< Deployment configuration>

EEE Payload



Bus

< Stowed configuration>

Acknowledgment

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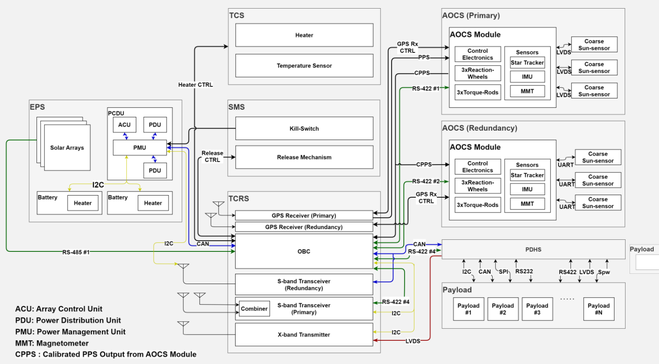
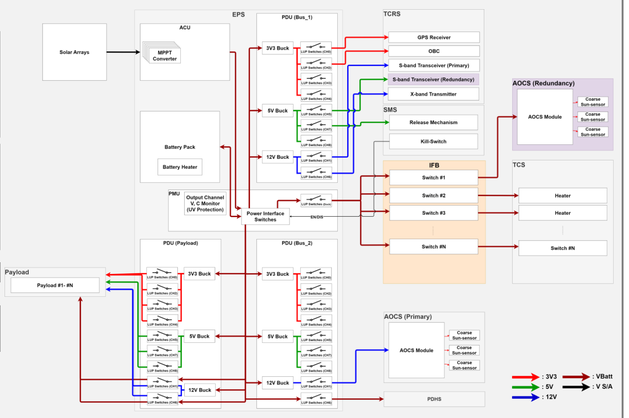
System Design

❖ System Diagram

◆PDHS interfaces various interface protocol for multi payloads
◆TCRS and AOCS has redundancy architecture for reliability of the system
◆Bus platform controls the power switch of each payload for efficient system design

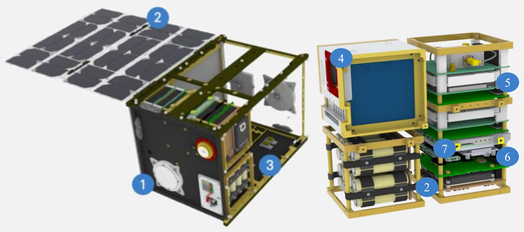


<EEETester interface diagram>

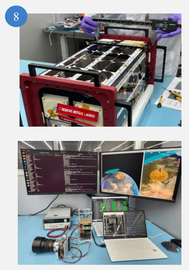


<EEETester power diagram>

❖EEETester subsystem configuration



▪< EEETester bus platform>

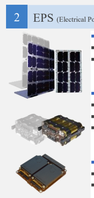


<EGSE configuration>

1 SMS (Structure Mechanism Subsystem)

- **12U CubeSat structure**
  - Aluminum alloy-based skeleton considering structural robustness
  - Surface treatment for ground/heat transfer characteristics
  - Kill-switch mechanism for pre-launch
- **External panels**
  - Attachment of panels for securing external components, thermal/space radiation shielding

2 EPS (Electrical Power Subsystem)



- **Solar Panels**
  - 30 % high-efficiency cells
  - Use double deployment solar panels For maximum power generation
- **Battery**
  - 8S2P configuration
  - 172 Wh capacity
  - Storage of generated power and supply
- **EPS**
  - Supply the power to Bus & Payload
  - Overcurrent & overvoltage protection

3 TCS (Thermal Control Subsystem)

- Thermal control of the heaters for the components susceptible to lower temperature
- Thermal isolation and passive control with MLI

4 AOCS (Attitude & Orbit Control Subsystem)

- **Star Tracker & Gyro,**
  - Attitude determination: < 6/40 arcsec (cross-/along-boresight)
  - Integrated algorithm implementation
- **RW & MTQ**
  - Modular design considering space utilization and structural robustness
  - Part selection based on mission design
- **Sun Sensors & Mag.**
  - Use wide-angle sun sensors
  - Use magnetometer with sun sensors

5 TCRS (Telemetry, Command & Ranging Subsystem)

- **OBC**
  - In-house subsystem with TRL9
  - Use the in-house FSW to control the all of subsystem
  - Main I/F : CAN bus & RS-422/485
- **Interface board & harness**
  - Expand interface between subsystem
  - In-house harness with IPC
- **GNSS receiver & antenna**
  - Consider GPS signal coverage
- **S-band Transceiver & antenna**
  - Stable TM/TC configuration
  - Use Omni direction antennae
  - Redundant configuration
- **X-band transmitter & antenna**
  - High-speed mission data download

6 FSW (Flight Software)

- In-house FSW
- Operation mode control
- All subsystem status monitoring
- Operation TC/TM & Mission data
- Implement the FDIR

7 PDHS (Payload Data Handling Subsystem)

- Control the multiple payloads
- Radiation protection circuit
- Data processing & storage for payload data
- CCSDS modulation with CADU

8 GSE (Ground Support Equipment)

- **MGSE**
  - 12U standard CubeSat test POD
  - Jig for the assembly between payload & bus platform
  - Stability MGSE for transportation
  - Protection during storage
- **EGSE**
  - Simulate bus subsystem signal & interface with bus platform
  - Dynamic simulation of attitude control and sensors
  - Simulate of solar panel power generation
  - Simulate of Ground station with RF signal
  - Simulate orbit operation scenario during burn-in test

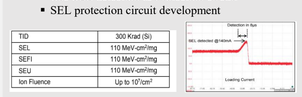
❖Payload Data Handling System (PDHS) development

Design & Analysis

Radiation hardness

- Design the SEE hardness
  - Use SEL detection & Protection circuit
  - SEL protection circuit development

TID	300 Krad (Si)
SEL	110 MeV-cm²/mg
SEFI	110 MeV-cm²/mg
SEU	110 MeV-cm²/mg
Ion Fluence	Up to 10^7/cm²



<SEL protection IC spec.> <SEL protection current graph>

<Latch-up block diagram> <IC block diagram>

Various Interface for Payload

- Use FPGA to Implement for various payload interface for different payload of EEETester #2 & EEETester #3

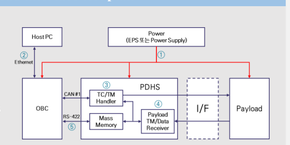
I/F	QTY	Spec.
I2C	2 EA	400k(High Speed Mode)
CAN	2 EA	1M
SPI	2 EA	1M(Standard), CS 2bit
RS232	2 EA	115,200bps
RS422	5 EA	10Mbps
LVDS	1 EA	200Mbit/s, 4bit data
Spacewire	1 EA	200Mbit/s

Technical development approach

- To increase reliability to select the COTS components and screening
- Systemically radiation hardness design & ECC in memories
- Various interface for muti-interface for different payload users
- Timing analysis and design for data CMD/TM in space environment

Payload interface test plan

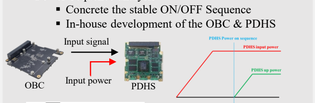
1. Turn on OBC, PDHS, Payload
2. OBC control by Ethernet
3. OBC-Payload CMD/TM
4. Receiving payload TM
5. Transfer payload data to PDHS



Development & Test

Power ON/OFF Sequence

- Power Sequence analysis
  - Concrete the stable ON/OFF Sequence
  - In-house development of the OBC & PDHS

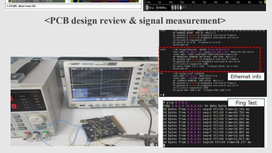


<Core input power>

<Power sequence example> <Power sequence analysis for PDHS>

Hardware verification

<PCB design review & signal measurement>



<Functional test of system and memories>

Hardware verification

Parameter	Spec.
FPGA	Xilinx SoC (COTS heritage)
Memory	DDR3L DRAM (8 Gbit)
Storage	SLC NAND Flash (512 Gbit)
Power Consumption	5 W (Average), 11 W (Max)
Mass	200 g (TBD)
Size	90 x 96 x 12 mm (/w case)
Modulation	CCSDS CADU format

<PDHS>