SSC24-S2-10

Design and Testing of a Resilient COTS Point of Load Converter for Deep Space CubeSats

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ABSTRACT

To support the development of the upcoming Binar Space Program 12U *Explorer Class* platform, currently being designed for lunar and interplanetary research applications, the design and testing of a modular Gallium Nitride (GaN) based Point of Load (PoL) converter is being undertaken. The converter has been designed to supply power to high-transient-current loads, such as communications systems, by regulating down a higher voltage derived from a range of common CubeSat battery configurations to a target voltage of 5V. The system consists of parallel-connected linear regulator and buck converter stages which deliver power to the load through a high-side current sense circuit. The current sense resistor has a fault tolerant current-to-voltage conversion stage followed by a hysteretic comparison trigger stage, feeding a majority-voter subsystem. The output from the majority voter is used as feedback to automatically enable the normally isolated buck converter when a high load current condition is detected at the output. The majority voter, power switches, linear regulator and Buck converter have been implemented using Gallium Nitride High Electron Mobility Transistors (GaN HEMT). Gallium nitride has been selected to take advantage of the high power density and ionizing radiation tolerance intrinsic to the technology.

INTRODUCTION

Small spacecraft are increasingly being asked to perform more complicated missions and operate in more difficult environments; this necessitates additional power generation within the compact satellite form factor. CubeSat scale propulsion systems, high performance computing, and other high-power-draw subsystems also necessitate more capable spacecraft power converters. With increased power consumption in a compact form factor comes an increase in the challenges associated with the design of a space- and mass-constrained satellite power systems. Examples of products that offer a similar output power as the proposed converter have sizes ranging from approximately 800 square millimeters[1] to entire 1-unit subsystems[2]. Integrating hardware rated for the difficult radiation conditions encountered in deep space into a CubeSat scale platform is complicated by the limited volume and mass budgets inherent to their design standards, and the often limited budgets of engineering teams designing the flight platform.

NASA has indicated a modular approach to power system design as being key to future exploration missions[3]. Modular, distributed approaches consume additional volume within the spacecraft, making the implementation of N+1 redundancy or other hardware-level fault recovery schemes more penalizing towards the limited spacecraft volume budget as individual module size increases to support higher power.

GaN HEMT have benefits that assist in addressing the volume, efficiency and fault tolerance challenges identified previously. When used in the design of voltage converters, they feature higher power density over traditional silicon, higher switching frequency which enables smaller passive components and lower losses, and intrinsic space environment robustness.

To provide a high conversion efficiency in all load situations, the converter utilizes a topology comprised of a parallel connected linear regulator and switching converter. This topology ensures that the highest efficiency converter is selected depending on the load conditions. The selection of which converter supplies the load is performed automatically, using a feedback signal from triple-redundant load current sensors. To further increase the fault resilience of the converter, the redundant current sensor outputs are combined using a two-of-three majority voter circuit. This circuit has been implemented without silicon-based technology, using only discrete gallium nitride transistors, to take advantage of the radiation dose tolerance that the technology provides.

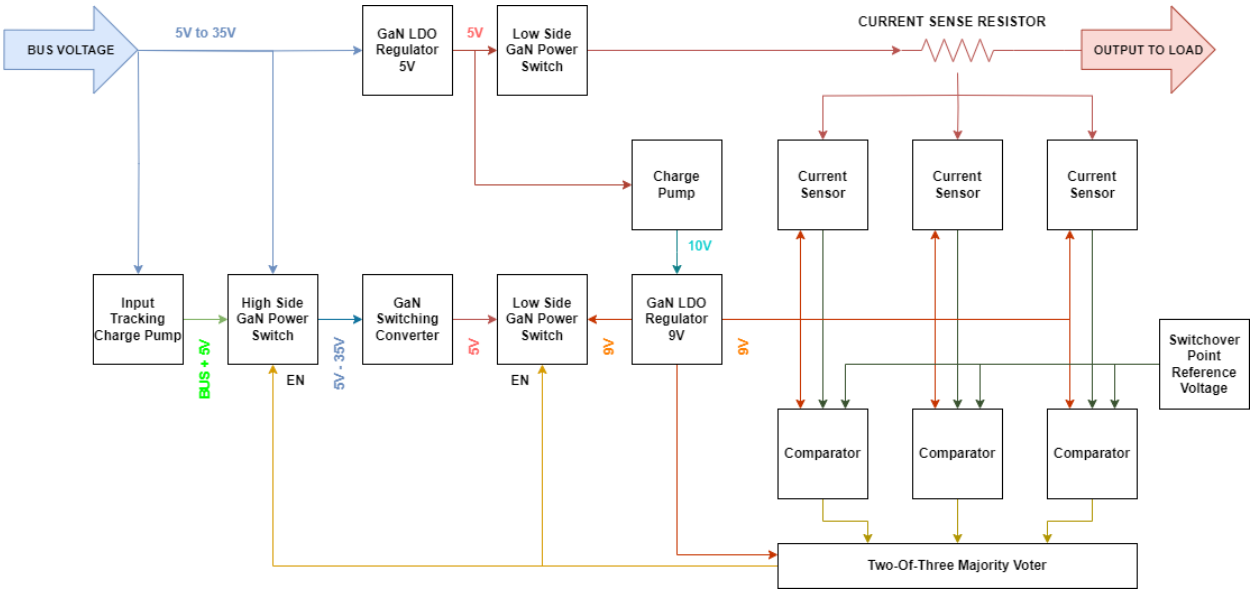

Figure 1: System Block Diagram of the Proposed Converter

The combination of GaN Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) and a high efficiency topology seek to address the challenges associated with current power system designs destined for deep space, or other environments where difficulties are encountered with high radiation conditions.

SYSTEM CONCEPT

The system targets high transient current loads in CubeSats destined for deep space. It has been designed in such a way as to support a modular implementation within the spacecraft architecture. These two high-level design requirements have acted as the driving force behind the selection of topology and modules included in the final system. The topology that has been developed consists of a parallel DC-DC converter system with logic to automatically switch between the highest-efficiency converter at any one time. An outline of the subsystems and connection topology of the proposed point of load converter is shown in Figure 1.

The switch between converters is determined automatically using an analog feedback system. When the load current measured by the converter increases above a set trigger level, the converter disables a pair of high- and low-side isolation power switches, connecting the buck converter subsystem to the input and output power rails. The converter will then assist in supplying power to the load for the duration of the high current transient event. Once the transient event has ceased, indicated by the load current dropping below a set trigger point, plus hysteresis margin, the pair of isolation load switches are re-enabled.

The combined converter topology has been selected to overcome efficiency issues inherent in the functionality of each converter. As power loss in a linear regulator is a function of the voltage differential across the regulator and load current, linear regulators are unsuitable for large differential voltages or large load currents. Buck switching converters overcome this limitation using magnetic passive components to store an intermediate charge level, alongside switched elements to connect and disconnect the magnetic storage components from the input power intermittently. The efficiency of a buck converter is thus much higher than a linear regulator when outputting a high current load, as the losses in the converter are dominated by parasitic losses within the switched elements themselves. The drawback to a buck switching converter is that under light load conditions the efficiency of the converter rapidly drops. This is because the parasitic loads of the switching elements remain constant as the load reduces, eventually constituting much of the converter power loss.

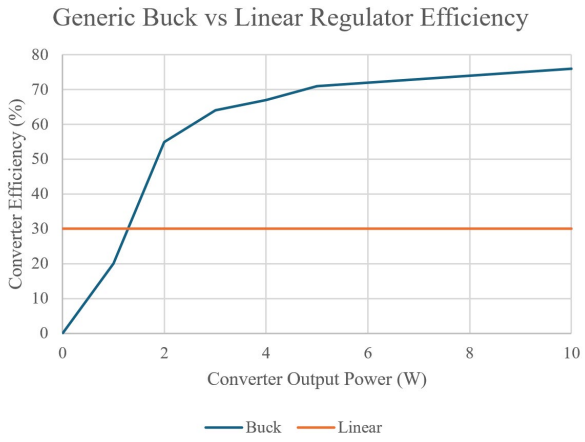

Figure 2: Generic Converter Efficiency Comparison

The parallel switching/linear converter and power multiplexing topology act to ensure that the point of load module is always selecting the highest efficiency power converter. An example of generic efficiency curves for the two converter topologies are indicated in Figure 2, indicating how the efficiency of the linear converter is higher than the switching converter for very light loads. The circuit samples the load current, and determined from a controllable switch point it automatically enables the buck converter when load currents increase above the optimal efficiency switchover point. By implementing switching logic, the converter can save power that would otherwise be wasted through idle converter losses, while still providing efficient high-power conversion when large power draw states occur.

The module utilizes gallium nitride technology, incorporating into the module design the beneficial power-to-volume ratio inherent in the technology. Gallium nitride MOSFETs, due to their inherently low on-state resistance, can switch very high current loads within small package components. A silicon MOSFET that matches the specifications of the selected GaN MOSFET used in the modules making up the point of load converter has an almost 100% increase in volume, leading to bulkier module designs[4, 5]. Another beneficial feature of GaN MOSFETs is their significantly lower inter-gate capacitance when compared to traditional silicon MOSFETs. This allows GaN devices to switch faster, which enables smaller passive components, lowering the already reduced volume required for the designs. The final feature of GaN being utilized for the design is the higher semiconductor bandgap voltage. The increased bandgap voltage ensures reliable operation over extended temperature ranges and under higher doses of ionizing radiation.

The higher bandgap voltage, however, adds to the complexity of driving these components into active saturation. For the GaN MOSFET used in the converter, it requires a gate-source bias voltage of approximately 3.5 to 5V higher than the drain-source voltage. Supplying the GaN MOSFET with a V_{GATE} voltage that equals the V_{DRAIN} voltage causes the MOSFET to enter partial turn-on mode, where the device has a high drain-source resistance and prevents full conduction. GaN MOSFETs are also only available in n-channel configurations, and within this they are also only commonly available as enhancement mode transistors. This limitation adds additional constraints to the circuits that can be designed with the MOSFETs, as the designer must always produce a controlled, higher gate voltage to fully switch the component into a saturated on-state.

The system has been designed for CubeSats, which commonly use 18650-series lithium batteries in their power storage system construction[6]. Therefore, the converter has been designed to operate from a two to eight cell series connected battery pack. A pack of this configuration has a V_{MAX} from 8.4 to 33.6V, a V_{MIN} from 5.2 to 20.8V, meaning the converter should have a total operational input ranging from 5.2V to 33.6V. The converter has been designed to output a constant 5V from this range of input voltages. The converter can output currents up to 5A, meaning each point of load module can operate up to 25W loads, and can be connected in parallel if higher power is required.

SUBSYSTEM DESIGN, SIMULATION AND TESTING

Input Tracking Charge Pump

Utilizing n-channel GaN MOSFETs necessitates the generation of a higher voltage level that can be applied to the gate to ensure complete turn-on of the FET. As indicated in Figure 3, this voltage is generated using a summing rail to rail operational amplifier that combines the subsystem input voltage with a fixed 4.7V reference voltage. The operational amplifier is powered above the input voltage using a charge pump, the output of which is routed into a current-buffered unity gain operational amplifier. To support the wide input range of the converter, both operational amplifiers need the capacity to operate up to 38.6V.

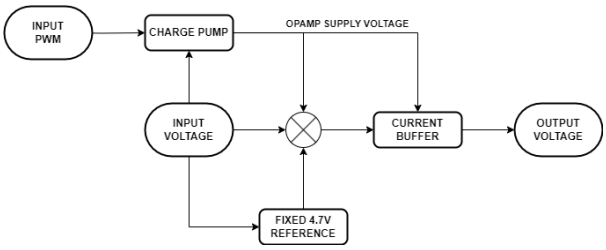

Figure 3: Gate Bias Circuit Block Diagram

The tracking charge pump circuit has been simulated using LTSpice and, as indicated in Figure 4, it was found to correctly output the input voltage plus margin for the converters designated input voltage range.

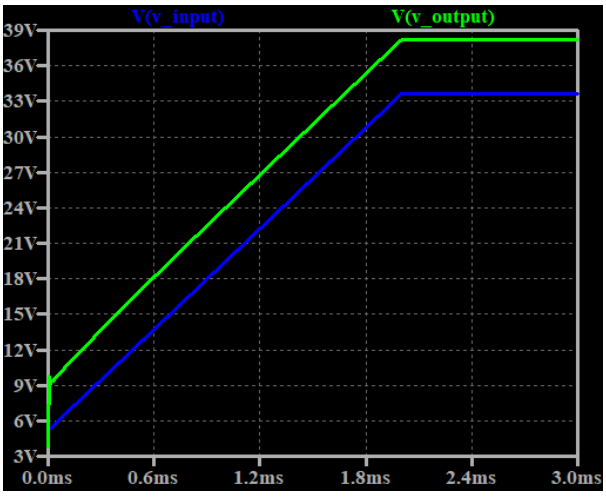

Figure 4: Charge Pump Voltage Simulation

Linear Regulator

The linear regulator uses a standard feedback-controlled topology. The feedback control has been implemented using an output voltage sense divider and operational amplifier to compare the output voltage to a selected voltage setpoint. The error signal generated is used to modulate the gate of an n-channel gallium nitride MOSFET pass element. The complete regulator subsystem block diagram is indicated in Figure 5.

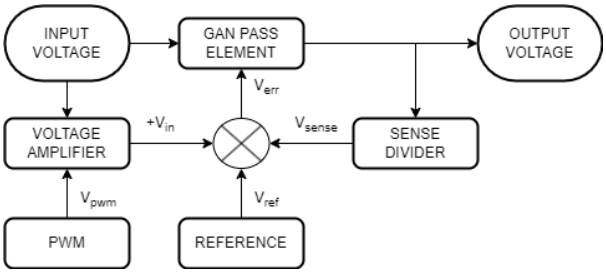

Figure 5: GaN Linear Regulator Block Diagram

The GaN linear regulator was functionally verified using a simulation of the circuit assembled in LTSpice. The GaN MOSFET simulation files used with LTSpice were obtained from the manufacturer[7]. Results of a voltage sweep simulation are indicated in Figure 6.

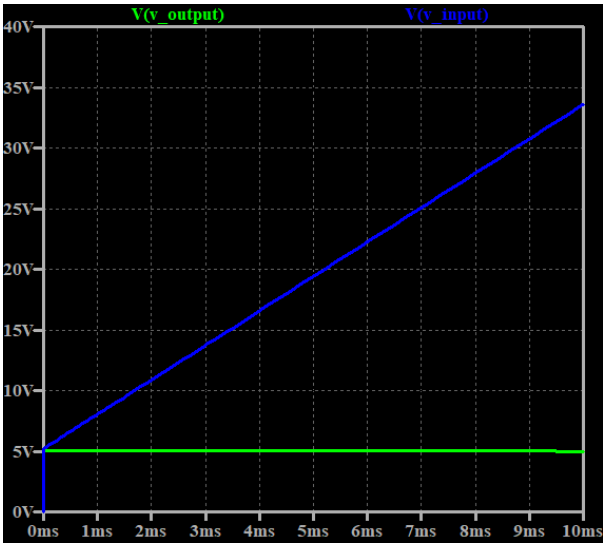

Figure 6: Linear Regulator Voltage Sweep

The GaN linear regulator was first prototyped with a single pass element MOSFET. It was found that having a single element led to a very high level of thermal dissipation within the MOSFET when a large voltage margin was induced between the input and output of the regulator, even for low load power draw. The module was thus redesigned to utilize four parallel MOSFETs.

For an initial test of the module, the converter was powered using a 7.4V bus voltage and set to regulate a 5.0005V output across a 100-ohm load. The linear regulator produced a peak-to-peak voltage noise at the output of 0.08V.

The converter was also subject to testing to determine the minimum input voltage required to produce a regulated 5V output, commonly known as the drop-out voltage. The converter output voltage began to lower when the input voltage fell below 0.017V above the output.

Switching Converter

The switching topology utilized for the module design is a synchronous non-isolated buck converter topology. This topology was selected to allow for the use of COTS gate drive controllers, greatly simplifying the design cost and module area requirements. A COTS gate drive controller and a custom feedback design utilizing discrete components were investigated as options for the final subsystem topology. The COTS controller has the benefits of ease of integration, simplicity of control and

significantly smaller footprint when compared to the discrete controller design. The discrete controller provides higher levels of system status information and a higher level of flexibility in component selection, enabling a more precisely tailored circuit; however, this comes at the cost of the unit price and footprint being increased by a factor of 3.4 over the COTS controller. As the module is designed to have fault tolerance through system level redundancy and priority towards small solution size, the COTS IC controller design will be incorporated into the final PoL system design.

The converter has been tested using a PWM signal generated by an STM32F303K8 Nucleo development board. The STM32 internal clock was configured for 64MHz operation, and the PWM output was enabled on timer 1 for channel 1 and inverted on channel 4. The PWM was set to have a prescale value of 1 and an auto-reload value (ARV) of 32. These settings produced a PWM output and matching inverted output running at 970kHz. The PWM duty cycle required to produce a target output voltage of 5V was determined using Equation 1, where duty cycle is rounded to the nearest whole integer.

$$\frac{ARV * V_{out}}{V_{in}} = Duty\ Cycle \quad (1)$$

Two tests were performed to measure the output noise of the switching converter. Both tests utilized a targeted output of 5V, regulated from both a 5.2V and 33.6V bus voltage. The converter output had a 100-ohm resistor added to act as a load to the circuit, ensuring a load current draw of 50mA. The results of the two tests are listed in Table 1.

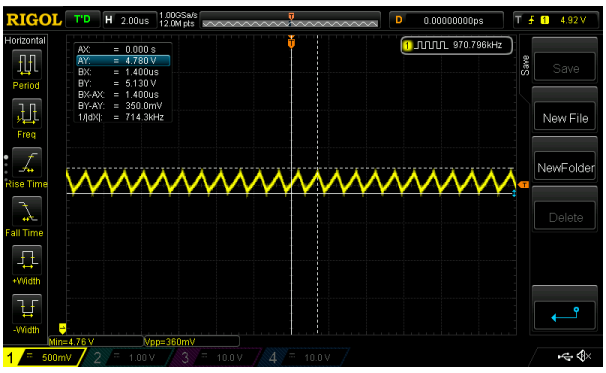

Figure 7: Converter Ripple, 5.2V Input Voltage

The high load ripple voltage, shown in Figure , indicates that there is a parameter mismatch between the output capacitor, switching frequency and load. Table 1 shows the results of changing circuit parameters to investigate the cause of the ripple. Increasing the switching frequency while maintaining the duty cycle reduces the output ripple voltage, but also reduces the overall output voltage across the fixed load resistor. It can therefore be inferred that the circuit requires a higher load capacitance to smooth fluctuations in the output.

Table 1: Switching Converter Ripple

Input (V)	Frequency (MHz)	Duty Cycle (%)	Output (V)	Ripple pk/pk (V)	Output vs Ripple (V/V)
7.4	1	68.75	4.911	0.35	1.719
7.4	1	75	5.342	0.4	2.137
7.4	2	75	5.168	0.28	1.447
7.4	4	75	4.858	0.23	1.117
7.4	8	75	3.865	0.15	0.580
29.6	1	15.625	4.445	0.7	3.112

Load Switch

The load switch consists of a GaN MOSFET acting as the power pass element, alongside a buffered gate drive circuit. The activation signal to the load switch enables and disables conduction of a GaN MOSFET configured as a logic inverter. The inverted input signal is then used to switch the gate of the buffered output switch. The buffered output switch acts to isolate the input voltage from the high voltage required to enable full conduction of the GaN pass element. The load switch circuit is shown in Figure .

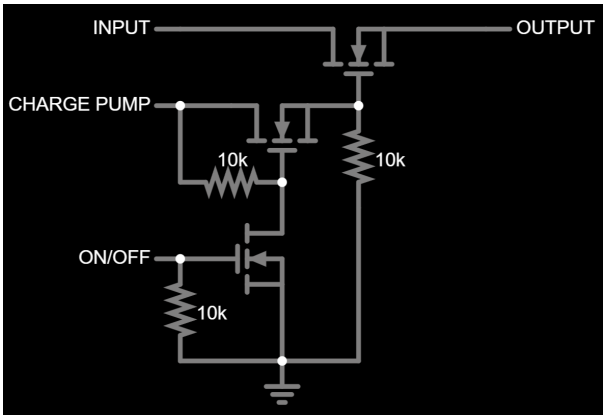

Figure 8: Load Switch Circuit

The pass element gate drive voltage is produced by a charge pump circuit that is tracking the pass element input voltage. Two load switches are used in the circuit, connected to the high and low side of the switching converter. These switches act to isolate the converter from both the load and the supply, disabling the circuitry when not in use. This ensures that the converter cannot

draw power from either the spacecraft bus or the load voltage when deactivated.

Current Sensor and Majority Voter

The current sensor circuit consists of a single load sense resistor in series with the module output, to which three individual amplified current-to-voltage converters are connected. The amplifiers have feedback networks tuned such that the output voltage of the amplifier when at the optimal current switch point falls within a 0 to 2.5V reference voltage range.

The output from each of the three amplifiers is routed into three voltage comparator circuits, where the analogue output from the amplifier is converted into a binary on/off signal depending on if the load current is higher or lower than the optimal current switch point. The comparator has a small amount of hysteresis added to each module, in the form of a feedback resistor network, to prevent oscillation of the output if the load current is close to the switch point. The output of each of these comparators forms the inputs to the majority voter circuit.

The two-of-three majority voter has been simulated with 13 n-channel GaN MOSFETs using LTSpice. The simulated circuit uses a 5V TTL logic level voltage to switch a 5V drive voltage level on the GaN MOSFETs.

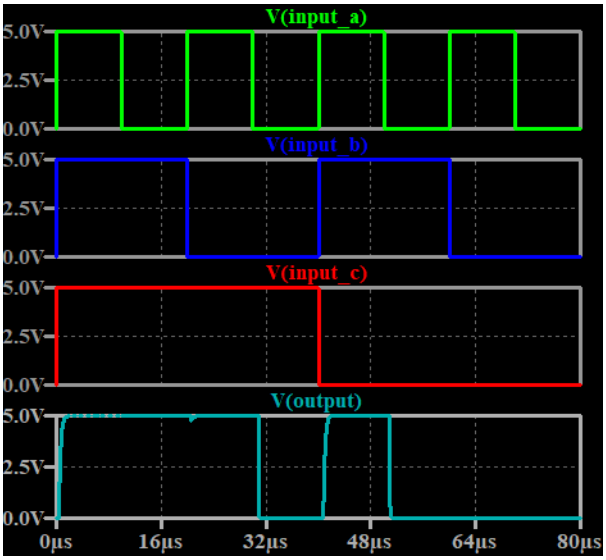

Figure 9: Majority Voter 100kHz Waveform

The circuit consists of three identical, parallel and-gate stages that drive two series-connected or-gates. The inputs (*input_a*, *input_b* and *input_c* in Figure) are connected to the three and-gate stages as combined pairs of the input signals, generating the outputs *AB*, *AC*, and *BC*. The and-combined pairs of signals are then fed into the or-gate pair to produce the final logic output, *AB|AC|BC*. During simulation, the circuit was found to be able to switch at a rate of 100 kHz with minor distortion to the output waveform. The switching waveform from this simulation is shown in Figure 10. The distortion was found to be caused by the current limiting resistors that are acting in place of a high-side p-channel MOSFET as would be included in a silicon logic gate. Lower distortion at high switching frequency must be traded against the higher current draw of the system when smaller resistors are used. The simulated system in Figure 3 has used 1 kilo-ohm resistors in the design, and peak current draw reaches 26mA during the switching test period.

CONCLUSION

Through computer simulation of subsystem level hardware blocks, a point of load converter has been developed targeting operation within a deep-space CubeSat. The system was successful in regulating the desired output power from the target input voltage range. Assembly of initial physical hardware was undertaken, and testing to verify the functionality of these systems has been performed. It was determined that it is possible to assemble most of the point of load system using COTS gallium nitride MOSFETs, reducing the size of the converter when compared to currently available radiation-hardened power modules.

FUTURE WORK

The point of load converter has several upcoming tasks that will need to be completed before it is ready for integrated testing. The outstanding circuits that have not been assembled will need to be completed and have functional testing performed to ensure that the hardware functions outside of a simulated environment. The switching converter will need additional analysis to optimize the output capacitor and inductor once a PWM drive frequency has been selected. After the modules have been constructed and the switching converter is optimized, the complete point of load module can be assembled in a distributed form to verify the switching logic functionality. The module can then be integrated into the final combined form factor in preparation for environmental testing.

Environmental testing will consist of verification of converter functionality during and after traditional spacecraft environmental stress testing. This includes thermal vacuum cycling across a range of expected temperatures and vibration functionality testing.

After the standard space environment testing is complete, the module will be further tested for deep space by verifying operation of the circuit under adverse

radiation conditions. The radiation conditions will be matched to the expected conditions encountered in deep space, and the module will be checked for single event transient errors alongside total dose related errors. The radiation conditions will be generated at the Heavy Ion Accelerator Facility, located in Canberra, Australia. This will be the first test of its kind being performed at the facility, and thus before the test can be undertaken a beam profile must be developed to match the cislunar space environment.

ACKNOWLEDGEMENTS

This work has been enabled by the support of the Space Science and Technology Centre, Curtin University. The author would like to acknowledge the staff and researchers of the Binar Space Program for assisting in the planning and proofreading of this paper, alongside Prof. Phil Bland and Dr. Robert Howie for their ongoing supervision and encouragement.

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